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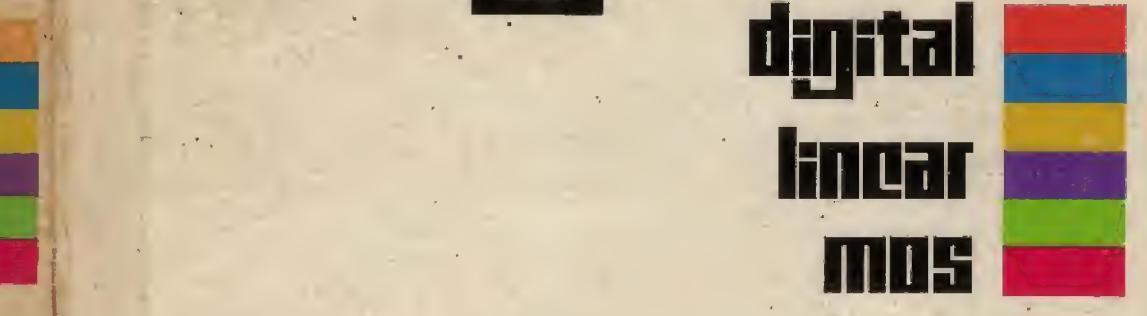

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82 series (except as noted on the data sheet)
82S series (except as noted on the data sheet)
8T series (except as noted on the data sheet)
Bipolar Memories: 82S06, 82S07

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INTERFACE
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8T00 Interface Functional Index

8T00 INTERFACE

DIGITAL 8000 SERIES TTL/MSI

NIXIE* DECODER/DRIVER

DESCRIPTION

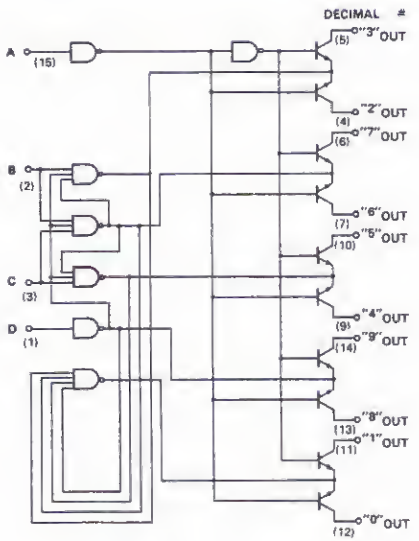
The 8T01 Nixie Decoder/Driver is a one-out-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes. Typical output breakdown voltages are in excess of 90 volts.

The 8T01 may also be utilized in driving relays or other high voltage interface circuitry. The element is designed with a dielectric isolation process utilizing TTL techniques and is therefore completely compatible with DTL and TTL elements.

The specially designed output drivers have extremely low leakage which eliminates background glow of off cathodes when driving Nixie tubes.

*Trademark Burroughs Corporation

LOGIC DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

MULTIPLEX OPERATION OF NIXIE TUBES USING SIGNETICS' 8T01 NIXIE DRIVER

Using the Burroughs Nixie Tubes designed for multiplexing techniques, a new approach to readouts can be taken which results in substantial device count savings. Specifically only one decoder/driver will be necessary to drive up to 20 Nixie tubes, though a memory element will be necessary to store the BCD codes, i.e., for 20 tubes one needs 20 four-bit words (assuming that the digits 0 through 9 are to be displayed).

Figure 1 is a block diagram of a logic subsystem for multiplexing Nixie Tubes. This technique can be achieved by combining the 8270 (four-bit shift) registers, 8T01 (Nixie decoder/driver) and 8281 (four-bit binary counter), 8277 (dual 8-bit shift register), in a small subsystem (implementation shown in Fig. 2).

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	8
1	0	1	1	9
1	1	0	0	8
1	1	0	1	9
1	1	1	0	8
1	1	1	1	9

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of a logic subsystem for multiplexing that recently appeared in an application note by Burroughs Corporation. (See Figure 2 for detailed drawing.) The system has a sequentially addressable word select memory with a capacity of N words where N is also the number of Nixie indicators in the system. Each word consists of at least four bits which represent, in binary form, the number of the corresponding decimal digit. The recirculation loop and the write circuits for the memory are not shown in Figure 1, but they would normally be required.

GENERAL MULTIPLEXED SYSTEM

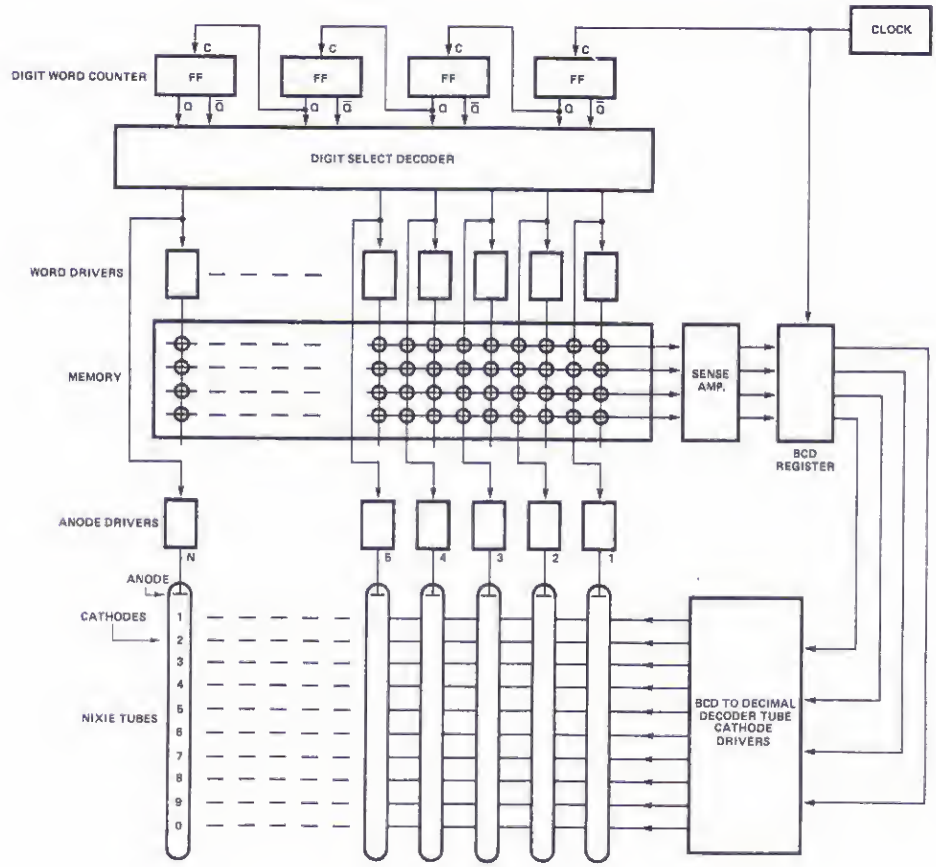


FIGURE 1

When displaying an N digit number, as illustrated in Figure 1, the N words of the memory are sequentially read out at a constant rate that is determined by the system Clock. Each time a word is read out, it is rewritten in the same position of the Memory, thus the information is preserved. When the displayed information is to be altered in one or more of the digit positions, the new information is written into the corresponding word position in the memory, just after the existing words are read.

SUBSYSTEM FOR MULTIPLEXING 16 NIXIE TUBES

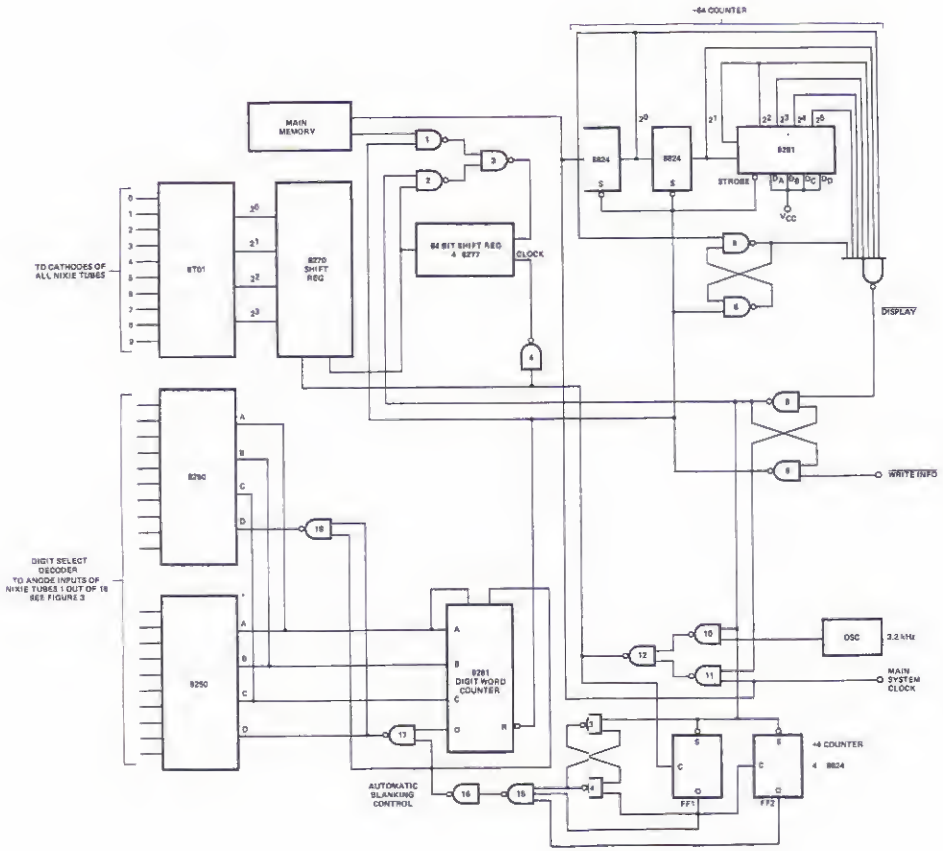


FIGURE 2

Referring to Figures 1 and 2, four packages of 8277 (dual 8-bit shift register) are used to hold the 16 four-bit BCD coded words that determine what each Nixie tube will display. A four-bit binary counter (8281) is used as the digit word counter. A divide by four counter (2-8822) is used to enable the data after every 4th clock pulse. Two one-outbf-eight decoders (8250) are used to implement the digit sect decoder, which drives the appropriate anode througha circuit such as shown in Figure A. The Nixie driver (ff01) accepts the four-bit BCD code from memory and drivs the cathodes of the tubes.

ANODE DRIVING CIRCUIT

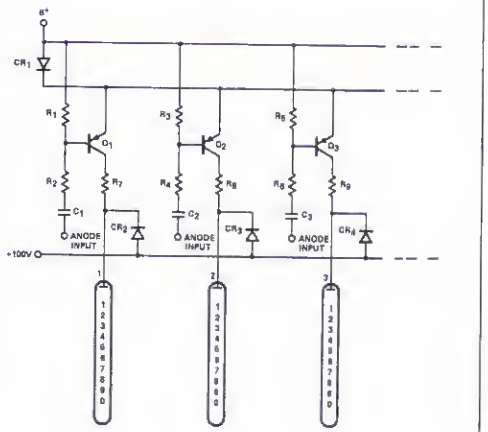


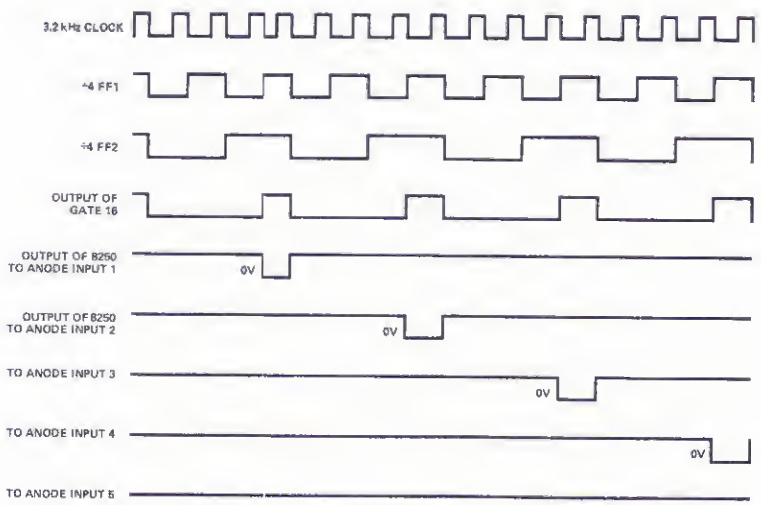
FIGURE 3

Figure 3 shows a constant voltage anode driver circuit. In the circuit, one of the transistors, Q_1, Q_2, Q_3, etc., is turned on while the others are held off. Diode CR_1, in conjunction with the base resistors, R_1, R_3, R_5, serve to back-bias the off transistors. To turn transistor Q_1 on, a negative pulse is applied to input number one. The components R_2 and C_1 are chosen to maintain transistor Q_1 in the on condition for the full period required by the system timing.

The collectors of the constant current drivers are connected through catching diodes CR_2, CR_3, and CR_4 to a +100 volt bus. This is done to prevent excessive voltages from appearing across these transistors. Without these diodes, overshoots would tend to occur due to the characteristics of the Nixie tube.

The 3.2kHz oscillator results in a 50Hz signal to an individual anode input. This is sufficiently greater than minimum eye "flicker" frequency (approximately 24Hz.) The upper limit of this oscillator could be 10kHz which will result in a minimum "ON" time of 100 microseconds for each tube. If the main clock repetition rate falls between these limits, there is no need for the oscillator.

TIMING DIAGRAM FOR 16 TUBE SUBSYSTEM



NOTE: ASSUMES THE 64-BIT SHIFT REGISTER HAS BEEN LOADED. NOTE THAT AFTER EVERY 4TH CLOCK (NEATIVE-GOING EDGE) ONE ANODE INPUT OUT OF 16 IS ENERGIZED. THUS ALL 16 TUBES WILL HAVE EEN ENERGIZED AFTER 64 CLOCK PULSES HAVE OCCURRED.

FIGURE 4

DETAILED DESCRIPTION

Refer to Figure 2 and Figure 3. The 64-bit shift right register is loaded from the main memory with the coded numbers to be displayed by each tube. The operation s as follows:

The write information input (Figure 1) normally logic "1" is set to a logic "0" level (pulsed operation). This allows the words in main memory to be shifted into the register. Also, the main clock from the calculator advances a counter such that after 64 counts the display input is set to logic "0" (pulsed operation), inhibiting any further counter advancement, or loading of the shift register. Simultaneously, as the display input goes to a logic "0", the 3.2kHz oscillator starts cycling the 64-bit shift register. Simultaneously, as the display input goes to a logic "0", the 3.2kHz oscillator starts cycling the 64-bit shift register.

The above is accomplished via the following individual steps:

The latch formed by gates 8 and 9 is initially set such that the output of 8 is a logic "0" level. The output of 8 inhibits the ÷ 4 (divide by four) counter, the 8281 (Digit Word Counter), and conditions the latch formed by gates 13 and 14 such that the output of 14 is set to a logic "0" level. As a result of this action, the output of 16 is a logic "0" level which forces the output of gates 17 and 18 to logic "1" levels.

Logic "1" levels at the "D" input of an 8250 (one out of eight decoder) inhibits the output by forcing them all to logic "1" levels.

At the point in time just prior to the negative-going-edge of the 64th clock pulse, all anode inputs to the NIXIE tubes have been at logic "1" levels. (Logic "1" from the 8250's).

After the 64th pulse (from the main system clock), the ÷ 64 (divide by 64) counter is decoded and the output of gate 7 goes to logic "0", forcing the latch formed by gates 8 and 9 such that the output of 8 is set to a logic "1" level, thereby releasing the inhibit on the ÷ 4 and 8281 counters.

Also, all the codes for the digits to be displayed are in the 64 bit shift register and the system is now ready for multiplexing to commence.

Now the system is in the multiplex routine, which is as follows:

The system is clocked by the 3.2kHz oscillator.

The ÷ 4 counter controls the anode strobing by holding the outputs of the 8250's at logic "1" levels for 4 clock pulses, then allowing one output to make the "1" to "0" transition thus firing the number one NIXIE tube viz. the input capacitor (1μf).

The time constant, TC(1K, 1μf) allows the tube to conduct for approximately 300 microseconds.

The next clock (5th pulse) shuts off the 8251's. When the negative-going-edge of the 8th (eighth) pulse has occurred, then the number 2 NIXIE will be fired. The process repeats for all 16 tubes.

The 8281 (Digit Word Counter) is advanced by the ÷ 4 counter. Therefore, the 8281 gets advanced *after* the negative-going-edge of every 4th pulse issued by the oscillator.

The outputs of the 8281 are decoded by the 8250's which fire the anodes of the NIXIE tubes.

The 64-bit shift register circulates the 16 BCD coded words that are to be displayed.

The 8270 (4-bit shift register) receives the BCD information from the 64-bit shift register and in turn is decoded by the 8T01 (BCD to Decimal) which drives the cathodes of all 16 tubes simultaneously.

Thus the operation is complete. The automatic blanking control ensures that the tubes are not conducting for 4 shift pulses while the next BCD coded word is shifted into the 8270.

DIGITAL 8000 SERIES TTL/MSI

SEVEN SEGMENT DECODER/DRIVER

INTRODUCTION

The Signetics' 8T04/5/6 are monolithic MSI seven segment decoder/drivers that have been designed with TTL techniques. They consist of the necessary logic to decode a 4-bit BCD input to provide the appropriate outputs to drive seven segment digital display devices. Numerals 0-9 as well as selected signs and letters can be decoded for driving the following types of displays:

- Light emitting diodes displays (LEDs)
- Incandescent displays
- Interface transistors and SCRs
- Relays

The three decoders differ basically in the electrical characteristics of the output transistors and their logical activating level. Figure 1 shows a composite logic diagram. The 8T04 has "active low," high current sink open collector outputs for driving indicators directly. The 8T05 has "active high" outputs with internal pull-up resistors to provide sufficient drive current to discrete transistors, SCRs and other interface elements as well as Utilogic NOR and OR gates. The 8T06 also offers "active high" outputs but these are of the open collector type for maximum versatility in a variety of current source applications.

LOGIC DESCRIPTION

A composite truth table (Table I) has been arranged to show the response of the 8T04/5/6 seven-segment decoder /drivers to a 4-bit binary input code. When neither of the auxiliary inputs are activated, a BCD code on the inputs (a, b, c, d) conditions the outputs (A through G) corresponding to a standard seven-segment layout as shown in Figure 2 such that numerals 0-9 can be displayed. Furthermore, any non-BCD input is defined as well such that selected signs and letters may be displayed in accordance with Table I.

Auxiliary terminals are provided for maximum versatility. A ripple blanking input (RBI) and a ripple blanking output (RBO) are used to suppress leading and trailing edge zeros in multidigit displays. In addition, the internal logic design allows the ripple blanking output to serve as a blanking input as well and is therefore designated as RBO/BI. This blanking input (BI) overrides the ripple blanking signal and may be used in various blanking and intensity modulation applications.

The lamp test (LT) input is independent of any other input and may be activated at any time. This input allows the integrity of the display to be checked by overriding all other input states.

LOGIC DIAGRAM

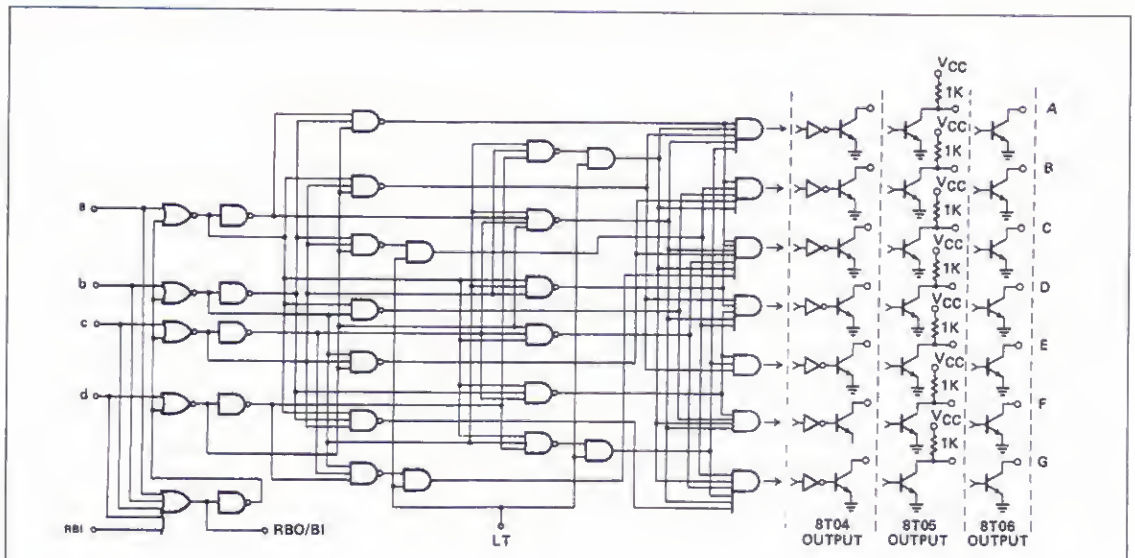
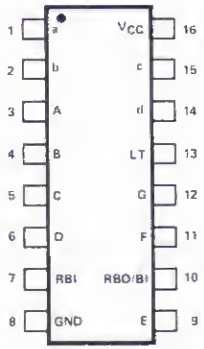


FIGURE 1

PIN CONFIGURATION AND 7–SEGMENT LAYOUT



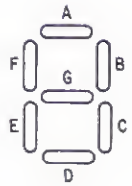


FIGURE 2

Where: a, b, c, d are the BCD inputs to the decoder/driver
A, B, C, D, E, F, G are the seven-segment outputs in accordance with the standard layout as shown.

RBI = Ripple Blanking Input
RBO/BI = Ripple Blanking Output/Blanking Input
LT = Lamp Test

TRUTH TABLE

TABLE 1

INPUTS						BI/RBO	OUTPUTS 8T04							OUTPUTS 8T05/06							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							OUTPUT STATE							
d	c	b	a	LT		NOTE	A	B	C	D	E	F	G	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	0	0	0	0	0	0	0	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 (Note 1 & 2)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 (Note 2)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	1	0	0	1	1	1	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	0	0	1	0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	-
1	0	1	1	1	X	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	0	0	0	1	0	0	0	1	1	1	0	1	1	1	R
1	1	0	1	1	X	1	1	1	0	1	1	1	1	0	0	1	0	0	0	0	,*
1	1	1	0	1	X	1	1	1	1	0	0	0	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	BLK

NOTE:

1. RBO/BI used as input
2. RBO/BI should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.
3. * Comma
4. X = Do not care, either "1" or "0"

TERMINAL CHARACTERISTICS

Since these 7-segment decoder/drivers are useful in many applications and interfacing situations involving bipolar as well as MOS circuits, it is important to have a complete understanding of the 8T04/5/6 characteristics.

The data inputs as well as the RBI input are TTL type base-emitter diodes. Clamp diodes are employed to prevent ringing that may occur on long interconnect lines. The equivalent circuit is shown in Figure 3.

The RBO/BI signal is generated as shown in Figure 4. When a BCD zero has been received at the data inputs with the RBI input being low, transistor Q turns on and the collector pulls the BI input low internally. Since the RBO/BI terminal may be grounded at any time, an overriding blanking signal can be supplied externally. To avoid forcing the collector high when Q is activated, the BI input should be driven by an open collector device such as an 8891.

The output transistors of the 8T04 and 8T06 are open collector devices. It can be seen from the equivalent circuit in Figure 5 that because of the collector-substrate isolation diode the output should not be taken more negative than 0.5V without current limiting. The output leakage for the 8T04 and 8T06 is specified at 100μA with 6V applied. Because collector breakdown typically occurs above 15V, an application may be considered with output voltages higher than 6V but below breakdown when using a selected device. In that case, current limiting to about 10mA should be employed to avoid excessive power dissipation in the output transistor.

The equivalent circuit for the 8T05 output which has an internal diffused pullup-resistor is shown in Figure 6. In interfacing it should be noted that the output will clamp at one diode drop above V_{CC}.

To allow judicious tradeoffs in designs, typical characteristics for current source and sink capability are given for the respective devices in Figures 7 through 9.

EQUIVALENT CIRCUITS

DATA INPUTS AND RBI

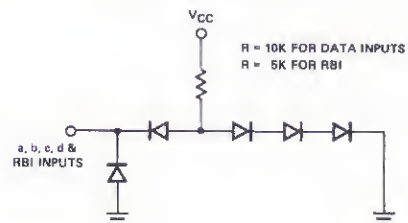


FIGURE 3

EQUIVALENT CIRCUITS (Cont'd.)

RBO/BI TERMINAL

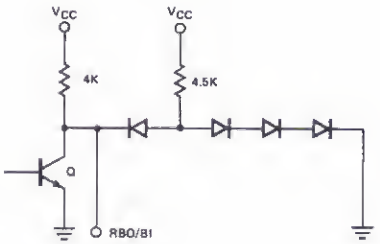


FIGURE 4

8T04 AND 8T06 OUTPUTS

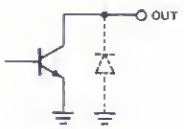


FIGURE 5

8T05 OUTPUTS

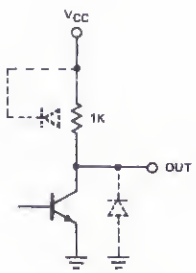


FIGURE 6

TYPICAL CHARACTERISTICS

TYPICAL CURRENT SINK CHARACTERISTICS OF THE 8T04 & 8T06 (OUTPUTS A THROUGH G)

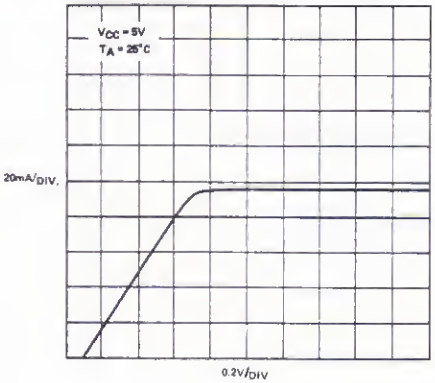


FIGURE 7

TYPICAL CURRENT SINK CHARACTERISTICS OF THE 8T05 (OUTPUTS A THROUGH G)

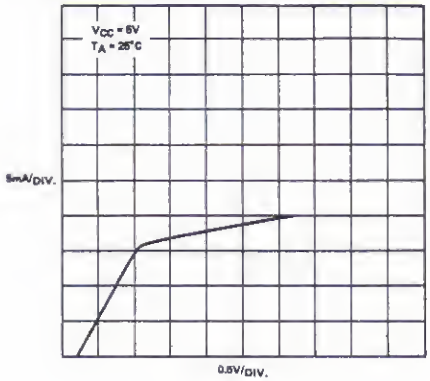


FIGURE 8

TYPICAL CURRENT SOURCE CHARACTERISTICS OF OF THE 8T05 (OUTPUTS A THROUGH G)

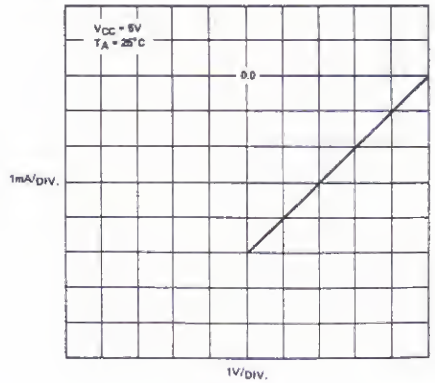


FIGURE 9

OUTPUT SPECIFICATIONS

Table 2 is designed to assist in selecting the proper decoder for a desired application. The 8T04 has "active low" outputs. Thus it is suited for high current sink applications where the driver has to sink current from a load. However, the 8T05/6 devices have "active high" outputs, meaning that they are well suited for applications where current has to be sourced to the load. This may be done either through the internal pullup resistor (8T05) or through an externally provided element (8T06) when high current is required.

OUTPUT SPECIFICATIONS OF THE SEVEN SEGMENT DECODER/DRIVER

TABLE 2

PART NO.	OUTPUT STRUCTURE	ACTIVATING LEVEL	CURRENT SINK SPECIFICATIONS	OUTPUT "1" LEAKAGE OR CURRENT SOURCE SPEC.
8T04	OPEN COLLECTOR	LOW	40mA @ .4V	100μA @ 6V
8T05	PASSIVE PULL–UP	HI	.5mA @ .3V	–2.3mA @ 1V; –500μA @ 3.9V
8T06	OPEN COLLECTOR	HI	40mA @ .4V	100μA @ 6V

APPLICATIONS

Several techniques are used for driving digital display devices. The most straightforward application is to use one 7-segment decoder/driver for each display. Because a blanking provision is available, the displays may be strobed for low power operation or variable light intensity.

Depending on the existing circuitry it may also be advantageous to time-share one decoder among several or all displays. In such a multiplexed operation, suitable timing and decoding are incorporated such that only one display will be illuminated at a time. This strobed operation is done at a repetition rate high enough to appear flicker free to the eye.

LIGHT EMITTING DIODE DISPLAY

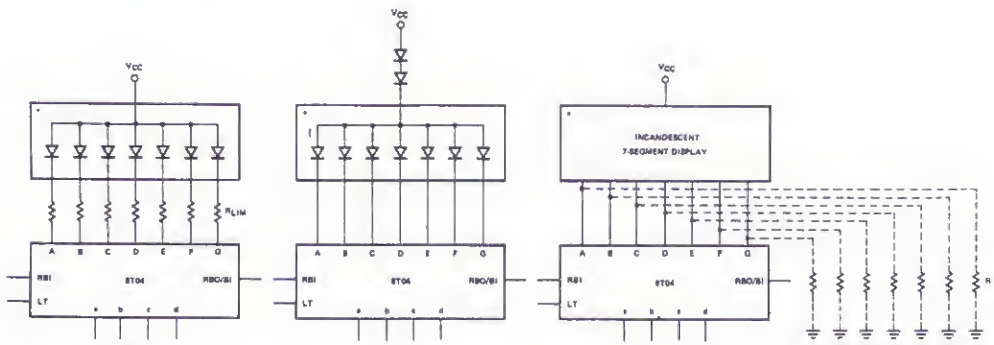
Several light emitting diode displays (LEDs) have common anpdes. These require a decoder/driver with "active low" outputs and high current sink capability. Similar requirements exist for incandescent displays and the 8T04 is ideal for these applications without the need for interface transistors.

The turn-on characteristics of the display are important when interfacing with the decoder/driver. Figure 10a shows the 8T04 driving a light emitting diode display. Since the forward drop of the LEDs may be slightly unequal, they may exhibit current-hogging if driven from a common voltage source. Thus, to obtain equal brightness in the display segments, LED manufacturers generally advise to use individual current limiting resistors. However, LED displays have been used successfully without an apparent difference in brightness as shown in Figure 10b. Current limiting resistors are therefore eliminated.

An important consideration for incandescent displays is inrush current through a cold filament, since it could be 10 times as high as the rated operation current. Figure 10c shows the 8T04 driving an incandescent seven-segment display and if the external resistors R (dotted connections) are used, a small current is allowed to flow through the lamps during the off-state, keeping the filaments warm. Thus, inrush current effects are minimized, prolonging the life of the lamp.

Surge current protection of the driver is not required in this context because the current-sink capability of the output transistors is beta-limited. Typical tests have shown that the output characteristics flaten out at about 80mA (Figure 7), therefore setting a natural limit to inrush current. Consequently, no damage to the driver will be sustained when driving lamps that have steady state currents falling within the defined output drive capability of the seven-segment decoder/driver.

8T04 DRIVING 7–SEGMENT DISPLAY



NOTES:

1. LED displays such as: Litronix Data Lit 10 ,Monsanto Man 1, Opcoa SLA 1.
2. Incandescent displays such as: Pinlites "Lite Pak" ,RCA Numitron DR 2000, Readouts Inc. Series 5.

FIGURE 10

8T05 INTERFACING APPLICATION

The 8T05 has "active high" outputs with internal 1K ohm pullup such that external buffers may be driven directly without the need for additional components. Hence, it is easy to interface with driver transistors that may be required for very high current incandescent lamps or high voltage interfaces to fluorescent or gas discharge displays.

Should the need exist to interface with logic circuits, one standard TTL load (-1.6mA @ .4V) can be driven. Utilogic OR and NOR gates have base inputs and only require 180μA input current, thus allowing a fanout of 10. The 8T05 can also be used to drive SCR's such as to interface the 7-segment decoder with electroluminescent displays that require high AC voltages. Such an application is shown in Figure 11.

If additional drive current is required from the 8T05 it is possible to add external resistors from V_{CC} to the 7-segment outputs of the decoder/driver. Since the minimum value of the total pullup resistors is constrained by the current sink capability of the output transistors, it is advantageous to use the 8T06 which is pin compatible and designed for high current source applications.

LED DISPLAY USING THE 8T06 DRIVER

Monolithic light emitting diode displays are presently manufactured with common cathodes which require a driver with current source capability. The 8T06 7-segment decoder/driver has been designed specifically to drive common-cathode LEDs, and employs open-collector transistors for maximum versatility. External pullup resistors must be used to limit the source currents in accordance with the LED manufacturers specifications and the intended usage of the display. A typical application of the 8T06 driving a common cathode LED is shown in Figure 12. Because of the 8T06's high current sink capability (40mA), it can be used as a LED driver for pulsed operation or in the multiplex mode where only one decoder/driver is used for a multidigit display. Figure 16 shows such an arrangement in detail.

8T05 DRIVING ELECTRO–LUMINESCENT DISPLAY

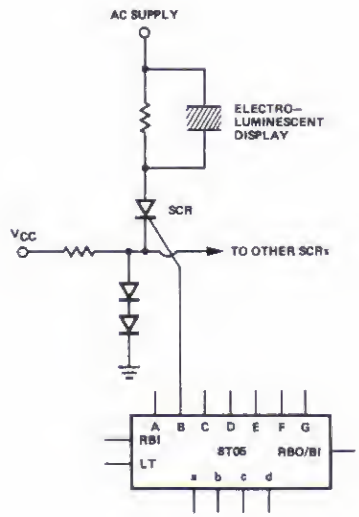


FIGURE 11

8T06 DRIVING MONOLITHIC LED DISPLAY

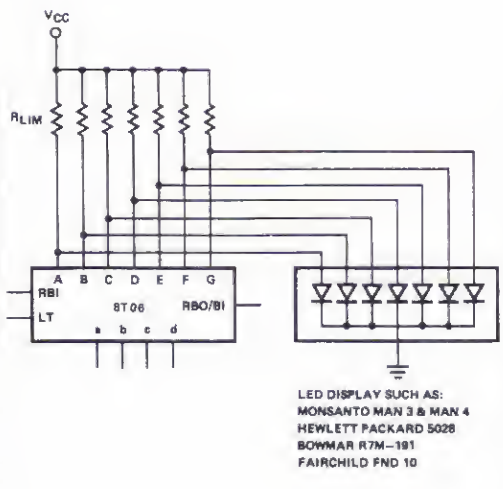


FIGURE 12

RIPPLE BLANKING AND INTENSITY MODULATION APPLICATION

The provision for automatic blanking of leading and/or trailing edge zeros is a very useful feature in multi-digit displays. By blanking insignificant zeros, any display can be easily read. For example, in a ten digit display a mixed integer fraction (000457.1800) would be displayed as 457.18.

To suppress leading edge zeros, the Ripple Blanking Output (RBO) of a decoder is connected to the Ripple Blanking Input (RBI) of the next lower stage device. In the total display, the most significant bit's RBI input is connected to ground to enable the blanking command to ripple through if that decoder is addressed with a BCD zero (0000). It is common practice to tie the least significant bit's RBI input to V_{CC} since it is generally not desirable to blank the least significant integer. Figure 13 shows an example for n-integers.

Trailing edge zero suppression is needed when the fractional part of a number has to be conditioned similar to the example above. Because it is desirable to retain the first zero after a decimal point, the RBI input of the most significant digit in the fractional part should be tied to V_{CC}.

The RBO terminal may also be used as an overriding blanking input (BI) in a variety of inhibiting and strobing operations that may be associated with the outputs. An extremely useful application also shown in Figure 13 is intensity modulation. The variable duty cycle multivibrator can be used for low duty cycle strobed operation or display dimming.

FLOATING DECIMAL POINT APPLICATION

The ripple blanking shown in the previous example may be extended to an application such as desk calculator displays where the position of the decimal point can be selected. In Figure 14 a few additional gates are used such that the decimal point can be fixed by means of a "select line". To select the decimal point position, the corresponding select line must be at a logical "1" while all the other select lines are held at a logical "0".

As a result, the least significant integer as well as the most significant part of the fraction will not be blanked (since 0.0 may occur which is a meaningful result) but any other leading or trailing edge zero will be blanked to obtain an easily readable display.

SEVEN–SEGMENT DISPLAYS FOR n–INTEGERS

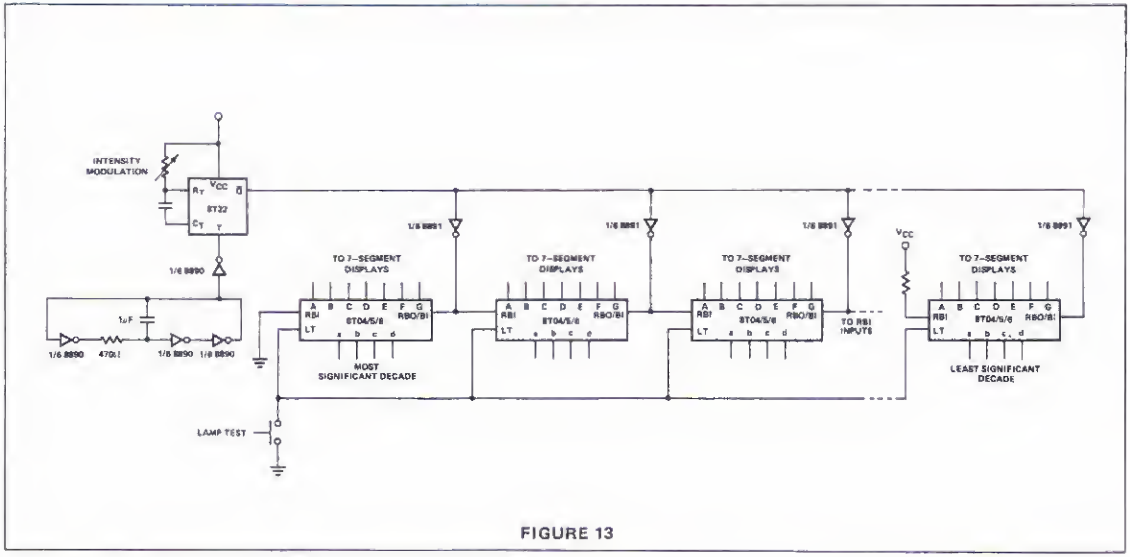


FIGURE 13

NOTES:

1. RIPPLE BLANKING– Automatically suppresses all unnecessary zero's which may be either those preceding the first significant digit (as shown) or those trailing the last significant digit after a decimal.
2. LAMP TEST– Overrides all output states generated from input codes.
3. INTENSITY MODULATION– Turns on the seven-segment displays only for the pulse duration. This may be used as a lamp intensity control or for low duty cycle pulsed operation.

8 DIGIT DISPLAY WITH FLOATING DECIMAL POINT AND RIPPLE BLANKING

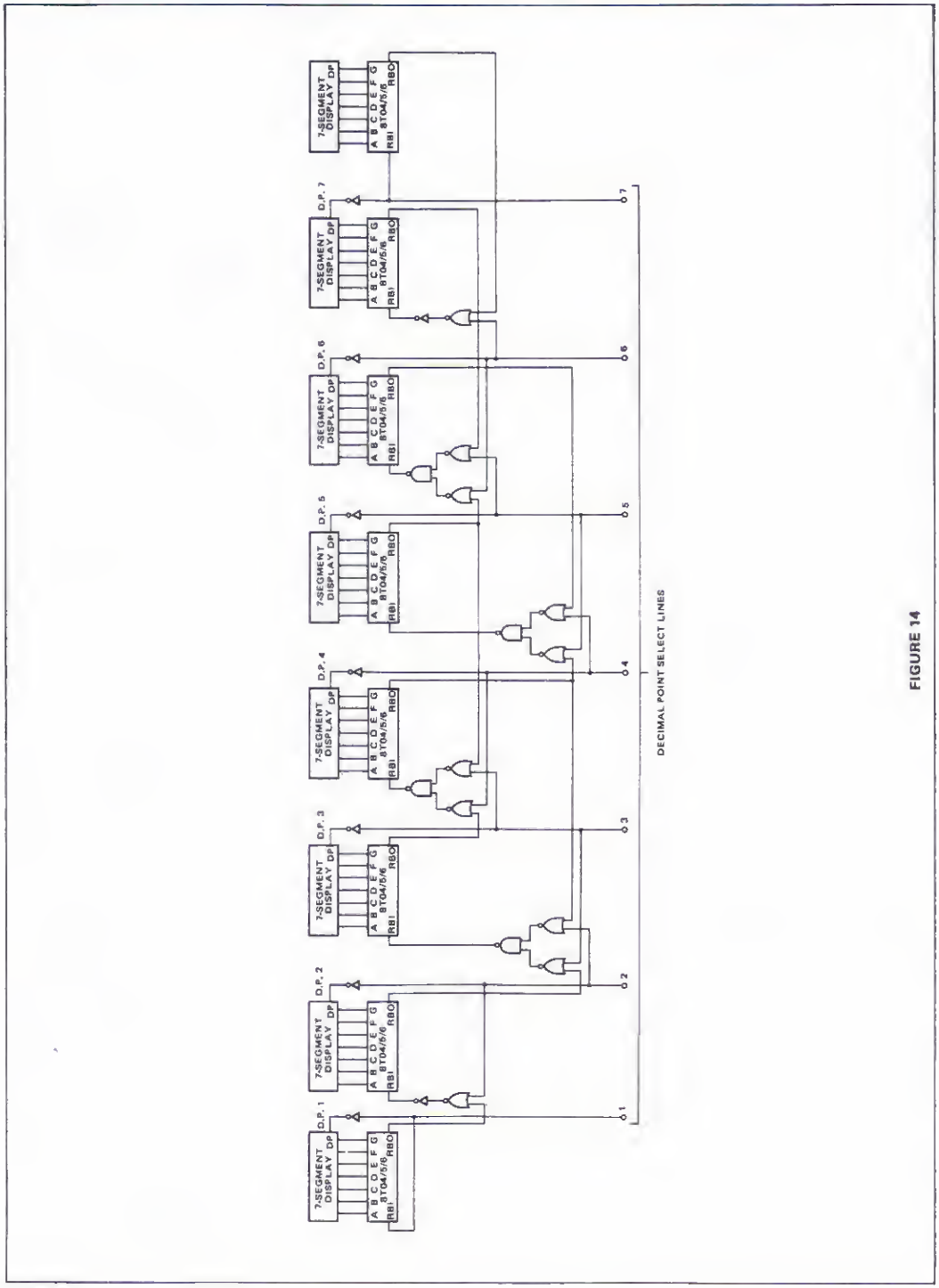


FIGURE 14

NOTES:
1. To select a decimal point, the corresponding select line must be at a logical "1" while all the remaining select lines are held at logical "0"s.
2. Gates used: 8880 Quad 2-input NAND Gate; 8885 Quad 2-input NOR Gate; 8890 Hex Inverter.

MULTIPLEXING OF DISPLAYS

When designing with multidigit displays, two distinctly different approaches may be taken when interfacing the displays with the decoder/driver circuitry. The standard solution would be to use one decoder/driver for each digit in the display. As the number of digits increases it is generally advantageous to time-share one decoder/driver among all digits or groups of digits as shown in Figure 15.

The choice of one technique over the other depends heavily on the application. In particular, the total hardware cost, package count, and power consumption in a multiplexed display system are not only influenced by the number of digits that time share a decoder/driver, but also if the BCD data is available in serial or parallel form.

The principal argument that may be advanced for multiplexing of displays is generally one of economics although a considerable power savings may result as an added benefit. For example, LED 7-segment displays have a high persistence allowing them to be strobed with a very low duty cycle which is an important consideration for battery powered equipment.

A circuit for multiplexing a counter display is shown in Fig. 16. By using the 8T10 Quad-D-Type Bus Flip-Flop with tri-state outputs, for storage buffers, the digit information of all counter outputs can be bussed onto common BCD lines. Thus, the design of a multiplexed display is greatly simplified. In this example, common anode displays are driven by an 8T04. Current limiting resistors are used in each 7-segment line to assure equal brightness even if the LED turn-on voltages are slightly unequal.

The 8250 Octal decoder that selects the BCD information from 8T10 buffers and corresponding digit drivers is indexed by an 8293 counter in the divide-by-8 mode. A 1kHz repetition rate for the multiplex oscillator was chosen which is high enough to make the display appear flicker free to the eye.

Notice that the 8T04 and 8T06 are very well suited for strobed operation of displays. Because of their high current sink capability, displays can be pulsed with high currents and low duty cycles, enhancing the apparent brightness of the displays and saving power at the same time. Use of the 8292 and 8293 counters further reduces system power consumption.

GENERALIZED MULTIPLEXING SCHEME FOR DISPLAYS

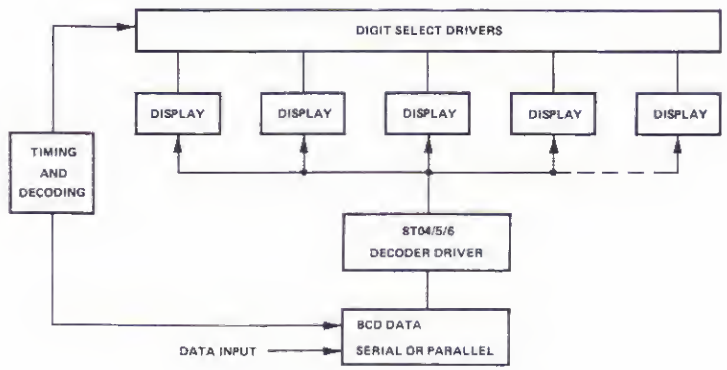
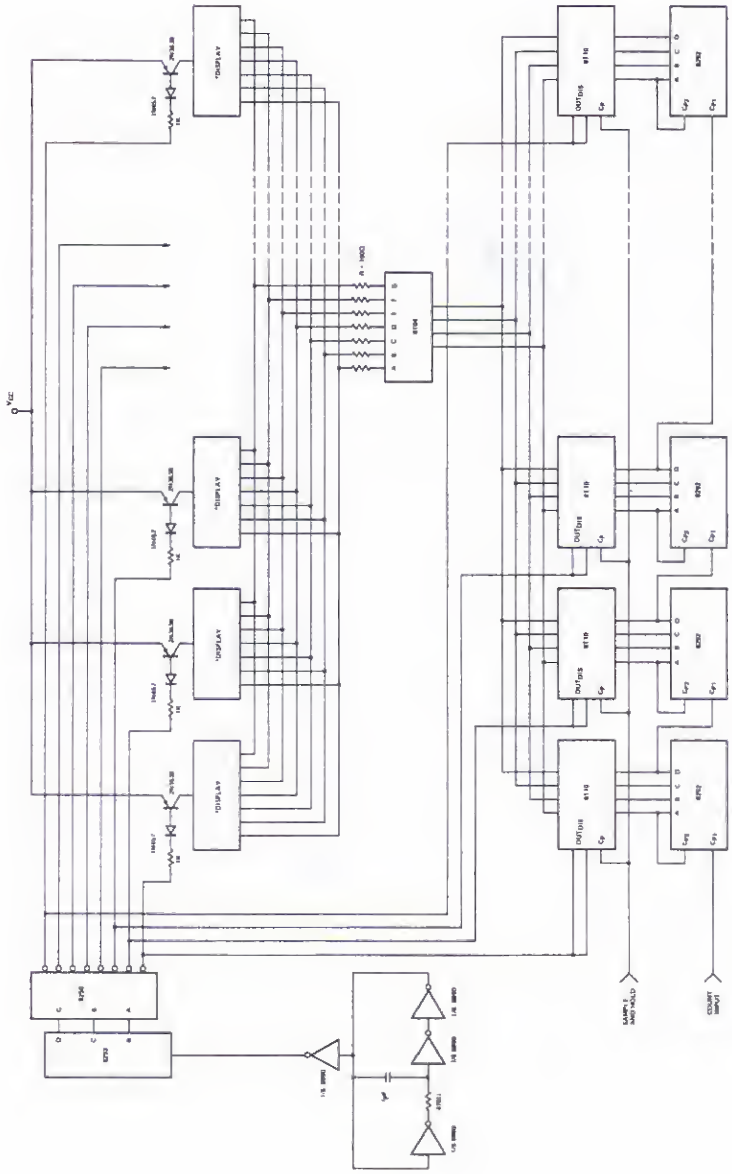


FIGURE 15

MULTIPLEXING EIGHT LED DISPLAYS



*Led displays such as Litronix Data Lit 10, Monsanto Man 1, Opcos SLA 1

FIGURE 16

DIGITAL 8000 SERIES TTL/MSI

8T09 QUAD BUS DRIVER/8T10 QUAD D-TYPE BUS FLIP-FLOP

INTRODUCTION

Designers of digital systems have been using open-collector TTL logic for many years because its wire-OR capability is a powerful design tool. With the addition of an external pull-up resistor, many open-collector outputs can be connected onto a common bus, resulting in a considerable savings of hardware and speed advantages over conventional approaches. Particularly in computer design where bus-organized systems architecture prevails, Signetics open-collector MSI and open-collector gates are used extensively.* There are applications, however, especially in systems with electrically short interconnects, such as on-card bussing and areas of modular systems design, in which performance can be improved by two new TTL compatible bus driver circuits that have been developed by Signetics.

SIMPLIFIED TRI-STATE BUS DRIVER

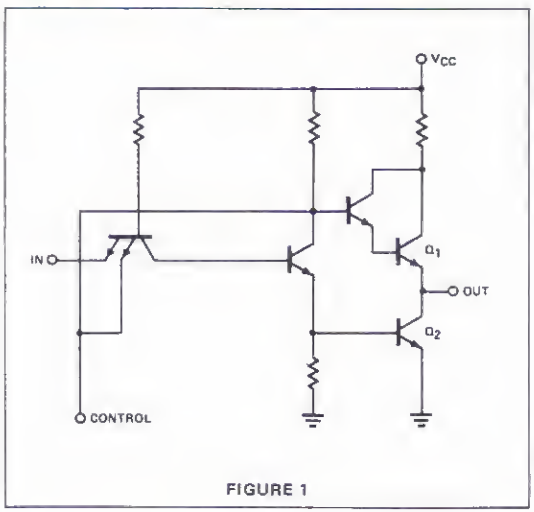


FIGURE 1

These designs, the 8T09 Quad Bus Driver and the 8T10 Quad D-Type Flip-Flop combine the advantages of active pull-up TTL with the wire-OR capability of open-collector ICs. As shown in the simplified circuit diagram in Figure 1, a bus driver can be designed to exhibit three distinct output states. Such a tri-state device is unique in that it may act as a normal TTL gate with low impedance logical "1" and logical "0" levels as long as the control line is high. If the control line is grounded, drive current is removed from the active pull-up Darlington-structure and a third, high impedance output state results. Since in that third state both output transistors (Q_1 and Q_2) are biased in the off-condition, only microampere leakage current will have to be supplied to the device by an active bus driver tied to the same bus.

Two integrated circuits, the 8T09 Quad Bus Driver and the 8T10 Quad D-Type Bus Flip-Flop that have tri-state outputs will be described here and applications such as bus organized information transfer, modular systems design and multiplexing will be discussed.

8T09 QUAD BUS DRIVER

The 8T09 Quad Bus Driver is a hardware realization of the tri-state bus driver concept. It may be seen from the circuit diagram in Figure 2 that depending on the state of the disable input, a driver will either act as a high speed inverting buffer or will exhibit a high impedance "OFF" state similar to an open-collector gate.

CIRCUIT SCHEMATIC OF 1/4 8T09

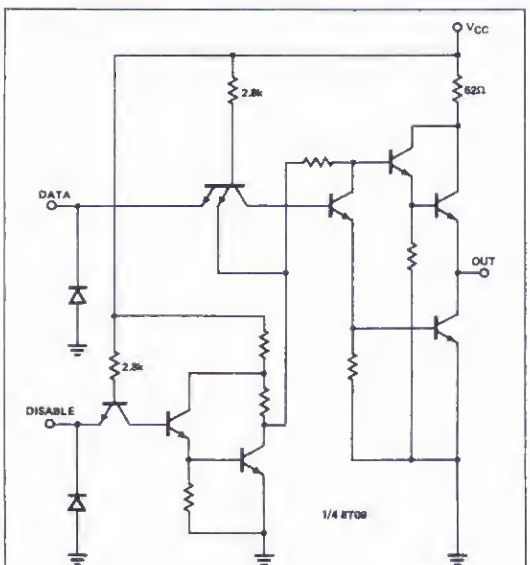


FIGURE 2

*Unified Bus Maximizes Minicomputer Flexibility, ELECTRONICS, December 21, 1970.

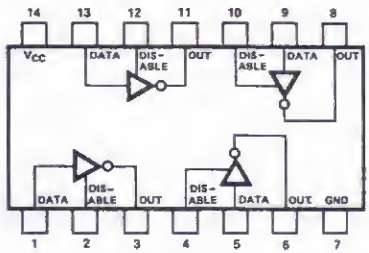
The Darlington pull-up structure at the output provides high current source capability (guaranteed 5.2mA at 2.4V) when driving a data bus, thus allowing high speed operation even when driving heavy capacitive loads. The current sink capability of the bottom transistor is 2-1/2 times that of a standard TTL gate (guaranteed 40mA at 0.4V) making the device very versatile in a variety of interface situations.

Figure 3 shows the logic diagram and truth table of the 8T09. A logical "0" on the disable input makes the bus-driver a high speed inverting buffer with low impedance logical "1" and logical "0" states. To place the output in the high-Z disable state, the disable signal has to be a logical "1". This fact is beneficial when considering fail-safe operation since removal of the disable signal, which may happen accidentally, will not damage any driver. The inputs of the 8T09s are diode clamped to discriminate against negative ringing.

APPLICATIONS OF THE 8T09 QUAD BUS DRIVER

Tri-state outputs combined with high-speed and high output current capability in both the logical "1" and logical "0" level allow the 8T09 to be used in a variety of bus-organized systems and wired-OR applications.

LOGIC DIAGRAM AND TRUTH TABLE OF THE 8T09



DATA	DISABLE	OUTPUT
0	0	1
1	0	0
0	1	HI-Z
1	1	HI-Z

FIGURE 3

In existing logic designs, the 8T09 may be used to replace open-collector devices to increase systems speed by as much as a factor of ten. This speed improvement is accomplished by the short propagation delays associated with the data path (10ns max.) and the excellent capacitive drive capability of the 8T09. As an added benefit, pull-up resistors are no longer necessary, which will also have an impact on new systems designs where bussing can be used.

Figure 4 illustrates the excellent drive capability of the 8T09. Since a disabled bus-driver is in the high-Z state and only requires 40uA leakage current, as many as 129 disabled drivers and a standard TTL gate (8880 or 7400)can be driven by one 8T09 in the logical "1" state. The 8T09 also has high current sink capability in the logical "0" state, making many other driver and receiver combinations possible. Of special interest is a bidirectional data bus as indicated in Figure 5. When using standard TTL gates as receivers such as 8880s and 7400s, as many as 25 receiver/transmitter pairs may be tied onto the same bus without exceeding the logical "0" drive capability of the 8T09.

LOGICAL "1" DRIVE CAPABILITY OF THE 8T09

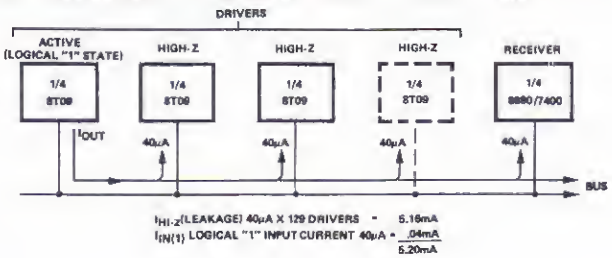


FIGURE 4

BIDIRECTIONAL DATA BUS

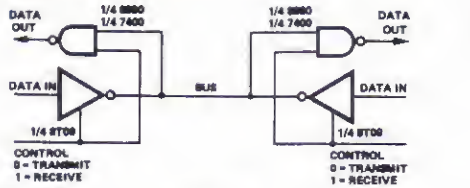


FIGURE 5

Standard MSI circuits may be adapted easily to bus-organized systems. By using the 8T09 as shown in Figure 6, a minicomputer can be designed using a single high speed bus. An arithmetic logic unit (74181), scratch pad memory (8225) and I/O devices (through 8233 multiplexers) may communicate directly. Moreover, microprogrammed instructions from a 1024 bit tri-state FROM (8229) may be put on the bus without need for an interface.

8T09 IN A BUS–ORGANIZED MINICOMPUTER

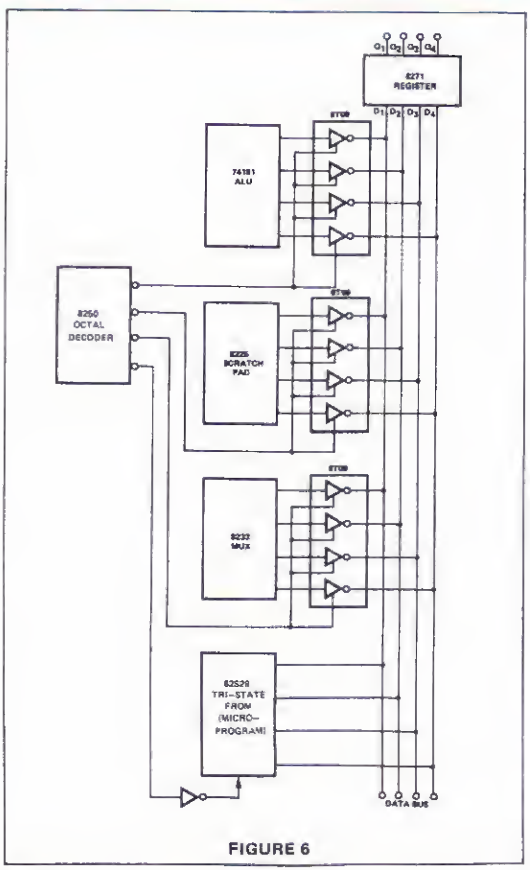


FIGURE 6

8T10 QUAD D–TYPE BUS FLIP–FLOP

A logical extension of the 8T09 bus driver is the 8T10 Bus Flip-Flop. In one integrated circuit a Quad D-Type flip-flop has been combined with tri-state output drivers for use in bus organized systems. As shown in Figure 7, the outputs are disabled, i.e., switched to the high impedance state when one or both of the inputs to the output disable NOR-gate are a logical "1". Having two output disables facilitates X - Y decoding with active low decoders such as the 8250/51/52. Since the outputs will only be enabled with a logical "0", fail-safe operation in bus-organized systems is assured should the disable signal be removed such as is the case when the disable driver card is removed for some reason.

LOGIC DIAGRAM OF THE 8T10

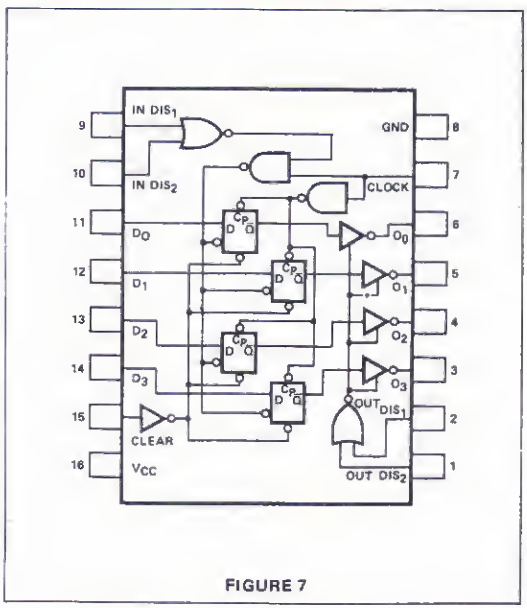


FIGURE 7

All four D-Type flip-flops operate from a common clock, and the data is transferred from the input to the output on the low-to-high transition of the clock pulse. The minimum clock-pulse width is 12ns.

With one or both of the input disable inputs at a logical "1" the flip-flops are in the hold mode and will store the information clocked in prior to the disable signal. The disable lines may change while the clock is high or low without altering the data. A common clear input has also been provided. All flip-flops will be reset upon application of a logical "1" clear pulse at least 15ns wide.

TRUTH TABLE OF THE 8T10

D_n	IN_{DIS}	OUT_{DIS}	OUT_{n+1}
0	0	0	0
1	0	0	1
X	1	0	OUT_n
X	X	1	HIGH Z

FIGURE 8

The "1" level output current from the 8T10 tri-state outputs is the same as the 8T09, thus by the same argument , an 8T10 output can drive 129 8T10s or 8T09s in the high-Z state as well as a standard 8800 or 7400 gate (Ref. Figure 4). The 8T10 outputs have 32mA current sink capability at 0.4V, meaning that up to 20 standard loads can be driven. Therefore, like the 8T09, the 8T10 can be used in a variety of applications where high current sink capability is required. To guarantee trouble-free systems performance, all data and control inputs of the 8T10 are diode clamped to discriminate against negative noise and ringing.

APPLICATIONS OF THE 8T10 QUAD D–TYPE BUS FLIP–FLOP

The buffered tri-state outputs of the 8T10 allow the device to be used directly with other 8T10s in high speed bus-organized systems without the need for interface gates or pull-up resistors. Whenever tri-state bus interfaces without storage are desired, the 8T09 may of course be used. The 8T09 bus driver has the same output characteristics as the 8T10 and with slightly higher current sink capability.

MULTIPLEXING OF DATA IN BUS–ORGANIZED SYSTEMS

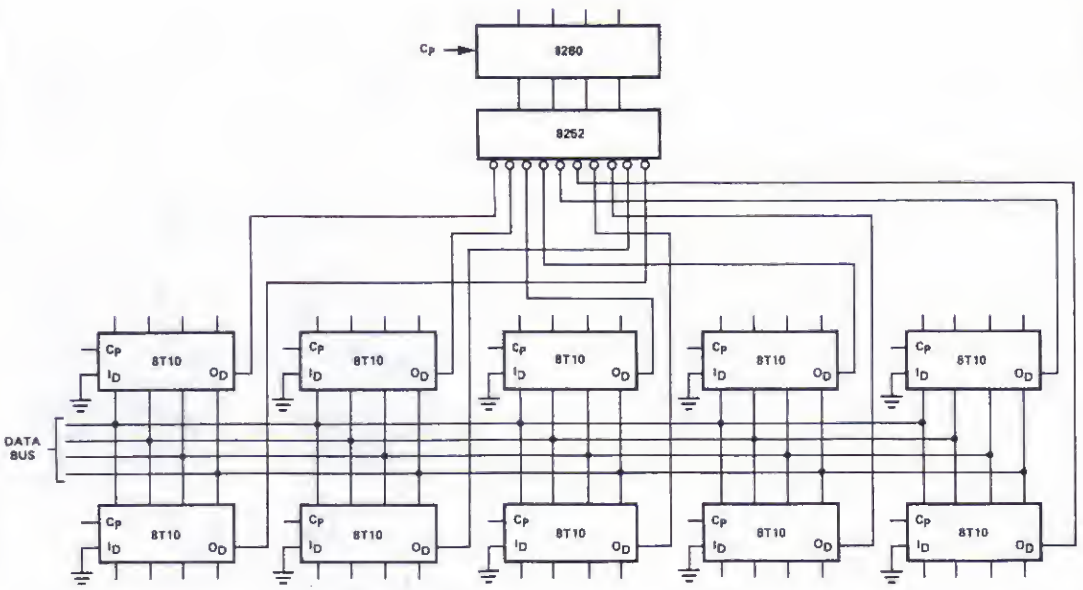


FIGURE 9

Multiplexing of data in bus-organized systems is rather simple, as illustrated in Figure 9. Each 8T10 provides data storage and is selected onto the bus by a logical "0" on both output disable lines. By means of an 8252 one-out-of-ten decoder and an 8280 counter, any one of the 10 bus flip-flop devices can be selected. Should another section of the bus be busy, the 8252 may be blanked, which disables all ten 8T10 devices shown.

As mentioned previously, as many as 129 other 8T10's, as well as a standard TTL receiving gate may be driven by an enabled 8T10. To facilitate output decoding, each 8T10 has a 2-input NOR-gate for the output disable function. As long as either NOR-gate input is high, the 8T10's outputs will be disabled and in the high-Z state. Figure 10 shows how two 8250 one-out-of-ten decoders are used in an X - Y matrix that can select one-out-of-64 8T10s onto the data bus.

X–Y MATRIX FOR SELECTION OF 8T10 BUS FLIP–FLOPS

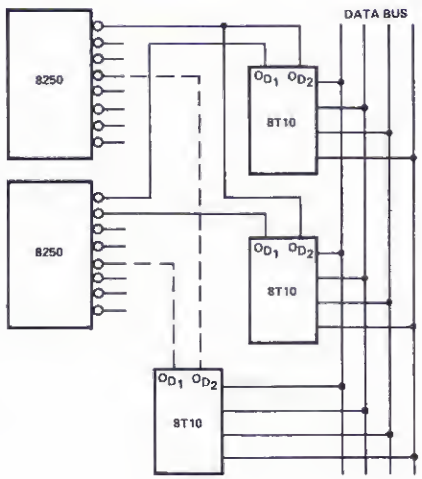


FIGURE 10

Multiplexing of displays is greatly simplified and hardware is significantly reduced when using the 8T10 Quad D-Type Bus Flip-Flop. Figure 11 shows that one decoder driver such as the 8T01 NIXIE decoder/driver or the 8T04/5/6 seven-segment decoder/driver may be time-shared among several displays. If the display is large enough, the digit select drivers and decoding circuitry will cost much less than individual decoder drivers. In addition, strobing displays will result in a net power savings.

MULTIPLEXING OF DISPLAYS USING THE 8T10

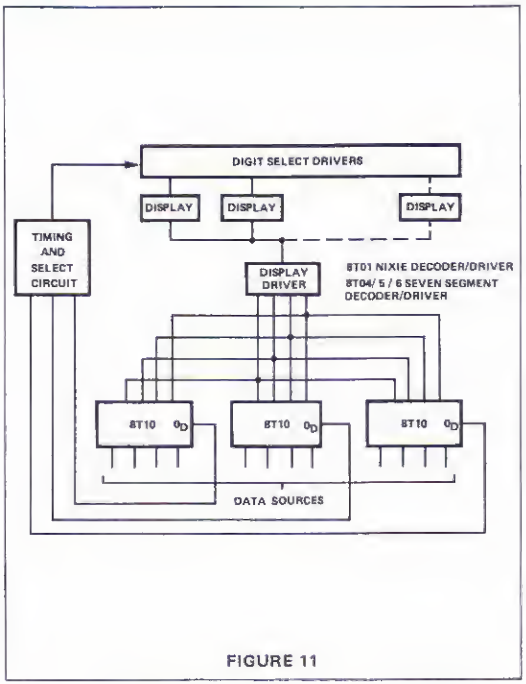


FIGURE 11

The 8T10 may also be configured into a bus-organized register file that can be used in a variety of applications requiring a scratch pad memory. Figure 12 shows such an application. Simultaneous read and write are possible and the memory is easily expanded in word length. Input and output decoding of the 8T10 is simplified because of its NOR-gate input and output disable lines.

SYSTEMS CONSIDERATIONS

The 8T09 and 8T10 bus devices are easy to use but caution should be exercised in systems design with tri-state devices. Because of their high output current capability the 8T09 and the 8T10 should be adequately decoupled just as other TTL drivers, placing a 0.01 to 0.1uf high frequency capacitor as close as possible to the package.

In a system only one tri-state bus device per common bus is allowed to be enabled at a time. It should be realized, however, that in a practical system, control signals may be skewed, creating a slight overlap of the disable signals. Thus it is possible for a transient condition to occur in which two output stages are turned on simultaneously with opposite logic levels. In general, these conditions should be avoided although narrow overlaps of control signals with low duty cycles may not damage any bus drivers and adequate decoupling will handle the surge current demand.

4X4 BUS–ORGANIZED REGISTER FILE

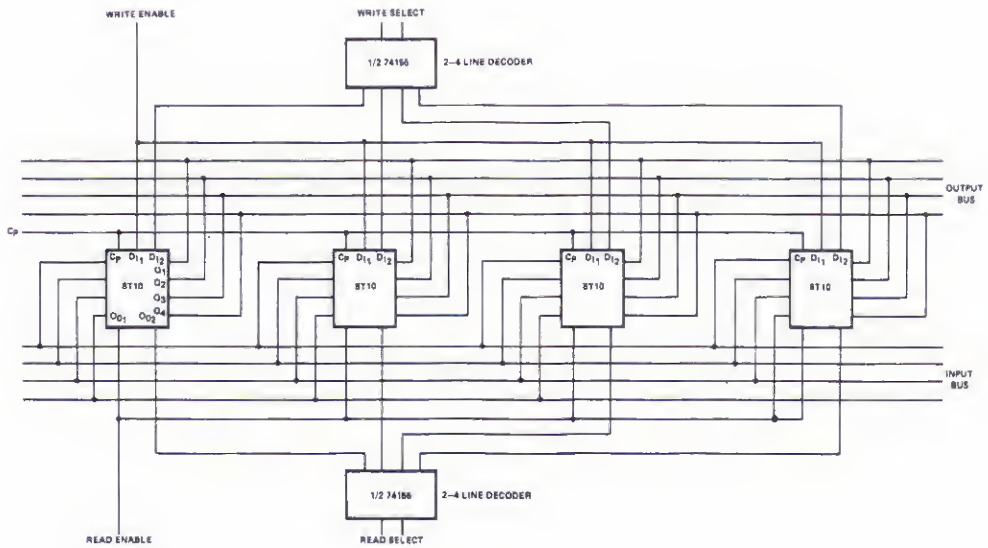


FIGURE 12

8T13 DUAL LINE DRIVER

The Signetics 8T13 is primarily intended for driving low impedance transmission lines such as coaxial cable, twisted pair or ribbon conductors. Both input and output are TTL compatible and the device is operated from a single 5 volt power supply.

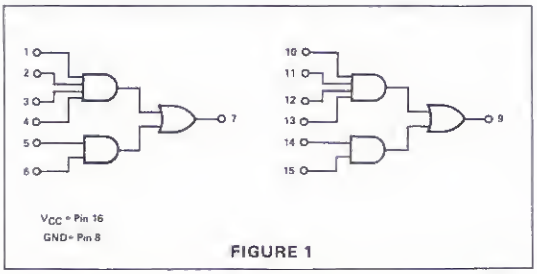


FIGURE 1

LOGIC

The 8T13 contains two AND-OR circuits with one 4-input and one 2-input AND gate for each driver as shown in Figure 1. Unused inputs should be connected to driven inputs where possible to increase circuit speed and to minimize noise coupling into the device.

CIRCUIT DESCRIPTION

The electrical schematic for one of the drivers is shown in Figure 2. The output of the driver is a low impedance emitter follower with built-in short circuit protection. Referring to the circuit, it can be seen that transistor Q_8 will turn on once the output has dropped below approximately two diode drops. Base drive will then be diverted from Q_9 and the output transistor will turn off. Typical output voltage versus current characteristics are shown in Figure 3 over the full temperature range (-55°C to +125°C).

1/2 8T13 LINE DRIVER

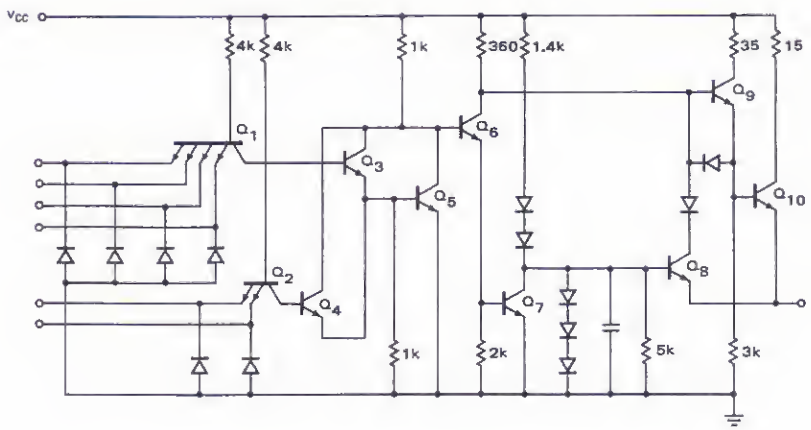


FIGURE 2

The output impedance of the emitter follower output stage during the logic "0" to logic "1" transition is approximately 15 ohms. This low impedance combined with the inherent drive capability of the 8T13 results in an excellent device for driving heavy capacitive loads. Figure 4 shows the typical rise time versus load capacitance for the 8T13 with a 50 ohm pull-down resistor. The output fall time will be governed by the equation: T_f=2.2 RC.

Parallel operation of the 8T13 for additional drive capability can be accomplished. The function obtained is then the logic OR of each output tied to the common bus.

TYPICAL OUTPUT CURRENT VS. OUTPUT VOLTAGE

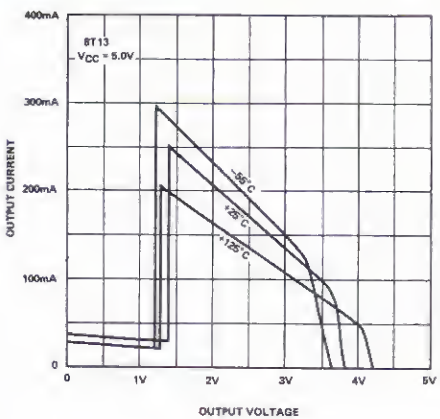


FIGURE 3

TYPICAL RISE TIME VS. LOAD CAPACITANCE

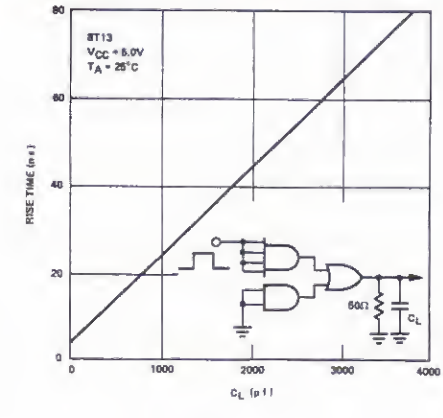


FIGURE 4

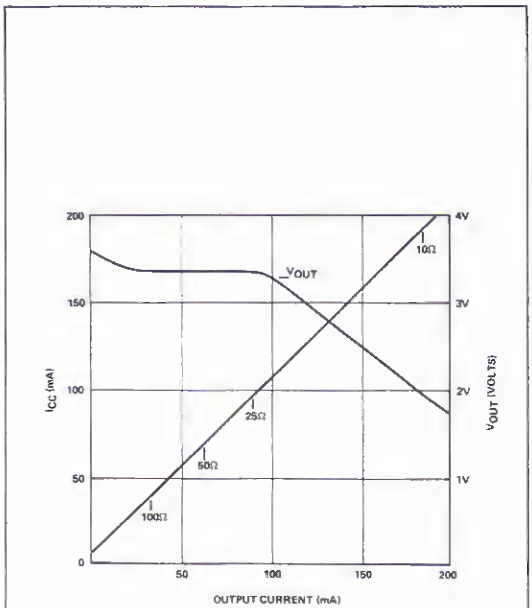


FIGURE 5

POWER DISSIPATION

Typical power supply current and output voltage as a function of load current is shown in Figure 5. For convenience corresponding values of load resistance are also shown. This graph is useful in calculating the total power dissipated by both line drivers in a single package.

Depending upon the output state, the power dissipation of each driver is:

(Logic '1') $P_{diss} = [(V_{CC} - V_{out}) \times I_{out}] + 50mW$

(Logic '0') $P_{diss} = 140mW$

For example, if both drivers in a package are connected to 50 ohm lines but one is turned off (logic '0' state), the total power dissipation would be:

P_{diss} = P_{diss} ('1' state) + P_{diss} ('0' state)

= [(5V − 3.3V) X 65mA] + 190mW

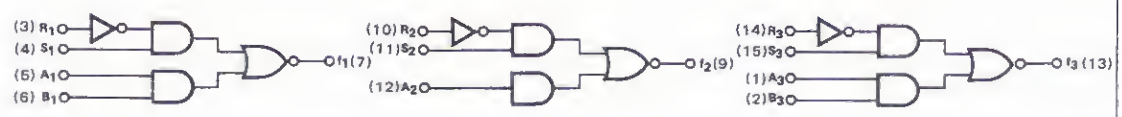
= 300mW

8T14 LINE RECEIVER

The 8T14 was designed to be used at the receiving end of a transmission line for reshaping digital pulses. The device has a built-in hysteresis of 0.5 volt (typical) to discriminate against line reflections and noise. The line receiver is also TTL compatible and operates from a single 5 volt power supply.

LOGIC

The 8T14 contains three line receivers, each of which can be strobed independently. Additional logic is included to allow the output to be forced to a logic "0" by external control signals. (Refer to Figure 6 for complete logic diagram.)



V_{CC} = Pin 16
GND = Pin 8

FIGURE 6

CIRCUIT DESCRIPTION

The receiver input of the 8T14 is basically a differential amplifier with a constant current source replacing the common emitter resistor (see Figure 7). The input impendance is therefore very large, being typically 30 – 50 kilohms. Loading effects are then minimal, an important factor when several receivers are used on the same transmission line.

The output of each line receiver is similar to that used in high speed TTL logic gates. Output rise time is reduced with the low impedance Darlington-type pull-up structure. Typical source and sink current capability over the full temperature range are shown in Figures 8 and 9.

1/3 8T14 LINE RECEIVER

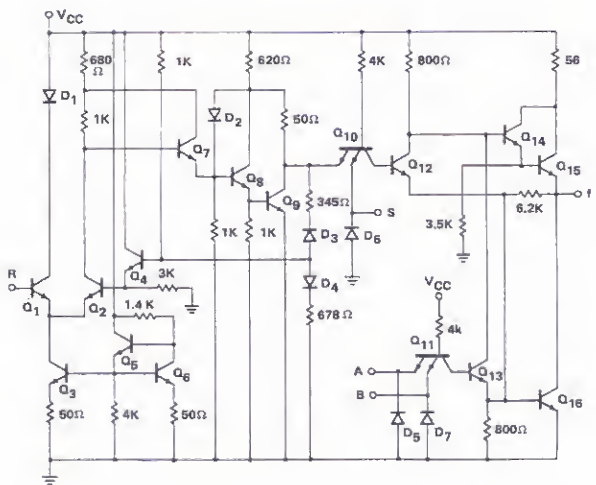


FIGURE 7

HYSTERESIS

The 8T14 exhibits typically 0.5 volt hysteresis as shown in Figure 10. Using the values of upper and lower threshold voltages as indicated, we can calculate the noise immunity for both logic one and zero levels. These calculations assume that the device is being driven with a logic swing of 0.4 to 2.8 volts.

Logic "1" Noise Immunity (N_1)

$$N_1 = V_1 - V_{UT} = 2.8V - 1.35V$$

$$N_1 = 1.45V$$

Logic "0" Noise Immunity (N_0)

$$N_0 = V_{LT} - V_0 = 1.85V - 0.4V$$

$$N_0 = 1.45V$$

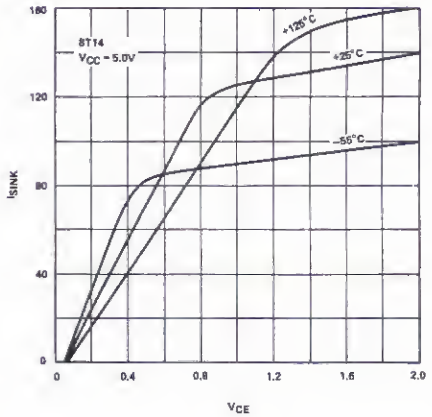


FIGURE 9

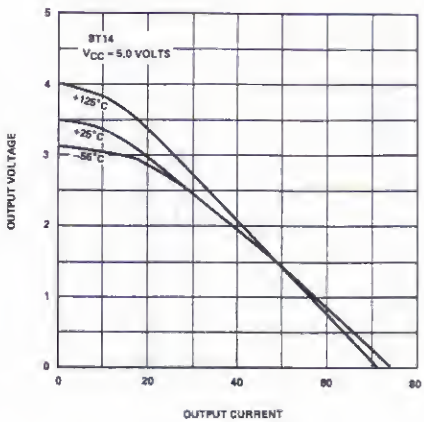


FIGURE 8

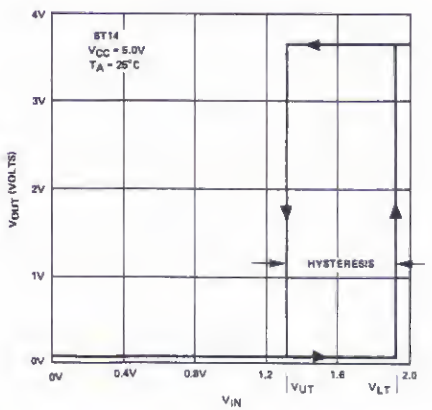
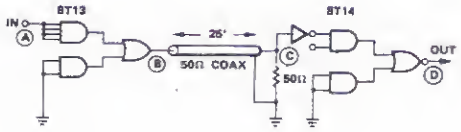


FIGURE 10

APPLICATIONS



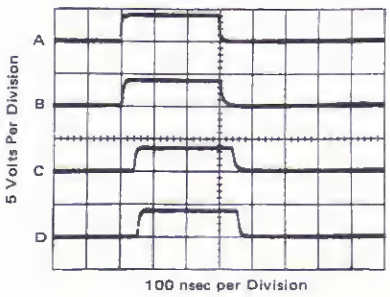
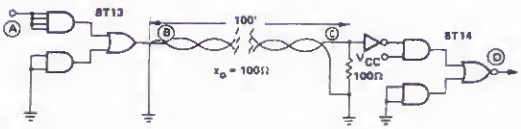


FIGURE 11

TWISTED PAIR



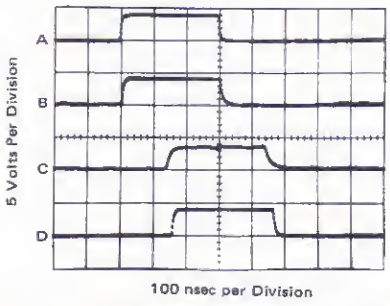
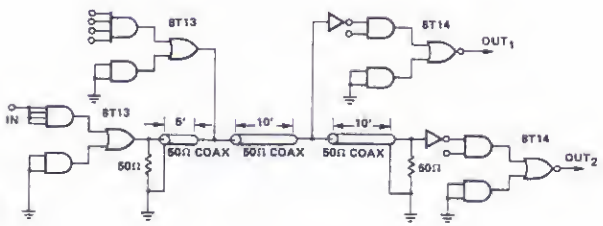


FIGURE 12

PARTY–LINE APPLICATION



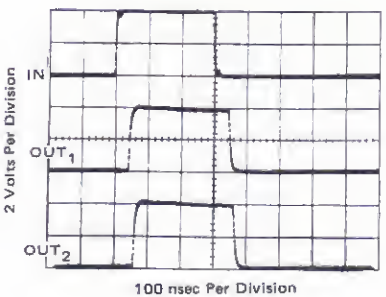


FIGURE 13

GENERAL EQUATIONS FOR PARTY LINE APPLICATIONS

When multiple drivers and receivers are tied onto a common bus in a party-line applications, it can be easily ascertained if the required current is within the drive capability of an 8T13 driver. Figure 14 shows a generalized example.

The equations given below will show if a driver can handle the load.

$$I_{OUT(1)}\Big|_{V_{OUT(1)} = 2.4V} \geq I_{TERMINATION + LOAD}$$

Where: $I_{LOAD} = (m-1)\, I_{LEAK(1)} + n I_{IN(1)}$
m = number of drivers
n = number of receivers

and $[n I_{IN(0)} + m I_{OUT(0)}]\, R_{TERM.} \leq 0.4V$
where $I_{OUT(0)}$ = LEAKAGE CURRENT

Example:

Can the 8T13 and 8T14 be used in a bus-organized system where 15 drivers and 20 receivers are tied onto one common bus. The bus is 100Ω coax-cable, terminated at both ends.

Given: m = 15
n = 20
$R_{TERM} = 100\Omega$

$$I_{OUT(1)}\Big|_{\text{at } V_{OUT(1)} = 2.4V} = 75mA$$

$I_{OUT(1)LEAK} = 80\mu A$ (from data sheets if $V_{CC} = 0$ for disabled 8T13)

$I_{IN(1)} = 0.17mA$

$I_{LOAD} = (14)\,(0.08mA) + 20(0.17)mA$
$= 1.46mA$

$$I_{TERM} = \frac{2.4V}{50\Omega} = 48mA$$

$I_{TERM} + I_{LOAD} \leq I_{OUT(1)}$
$49.46mA < 75mA$

$I_{IN(0)} = 0$

$$I_{OUT(0)}\Big|_{\text{at } V_{OUT(0)} = 0.4V} = 200\mu A \text{ (from data sheets)}$$

$[15(200\mu A)]\ 100\Omega \leq 0.4V,$
$.03V < 4V$

The answers show that the above application is well within the 8T13 drive capability.

PARTY–LINE APPLICATION

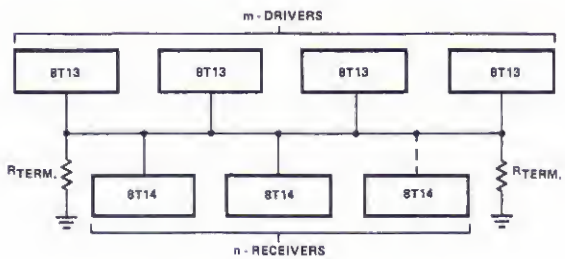


FIGURE 14

DIGITAL 8000 SERIES TTL/MSI

8T14 AS A SCHMITT TRIGGER

The Signetics 8T14 Triple Line Receiver was designed primarily for data communication systems where digital information must be recovered with a high degree of accuracy, even in the presence of noise.

However, as shown in Figure 1, the Line Receiver inputs having hysteresis together with the additional logic functions available make the 8T14 a powerful multipurpose device. For a thorough discussion of the 8T14's electrical characteristics please refer to the applications memo covering the 8T13 Line Driver and the 8T14 Line Receiver.

8T14 TRIPLE LINE RECEIVER

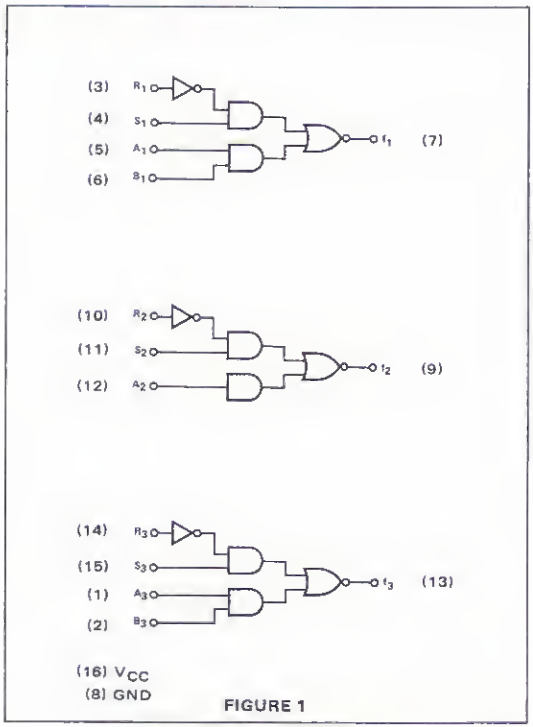


FIGURE 1

The built-in hysteresis of the line receiver makes it ideal for use as a Schmitt trigger. For example, signals with slow transition times can be reshaped with the 8T14 to be suitable for use with high speed logic as illustrated in Figure 2. By taking advantage of the additional logic inputs, the circuit could also be used as a controlled Schmitt trigger. Typical rise and fall times of the 8T14 are less than 10ns with minimum capacitive loading.

SCHMITT TRIGGER

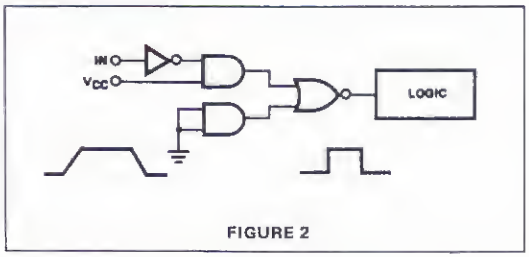


FIGURE 2

A special case of a Schmitt trigger application is sine-to-square wave conversion. The circuit shown in Figure 3 was found to be a very effective and convenient means of driving the frequency divider chain of a digital clock.

SINE–TO–SQUARE WAVE CONVERTER

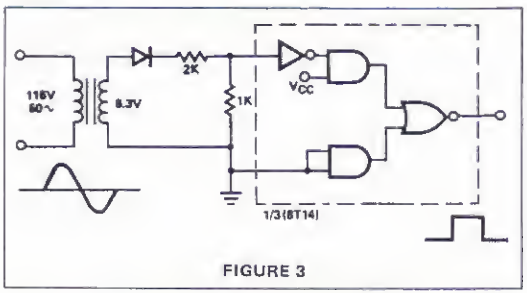


FIGURE 3

The Schmitt trigger characteristics of the 8T14 can also be used to advantage in a monostable multivibrator, or one-shot as illustrated in Figure 4.

ONE–SHOT

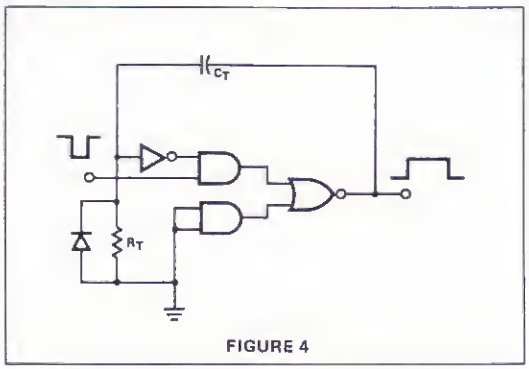


FIGURE 4

With resistor values less than 5K, the output pulse width is $\cong 0.9\ R_T\ C_T$. Above 5K, R_T begins to approach the input impedance of the 8T14 and the equation is no longer valid. Figure 5 is a graph of pulse width versus timing capacitance for the circut shown in Figure 4.

OUTPUT PULSE WIDTH VS. TIMING CAPACITANCE

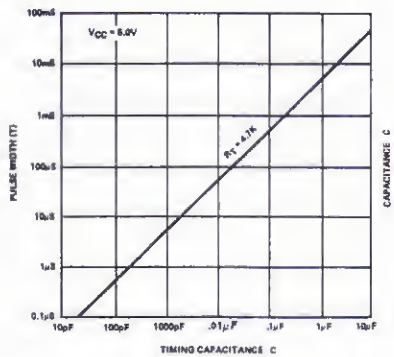


FIGURE 5

To increase pulse width, capacitor multiplication with PNP transistors can be used as indicated in Figure 6. The effective capacitance becomes approximately $\beta X C_T$. Using a 10KΩ resistor and 47µF capacitor, pulse widths of 50 seconds were obtained.

ONE SHOT WITH BETA MULTIPLIER

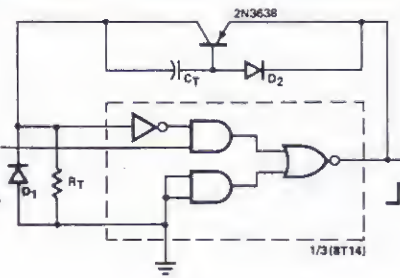


FIGURE 6

Without diode D_2, capacitor C_T does not discharge rapidly below 1.5 volts and does not allow the one-shot to retrigger. The diode provides a low impedance path back through the saturated output transistor and significantly increases the duty cycle.

When the input pulse width is larger than the required output pulse, the input can be differentiated by a small series capacitor. Using a 22pF capacitor, output pulse widths as short as 50ns can be obtained.

By providing an additional stage of inversion, the 8T14 can be used as a gated oscillator as shown in Figure 7. Using one of the remaining receivers in the package for the inverter the circuit was found to oscillate at:

$$f_{osc} \cong \frac{1}{0.7\ RC}$$

OSCILLATOR

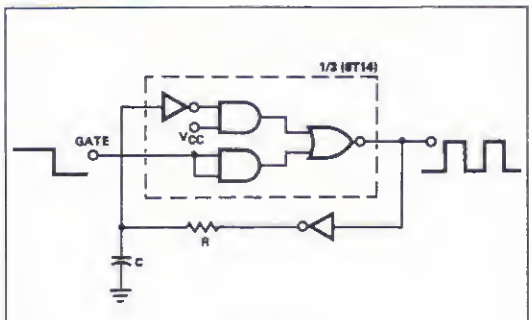


FIGURE 7

Figure 8 is a graph of oscillator frequency versus capacitance for two values of resistance. With the addition of a Hex Inverter such as Signetics 8890 three separate oscillators with buffered outputs could be built with only two packages.

OSCILLATOR FREQUENCY VS. CAPACITANCE

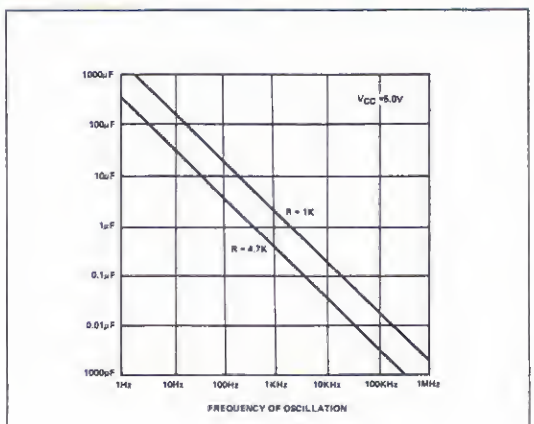


FIGURE 8

8T15 DUAL LINE DRIVER

The 8T15 Dual Communications Line Driver provides line Driving capability for data transmission between data communication and terminal equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24.

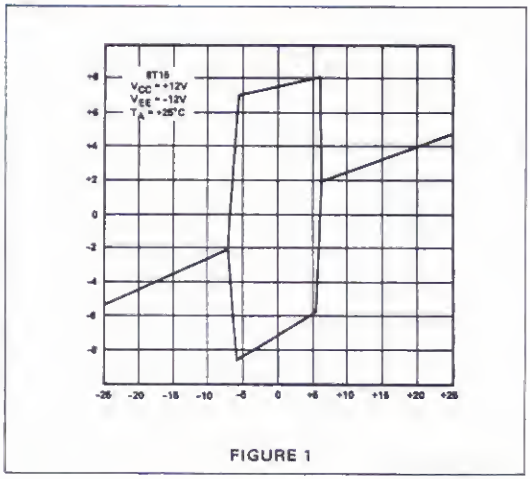
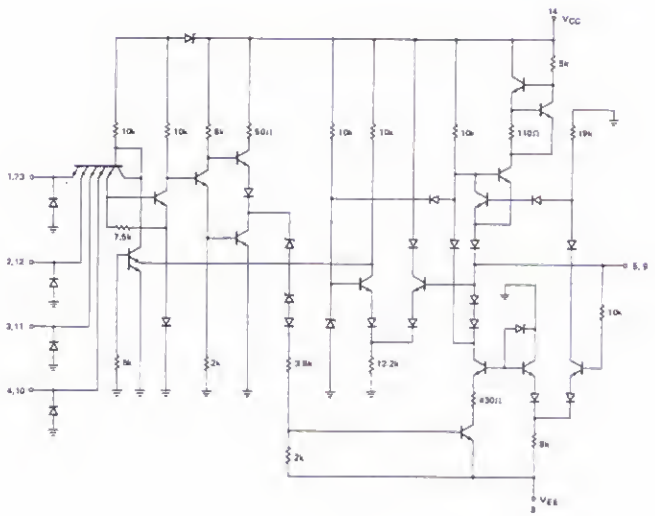


FIGURE 1

CIRCUIT DESCRIPTION

The 8T15 requires a dual power supply with nominal voltages of +12 and -12V volts. The output circuit features current limiting and can be shorted to ±25 volts without damage. Figure 1 shows the typical output characteristics for all possible operating conditions. Above approximately ±7 volts, the effects of current limiting cause the output impedance to increase to ⩾ 5 kilohms.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM

As shown in Figure 2, each driver performs the logic NAND function of four inputs and will accept standard TTL logic levels. The output is buffered to drive interface lines with nominal data levels of +6V and -6V. Output slew rate may be adjusted by attaching and external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as ±25 volts.

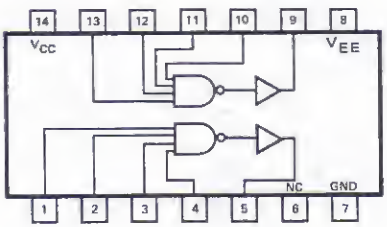


FIGURE 2

Figure 3 shows the typical transfer curve of the Line Driver at +25°C. Except for the output voltage swing of ±6 volts, the curve is essentially identical to that for a standard TTL gate.

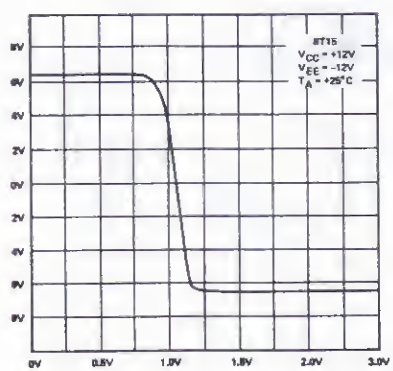
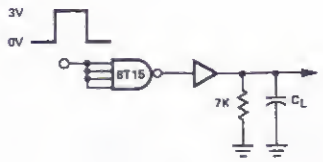
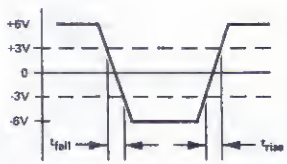


FIGURE 3

In systems where crosstalk is likely to occur between transmission lines, the rise and fall time of the data pulse can be tailored by connecting a capacitor from the output of the 8T15 to ground. Since the output current in either a "1" or "0" state is supplied through a constant current source, the transition time is a linear function of the load capacitance as shown in Figure 4. The circuit below was used to measure the transition time as C_L was varied between 0 and 1μf.





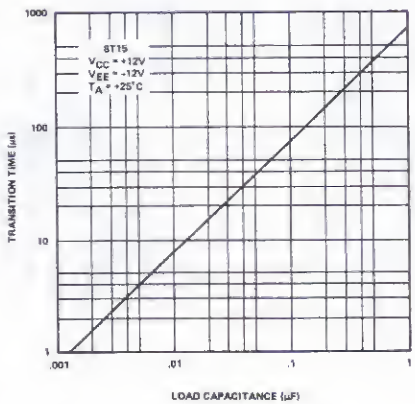


FIGURE 4

Table 1 provides a summary of the specific requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24 for Communications Line Drivers along with the electrical characteristics of the Signetics 8T15.

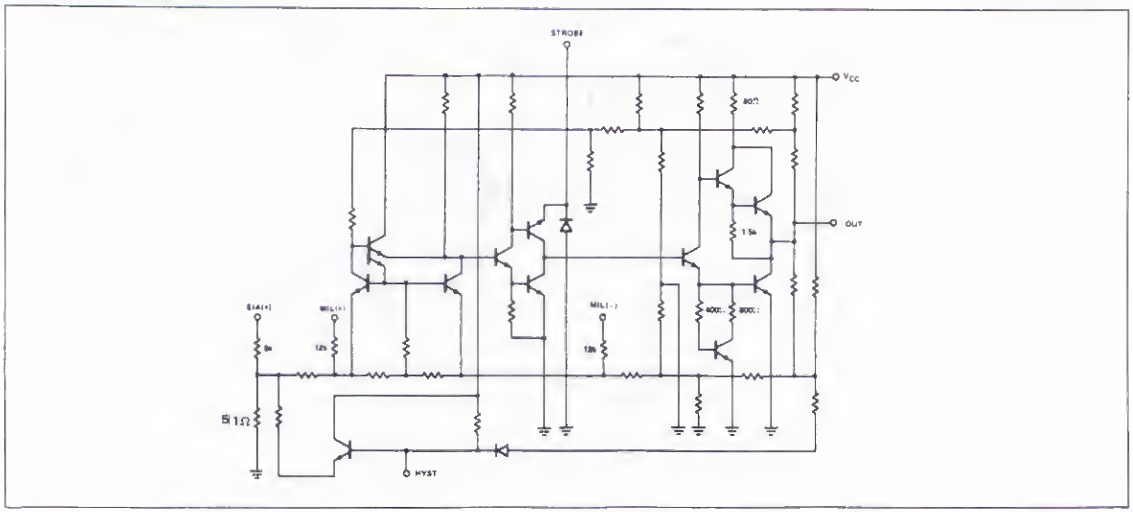
TABLE 1

SPECIFICATION	EIA RS-232B, C	MIL-STD-188B	CCITT V24	SIGNETICS 8T15	
				(LIMIT)	(TYPICAL)
Output Voltage "1"	-5Vmin.(R_L = 3000Ω) -15Vmax.(R_L = 7000Ω)	-6 ±1V	-5Vmin. (R_L = 3000Ω) -15Vmax.(R_L = 7000Ω)	-5Vmin. -7Vmax at 4mA	-6V at 4mA
Output Voltage "0"	+5Vmin.(R_L = 3000Ω) +15Vmax.(R_L = 7000Ω)	+6 ±1V	+5Vmin.(R_L = 3000Ω) +15Vmax.(R_L = 7000Ω)	+5Vmin., 7Vmax. at -4mA	+6V at -4mA
Source Impedance (power on)	Not Specified	100Ω max. for I < 10mA	Not Specified		95Ω for ±(0.5 to 4.0 mA)
Source Impedance (power off)	300min. at ±2V	N/A	300min. at ±2V	300min. at ±2V	2.5MΩ
Max. Short Circuit Current	±500mA max. (to ±25V)	100mA max. (to ground)	±500mA max. (to ±25V)	±25mA max. (to ±25V)	±5mA (to ±25V)
Wave Shape (rise and fall time)	±4% of pulse Interval (max.)	±5% of pulse Interval (min.)		4μs-3000pF 200ns-20pF	2μs-3000pF 25ns-20pF
Bit Rate	0-20KHz	4KHz normal	20KHz max.		3MHz
Open Circuit Drive	±25V max.	±6V ±1V		±6V ±1V	±6V
Signal Characteristics	1ms max. transition		1ms max. transition		2μs with C_L = 3000pF
	30V/μs max. dV/dt		30V/μs max. dV/dt		20V/μs with C_L = 500pF

8T16 DUAL LINE RECEIVER

The 8T16 was designed for use as either an EIA or MIL Line Receiver for interfacing with data communication and terminal equipment. Two MIL inputs (MIL+ and MIL-) and one EIA input are provided on each receiver. Each output can be strobed independently and a hysteresis control is provided for shifting the threshold voltages for use in the EIA Fail-Safe mode. The 8T16 operates from a single +5 volt power supply.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM

The strobe input operates as follows:

a) A "0" on the strobe input allows data transfer.

b) A "1" on the strobe input holds the output high. (Throughout this Application Memo the negative logic convention is used, i.e., a logic "1" refers to a relative low voltage and a logic "0" to a relative high voltage.)

It is important to note that when using the EIA input both MIL inputs must be grounded. The EIA input can be left open when unused.

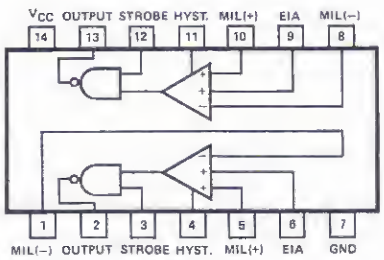


FIGURE 5

The 8T16 Line Receiver accepts single-ended (MIL and EIA) or differential (MIL) signals and converts them to standard TTL logic levels. The circuit employs hysteresis to obtain the high noise margins required when the receivers must operate in noisy environments. The upper threshold voltage can be shifted above 0 volts by grounding the hysteresis control line. This allows the receiver to be used in the EIA Fail-Safe mode. Figures 6 through 8 illustrate typical hysteresis characteristics for all three operating conditions.

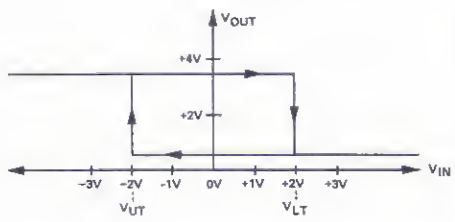


FIGURE 6

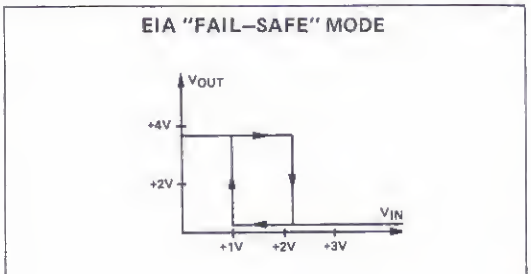


FIGURE 7

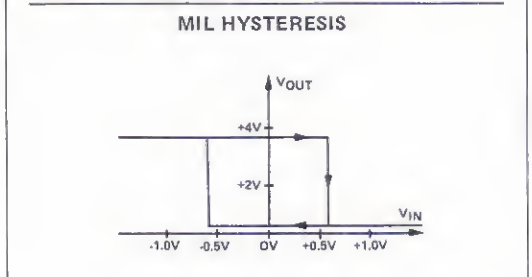


FIGURE 8

Figure 9 is a curve of noise immunity versus pulse width assuming the receiver is being driven with a signal whose amplitude is normally ±6 volts. The noise rejection capability of the 8T16 provides approximately 15 volts of noise immunity to pulses ⩾ 30ns.

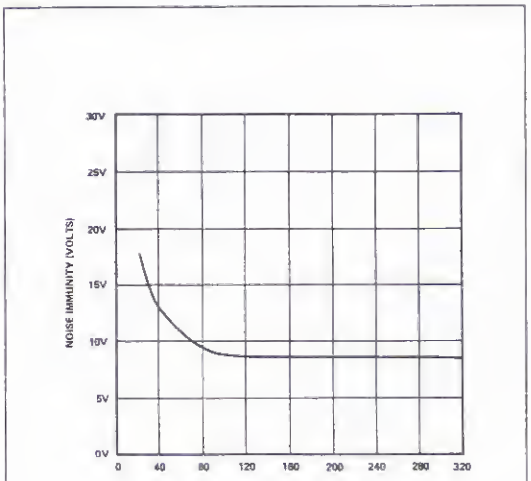


FIGURE 9

The 8T16 output is TTL compatible as shown in Figures 10 and 11 where the typical source and sink current capability are illustrated for the 0°C to +75°C temperature range.

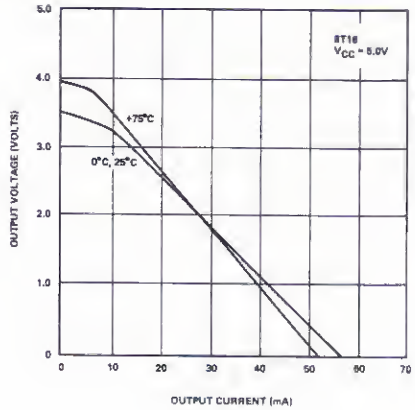


FIGURE 10

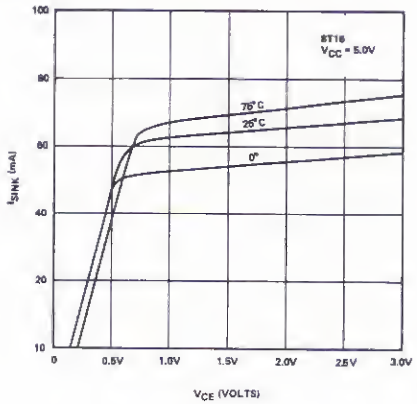


FIGURE 11

TABLE 2

SPECIFICATION	EIA RS-232B, C	MIL-STD 188B	CCITT V24	SIGNETICS 8T16 LIMIT	SIGNETICS 8T16 TYPICAL
Input Thresholds (V) Max.	+3V, -3V	Not Specified	+3V, -3V	+3V, -3V (1) +0.9V, -0.9V (2) +3V, +0.3V (3)	+2V, -2V (1) +0.6V, -0.6V (2) +2.1V, +1V (3)
Input Thresholds (I) Max.	Not Specified	0.1mA max.	Not Specified	.1mA max.	0.050mA
Input Resistance	3K min., 7K max.	6K min.	3KΩ min., 7K max.	3K min. 7K max. (EIA) 7.5K min. (MIL)	5K (EIA) 12K (MIL)
Hysteresis	Not Specified	Not Specified	Not Specified	2.4V min. (EIA) 0.7V min (MIL)	4V (EIA) 1.2V (MIL)
Max. Input Voltage	±25V (min.)	Not Specified	±25V (min.)	±25V (EIA AND MIL)	
V_{CC}	Not Specified	Not Specified	Not Specified	+7V	+5V ±5%

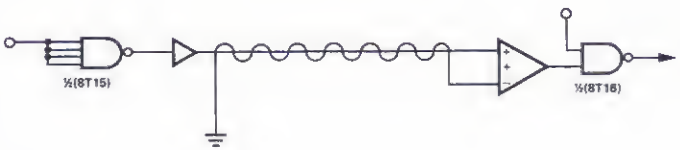
NOTES: 1) EIA Input, Hysteresis terminal open 2) MIL Input 3) EIA Input, Hysteresis terminal grounded

APPLICATIONS

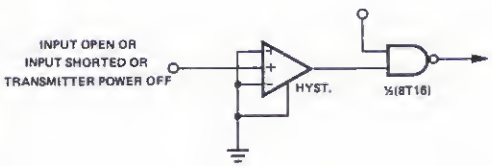
HIGH DIFFERENTIAL NOISE IMMUNITY

APPLICATIONS (Cont'd)

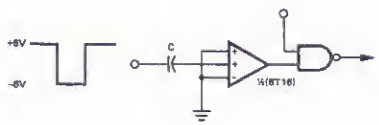
HIGH COMMON MODE NOISE IMMUNITY



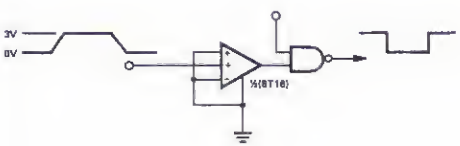
EIA FAIL-SAFE OPERATION



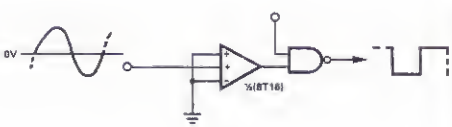
AC COUPLED OPERATION



SCHMITT TRIGGER



SINE-TO SQUARE WAVE CONVERTER



DIGITAL 8000 SERIES TTL/MSI

8T20 BI-DIRECTIONAL ONE-SHOT

INTRODUCTION

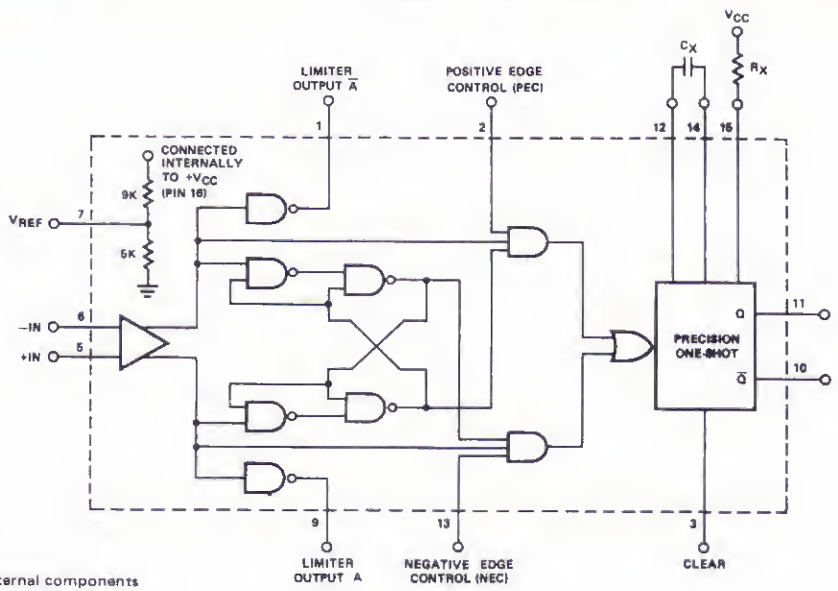
The 8T20 bidirectional one-shot is a functional building block that combines in one monolithic IC a high speed comparator, digital control circuitry and a precision one-shot. As shown in Figure I, the device may be driven with differential or single ended signals; and for convenience, a resistive divider on the chip will provide a TTL reference voltage. The comparator outputs are limited and made accessible through buffers for additional design flexibility. The output of the limiter feeds digital control circuitry which generates a trigger pulse each time the input makes a positive or negative transition across the reference level. By means of a positive edge control (PEC) as well as a negative edge control (NEC) the precision one-shot may be conditioned to trigger on the positive edge and/or the negative edge. The one-shot is non-retriggerable and its period may be adjusted by means of external timing components. An active-high clear input inhibits the operation of the 8T20 and terminates already initiated timing cycles as well.

The 8T20 will simplify system design and significantly reduce parts count in applications where signal conditioning and timing pulse generation is required. Input and output waveforms are shown in Figure 2 for easy reference. The usefulness of the 8T20 in magnetic recording of digital data and digital data transmission will be discussed among other applications.

DEVICE DESCRIPTION

The input stage of the 8T20 is a differential pair with high input sensitivity and a differential input impedance of approximately 2kΩ. The differential threshold voltage (V_T) is ±4mV maximum and is defined as the maximum offset voltage from the reference level of one input beyond which the one-shot is guaranteed to fire. Thus, by observing the first accessible digital output of the one-shot which is pin 12 (one of the C_X terminals), the DC input voltage (V_T) required to make the one-shot trigger can be ascertained.

LOGIC DIAGRAM



NOTES:
1. R_X,C_X external components
2. Pulsewidth $t_W = R_X C_X \text{Log}_e 2$
3. 4 V_{EE} = −5V ± 5%
4. 8 GND
5. 16 V_{CC} = +5V ± 5%

FIGURE 1

Common mode signals will not cause false triggering of the 8T20 as long as they are confined within the dynamic range of the analog inputs which is between -3.2V and +4.2V. Since in many applications TTL compatible signals are available to drive the 8T20, the output of an internal resistive divider can be connected to one of the differential inputs as a TTL threshold reference (approximately 1.6V).

When driving the 8T20 differential inputs with slow edges or with low frequency sine waves, it is possible to get false triggering of the one-shot unless input signals have a slew rate of at least 50mV/μsec.

The differential pair is followed by a level shifter and limiter circuit; but for simplicity, only the block diagram is shown in Figure 1. The comparator has differential outputs which feed the internal digital circuitry and for additional versatility they are also buffered and brought out (pins 1 and 9).

INPUT/OUTPUT WAVEFORMS

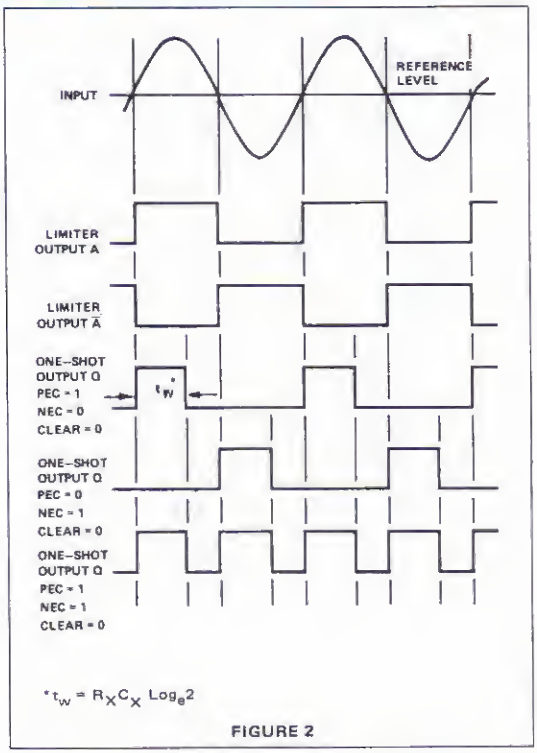


FIGURE 2

The input signal transitions which have been shaped by the limiter output of the comparator are processed by the pulse generating and control circuitry as shown in Figure 3. Input transitions at gates A and B are transformed into trigger pulses and the outputs C and D may be inhibited by means of the PEC and NEC signal. Thus the one-shot that follows the OR-gate E can trigger on either edge or both.

INTERNAL PULSE GENERATING AND CONTROL CIRCUITRY

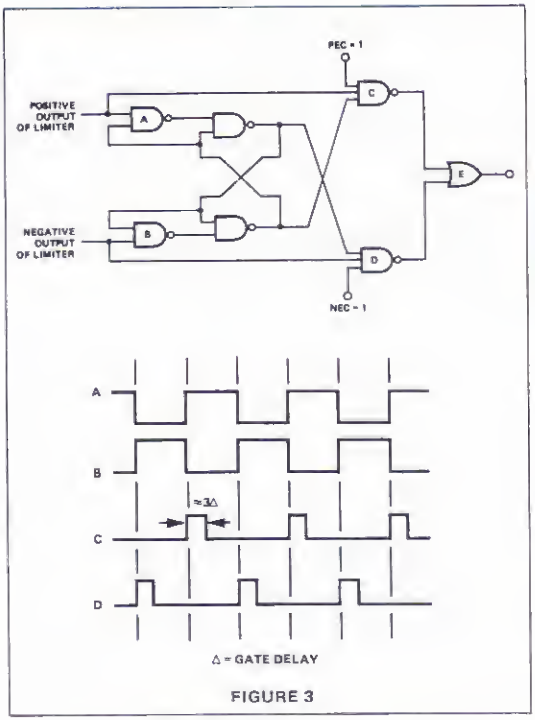


FIGURE 3

A simplified circuit diagram of the 8T20 timing circuit is shown in Figure 4. The design offers extremely accurate output pulse widths that depend essentially only on the accuracy of external timing components. The timing capacitor C_X can be charged rapidly through the emitter follower action of Q_2 permitting duty cycles in excess of 90%.

TIMING CIRCUIT

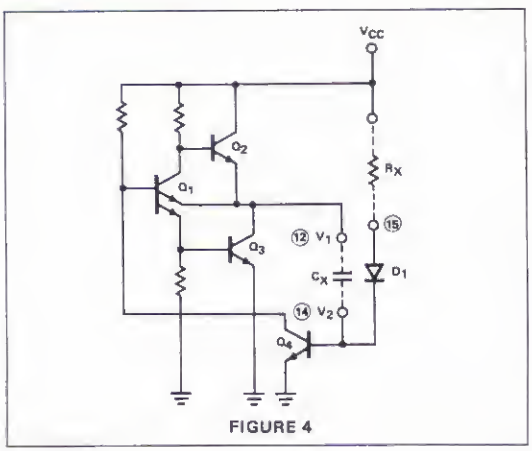


FIGURE 4

In the stable state, the capacitor is charged up to $V_{CC} - V_{BEQ2} - V_{BEQ4}$. When the one-shot is fired, Q_3 will turn on, clamping the capacitor C_X at V_{BEQ3}. As shown in the timing waveform, Figure 5, voltage V_2 drops from V_{BEQ4} to $-V_{CC} + V_{BEQ2} + V_{BEQ3} + V_{BEQ4}$. In this quasi-stable state C_X will charge through the timing resistor R_X towards $V_{CC} - V_{D1}$. When V_{BEQ4} is reached again, the one shot will revert to its stable state, only utilizing the linear part of the charging curve.

TIMING WAVEFORM FOR SIMPLIFIED ONE–SHOT

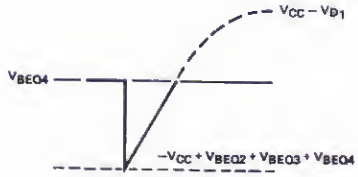


FIGURE 5

The output pulse width (t_W) can thus be calculated by setting $V_2 = V_{BEQ4}$ at $t = t_W$, resulting in:

$$e^{-t_W/R_XC_X} = \frac{-V_{CC} + V_{BEQ4} + V_{D1}}{-2V_{CC} + V_{BEQ2} + V_{BEQ3} + V_{BEQ4} + V_{D1}}$$

By close matching of the forward voltages of the diodes, pulse width (t_W) becomes:

$$t_W = R_XC_X \log_e 2 \doteq 0.69\ R_XC_X$$

Where:

t = sec
R = ohms
C = Farads

Stability over temperature and V_{CC} variations is better than ±1% and typical timing charts are shown in Figures 6 and 7. The timing resistor R_X should be restricted between 2kΩ on the lower end to get reasonable duty cycles and 40kΩ on the high end such that Q4 can still be turned on at low temperatures. C_X should not exceed 1000μF such that safe current levels are maintained in the recovery transistor Q2.

OUTPUT PULSEWIDTH VS. TIMING RESISTOR VALUE

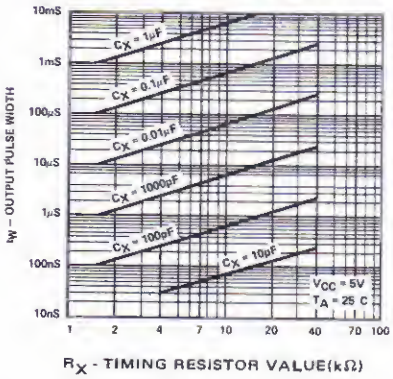


FIGURE 6

OUTPUT PULSEWIDTH VS. TIMING CAPACITOR VALUE

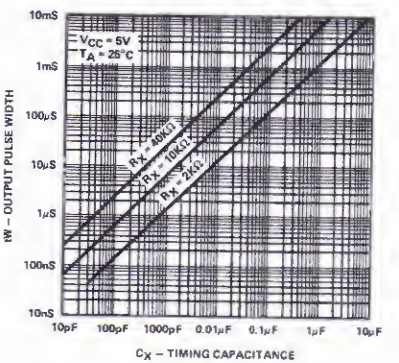


FIGURE 7

EXTENDING THE ONE–SHOT RANGE WITH A BETA–MULTIPLIER CIRCUIT

By adding an external transistor, the pulse width of the one-shot may be extended since very large timing resistors can be used as shown. However, it is more difficult to match V_{BE}'s and PW accuracy suffers slightly. In the connection shown in Figure 8, the internal diode is not utilized and the pulse width is calculated as follows:

$$e^{-t_W/R_XC_X} = \frac{-V_{CC} + V_{BEQ4} + V_{BEQX}}{-2V_{CC} + V_{BEQ2} + V_{BEQ3} + V_{BEQ4} + V_{BEQX}}$$

Thus, it can be seen that pulse width (t_W) will reduce again to

$$t_W = R_XC_X \log_e 2 \doteq 0.69\ R_XC_X$$

if V_{BE} of the external transistor Q_X matches and tracks the internal transistor V_{BE}s. This somewhat surprising result is possible since C_X, connected as shown in Figure 8, will now charge towards V_{CC} instead of $V_{CC}-V_{D1}$ and V_2 is equal to $V_{BEQ4} + V_{BEQX}$ in the stable state of the one-shot.

For transistors with β = 100 timing resistor values up to 3.3MΩ can be used which combined with a 1000μF capacitor will give a pulse width t_W of approximately 35 min.

BETA MULTIPLIER CIRCUIT TO EXTEND PULSEWIDTH

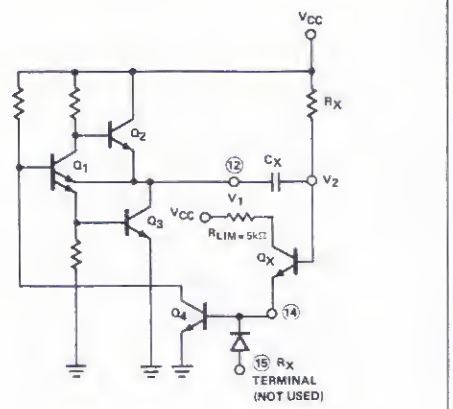


FIGURE 8

PULSE POSITION ERROR

In applications such as frequency doubling and processing of self-clocking digital codes received from magnetic media, it is extremely important to have minimum pulse position variations. As shown in Figure 9, when triggering on a positive transition a time delay Δt_1 is encountered, whereas on a negative transition a time delay Δt_2 is seen. A pulse position error (P.P.E.) can now be defined as P.P.E. = $|\Delta t_1 - \Delta t_2|$. Because of the close matching of components on the 8T20 chip, this error is typically less than 3ns, far superior to discrete implementations of this circuit.

DEFINITION OF PULSE POSITION ERROR

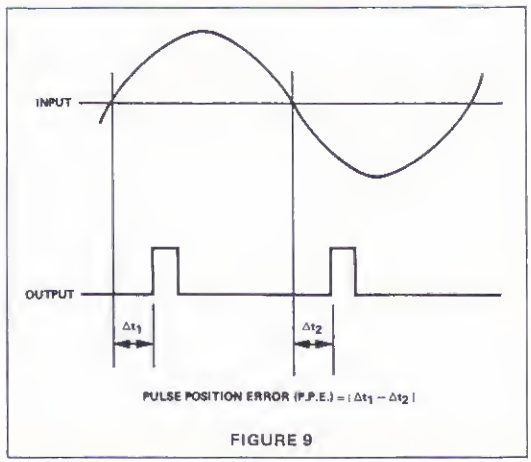


FIGURE 9

APPLICATION OF THE 8T20 IN DISC, DRUM AND TAPE PLAYBACK SYSTEMS

The 8T20 has been specifically designed for use in playback systems when recovering high-speed data from magnetic recording media. Because of the 8T20's inherent capability to double an incoming frequency with a low pulse position error (typ. < 3 ns) the device is particularly suited to process data encoded in self clocking formats such as those depicted in Figure 10. For clarity, these codes are referenced to the original clock.

Both the Manchester code and the double-frequency (diphase) code have at least one transition per bit cell, thus always containing clock information even with long strings of "1"s or "0"s. Manchester coding contains information in the direction of change, whereas double-frequency coding has two transitions per bit cell for a logical "1" and one transition per bit cell for a logical "0".

In recovering data from disc or drum files, several steps must be taken to pre-condition the linear data. The NE592* video amplifier, coupled with the 8T20 bi-directional one-shot, provides all the signal conditioning necessary for phase encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the Gaussian pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV p-p to 3mV p-p for oxide coated disc files and 1 to 20mV p-p for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

*See Signetics-Liner 592 Data Sheet

The classical approach to peak-time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the pre-conditioning described above is shown in Figure 11. Readback data is applied directly to the input of the first 592. This amplifier functions as a wideband AC coupled amplifier with a gain of 100. The NE592 is excellent for this application because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common mode rejection ratio of the amplifier is preserved.

The output of the first stage amplifier is routed to a linear phase shift low pass filter. The filter is a single stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$$L = \frac{2R}{\omega_c} \qquad C = \frac{1}{\omega_c R}$$

Where R = Characteristic impedance (ohms)

ω_c = Cutoff frequency (Radians/sec)

The second 592 is utilized as a low noise differentiator/amplifier stage. The 592 is excellent in this application because it allows differentiation with excellent common mode noise rejection.

The 8T20 input stage will act as a high gain limiter, squaring the pre-amplified and filtered signal. The device's digital pulse generating circuitry will detect positive and negative transitions (zero-crossings) that will trigger the internal one-shot as conditioned by the PEC and NEC control signals. A pulse train will result that contains the original data and clock information. This information is usually put on the read-bus for processing by pulse recognition circuitry to recover the data. It is customary in a high-precision system to use a phase-locked loop system to recover the original clock.

PHASE ENCODED DATA

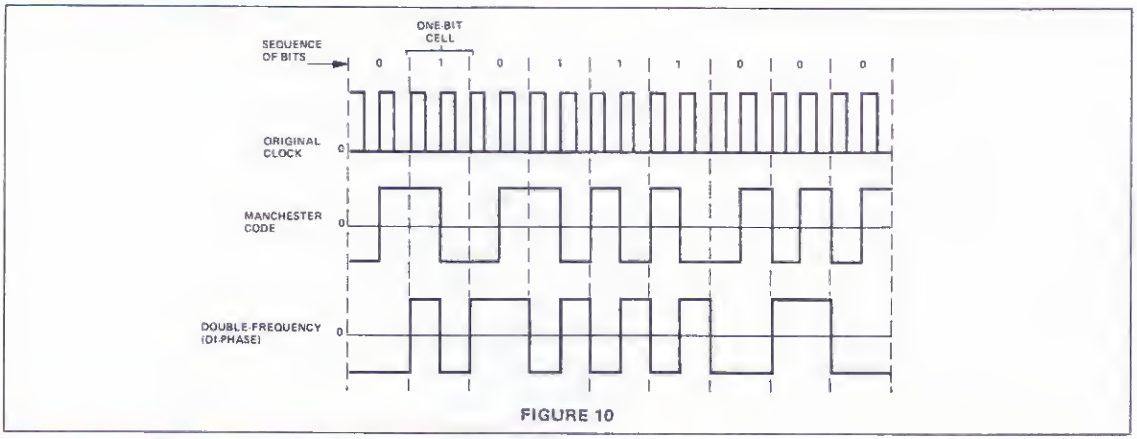


FIGURE 10

5MHz PHASE ENCODED DATA READ CIRCUITRY

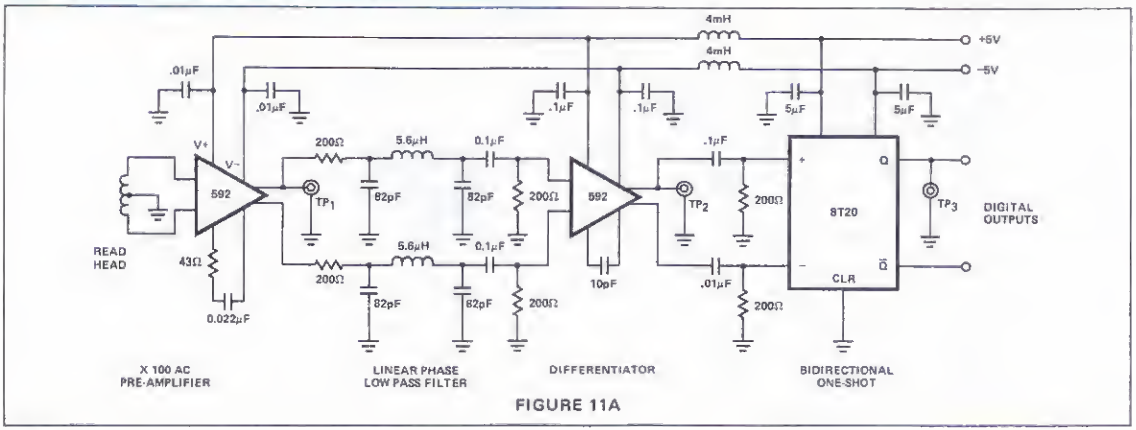
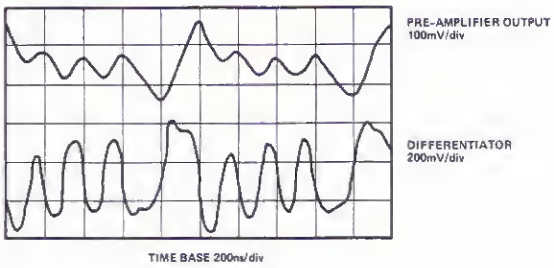
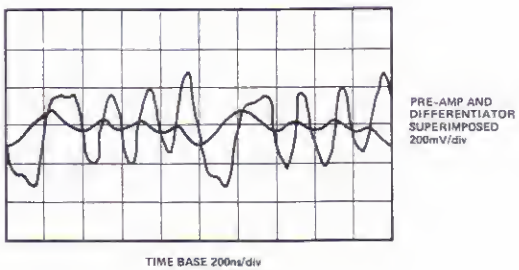


FIGURE 11A

The circuit in figure 11a was tested with an input signal approximately that of a readback signal. The results are shown in Figure 11b.

USING THE NE592 AND 8T20 IN PHASE ENCODED DATA SYSTEMS





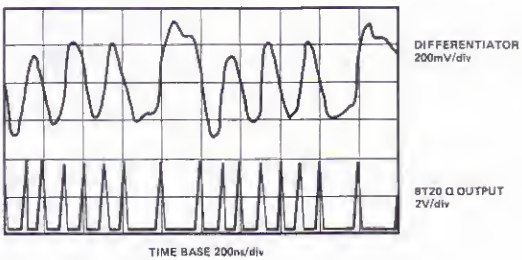


FIGURE 11B

BINARY TO DI–PHASE TRANSMITTER

In airborne applications and systems where it is desirable to transmit data and clock information over the same transmission link the 8T20 is extremely useful. The waveforms in Figure 12 show that in order to convert binary data to a di-phase code it is necessary to conditionally double the input clock frequency, depending on whether a logical "1" or logical "0" is to be sent. The 8T20 is ideally suited for this frequency doubler application and far superior to exclusive-OR doubler circuits which suffer from pulse jitter problems. Because the 8T20 has triggering edge control, logic design is simplified over a discrete approach. The binary data can be fed into the PEC terminal without additional logic. The $\overline{Q}$ output of the bidirectional one-shot generates trigger pulses for the driver flip-flop (1/2 7473) as illustrated in Figure 13. To make the transmitter more useful, Figure 13 also shows how 10 channnels can be multiplexed by using an 8274 10-bit parallel-in, serial-out shift register and a 74192 divide-by-ten counter.

WAVEFORMS

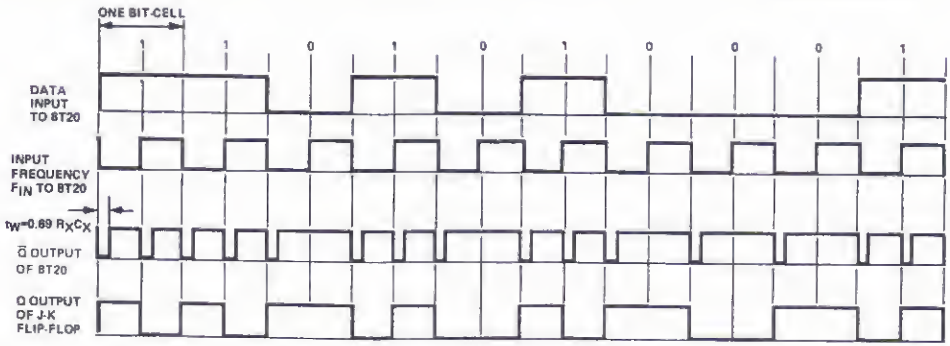


FIGURE 12

BINARY TO DI–PHASE TRANSMITTER

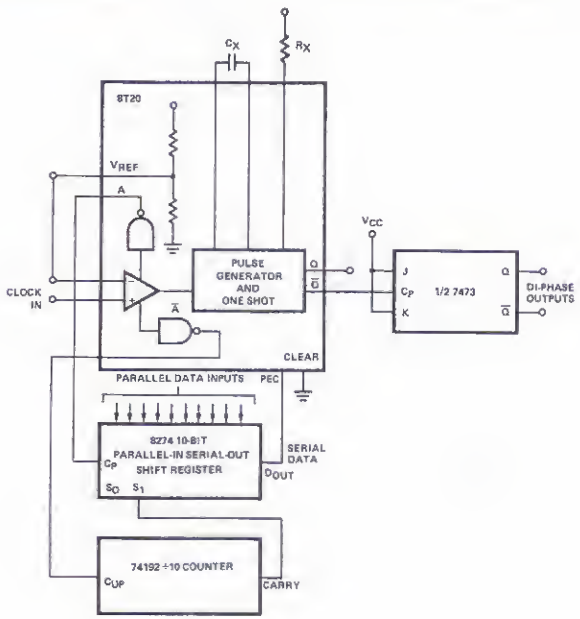


FIGURE 13

DI–PHASE TO BINARY RECEIVER

To recover the di-phase signal just described, Figure 14 shows the 8T20 input acting as a line receiver while the one-shot portion is conditioned as a frequency doubler. The addition of a 74121 non-retriggerable one-shot will recover the clock signal by choosing a duty cycle long enough to only permit one clock pulse per bit cell.

The 8T20 also triggers a 7473 flip-flop which is reset by the data-clock as well. Thus, whenever a logical "1" is to be clocked into the 8273 10-bit serial-in, parallel-out shift register, the Q output of the 7473 puts out a pulse. Figure 15 illustrates the waveforms associated with the di-phase to binary receiver circuit. The recovered data can be monitored at the Q_1 output of the 8273 shift register and is shown in Figure 14.

DI–PHASE TO BINARY RECEIVER

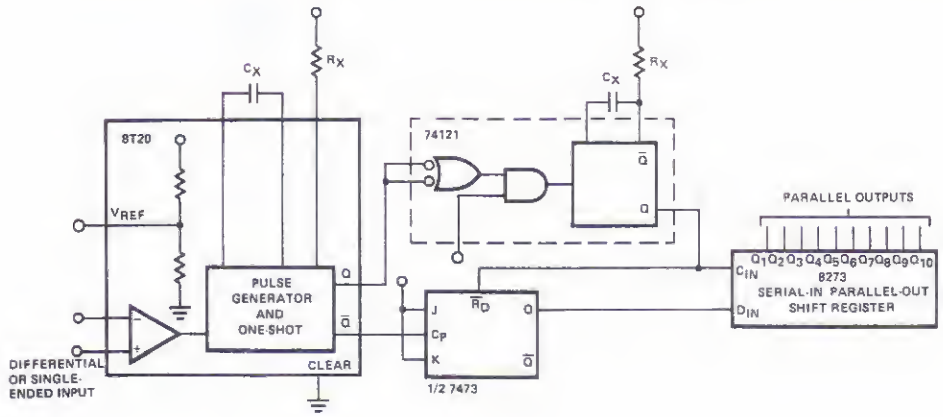


FIGURE 14

WAVEFORMS

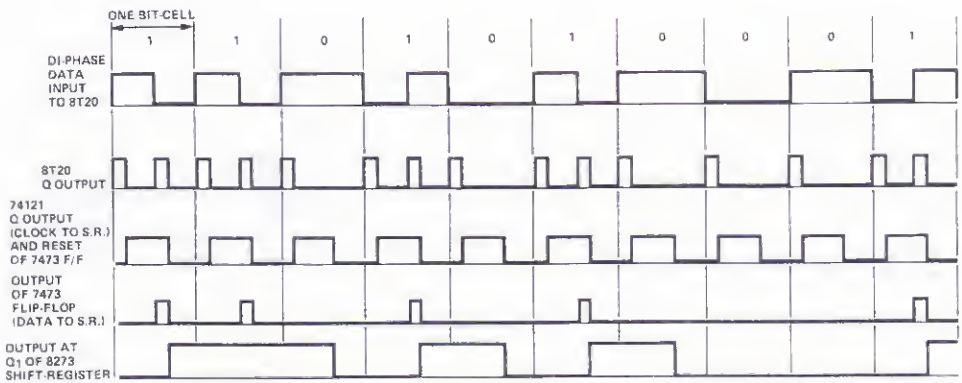


FIGURE 15

HYSTERESIS INCREASES VERSATILITY OF THE 8T20 BI-DIRECTIONAL ONE-SHOT

To extend the usefulness of the 8T20 to systems usage where hysteresis is desirable (i.e., when receiving signal's in a high noise environment or signals with slow edges) feedback can be employed by using the buffered limiter outputs A and $\overline{A}$. Depending on whether the 8T20 is used in a single ended application or in a differential configuration, hysteresis is easily obtained by referring to Figures 16 and 17 respectively.

In Figure 16a the $\overline{A}$ output of the limiter is used to provide feedback to the negative input of the comparator of the 8T20. The state of $\overline{A}$ output determines if R_3 is switched in or out of the hysteresis loop. The thresholds are influenced by the input impedance but are easily approximated as:

$$\text{Lower Threshold Voltage } (V_{LT}) = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$\text{Upper Threshold Voltage } (V_{UT}) = \frac{R_2 // R_3}{R_1 + R_2 // R_3} V_{CC}$$

Performance data for this circuit are shown in Figure 16b.

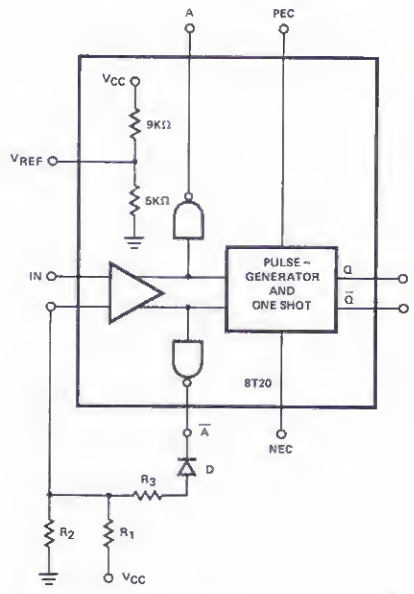
For a symmetrical feedback arrangement advantage can be taken of both the A and $\overline{A}$ outputs by feeding them back as shown in Figure 17a. R_1 and R_4 are the feedback resistors and if they are the same value, hysteresis is symmetrical around zero with the following threshold voltages:

$$\text{Lower Threshold Voltage } (V_{LT}) = \frac{R_4\ V_1 \text{ out}}{R_4 + R_2}$$

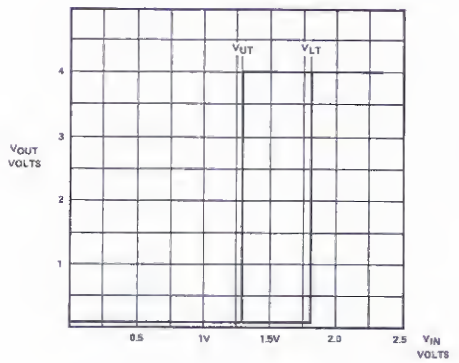
$$\text{Upper Threshold Voltage } (V_{UT}) = \frac{-R_3\ V_1 \text{ out}}{R_1 + R_3}$$

V_1 out is the logical "1" output voltage of the $\overline{A}$ and A TTL totempole outputs (approximately 3.5 Volts). Performance data for the symmetrical hysteresis circuit are shown in Figure 17b.

SINGLE ENDED FEEDBACK FOR HYSTERESIS



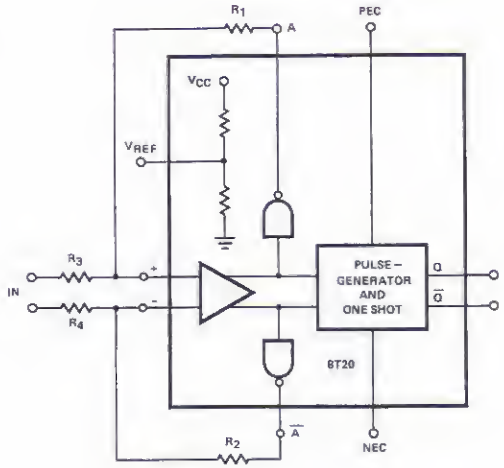
a.



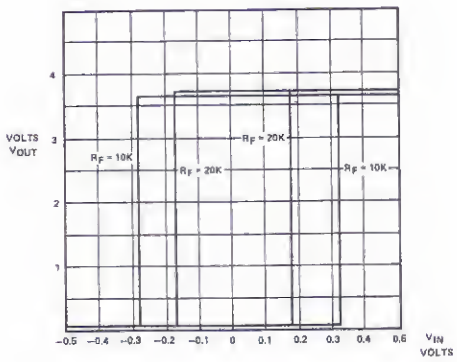
b.

FIGURE 16

SYMMETRICAL FEEDBACK FOR HYSTERESIS



a.



b.

FIGURE 17

DIGITAL 8000 SERIES TTL/MSI

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

INTRODUCTION

The Signetics 8T22 Retriggerable monostable multivibrator is a one-shot that has a duty cycle as high as 100% and responds to input triggers while in an active timing state. After the last input pulse is received, the 8T22 completes one timing cycle.

APPLICATIONS

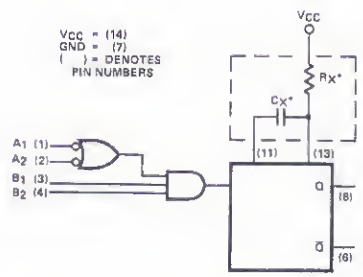
- 100% maximum duty cycle
- Leading and trailing edge triggering
- Maximum repetition rate >10mHz
- D-C coupled inputs insensitive to input transition times.
- Output pulse width insensitive to power supply variations
- Input clamp diodes
- Pin-for-pin replacement for 9601.

Applications of the 8T22 retriggerable one-shot include missing pulse detection, oscillator circuits, variable pulse delay generation, non-retriggerable operation, pulse duration modulation and others.

DEVICE DESCRIPTION

A functional block diagram of the 8T22 is shown in Figure 1. The multivibrator has four inputs, two active *high* and two active *low*. This allows leading edge and/or trailing edge triggering. The TTL inputs are level sensitive and make triggering independent of input transition times. When input conditions for triggering are met according to the truth table also shown in Figure 2, a new timing cycle starts. The external timing capacitor, C_X is rapidly discharged and then allowed to charge through R_X. An input cycle time shorter than the output cycle time will retrigger the 8T22 and result in a continuously high Q output. Retriggering, however, may be inhibited by tying the $\overline{Q}$ output back to an active low input as shown in the applications section. Complementary outputs with active pull-ups are provided for maximum systems flexibility.

LOGIC DIAGRAM



*EXTERNAL TIMING DIAGRAM

FIGURE 1

TRIGGERING TRUTH TABLE

PIN NUMBER			
1	2	3	4
H→L	H	H	H
H	H→L	H	H
L	X	L→H	H
X	L	L→H	H
L	X	H	L→H
X	L	H	L→H

OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram. (Figure 1)
2. The value of R_X may vary from 5.0 to 50 kΩ for 0 to 75°C operation.
3. C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_x}\right]$$

Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Figure 2.

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   - A. For use with low leakage electrolytic capacitors.
     The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and Rule 3 above is satisfied.
   - B. Use with high inverse leakage current electrolytic capacitors.
     The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

     $$t \approx 0.3\ RC_X$$

   - C. Use to obtain extended pulse widths:
     This configuration obtains extended pulse widths, because of the larger timing resistor allowed by Beta multiplication. Electrolytics with high (>5 μA) inverse leakage currents can be used.

     $R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or <2.5 MΩ whichever is lesser

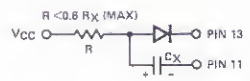
     R_X (min) < R_Y < R_X (max) ($5 \leqslant R_Y \leqslant 10$ kΩ is recommended)

     Q_1: NPN silicon transistor with h_{FE} requirements of above equations.

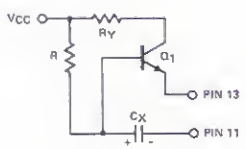
     Output pulse width, $t \approx 0.3\ RC_X$

     Configuration B and C are not recommended with retriggerable operation.

a.

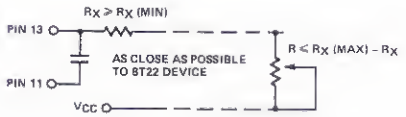


b.



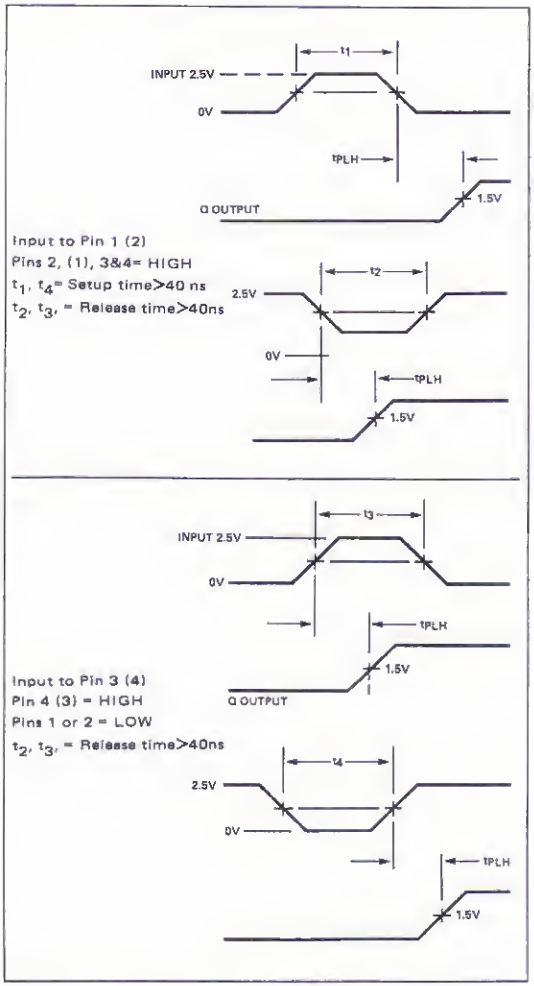
c.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

8. Input Trigger Pulse Rules. (See Triggering Truth Table)



9. The retrigger pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.32\ R_X C_X \left(1 + \frac{0.7}{R_X}\right) + t_{PLH}$$

The retrigger pulse width is equal to the pulse width t plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t.

NOTE: Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle time.)

10. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located close to the 8T22 is recommended.

OUTPUT PULSE WIDTH

As given in Operating Rule 5, the output pulse width (t) is defined by the relationship

$$t = 0.32\ R_X\ C_X \left[1 + \frac{0.7}{R_X}\right]$$

Where R_X is in KΩ and C_X is in pF, t is ns

However for capacitor values less than 1000 pF, the typical curve below should be used.

TYPICAL OUTPUT PULSE WIDTH FOR C_X<1000pF

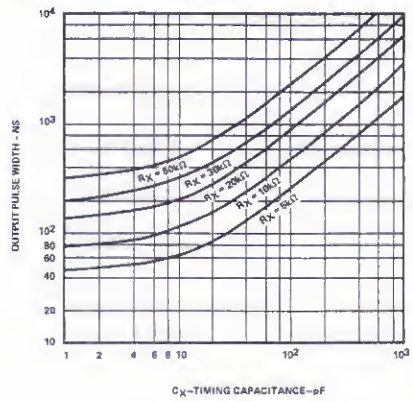


FIGURE 2

APPLICATIONS

The 8T22 can be used for virtually any application currently performed by other discrete or IC one-shots. Its 100% duty cycle and retriggerability make it a universal building block for all one-shot applications. Typical applications of the 8T22 are shown in the following discussion.

NON-RETRIGGERABLE OPERATION

In situations where non-retriggerable operation is required, i.e., where input triggers are ignored during the output cycle, the input gating may be used to inhibit retriggerability, as illustrated in Figure 3. This connection may be used for frequency division of a fixed frequency input. By selection of appropriate values of R_X and C_X, the 8T22 will retrigger on some multiple of input pulses.

CONNECTION FOR
NON-RETRIGGERABLE OPERATION

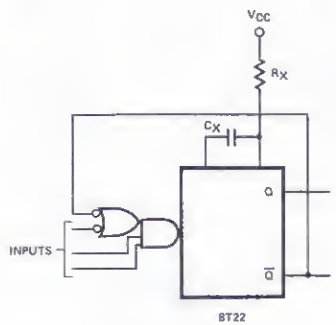


FIGURE 3

OSCILLATOR CIRCUITS

The most common astable multivibrator connection of an 8T22 is shown in Figure 4. By returning the normally high $\overline{Q}$ output to the input AND gate, a retrigger signal is generated (low to high transition) when the timing cycle has expired. Thus the 8T22 acts as an oscillator with a typical positive pulse width of 25ns. In those applications where longer positive pulses are required, they may be stretched as the two suggestions in Figure 5 show.

BASIC ASTABLE CONFIGURATION

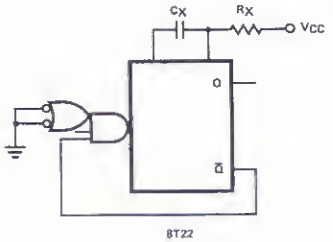


FIGURE 4

TWO METHODS OF EXTENDING 8T22 OSCILLATOR

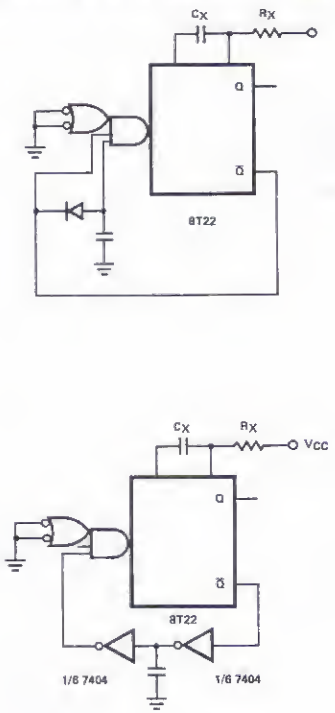


FIGURE 5

One method that may be used in constructing a low frequency multivibrator without using a large capacitor is shown in Figure 6. In this case, resistor R_X is returned to the Q output rather than to V_{CC}. With C_X = 0.47μF and R = 47K 100 Hz operation with 30 ms pulse width has been achieved.

100 Hz MULTIVIBRATOR 2ms PULSE WIDTH

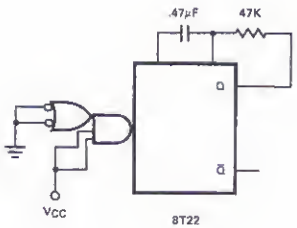


FIGURE 6

In applications where a gated clock generator is necessary, the circuit shown in Figure 7 is useful since it prevents output transients from occurring when the clock generator turns on following an enable signal. The 7404 inverters together with the capacitor C serve as delays to increase the output pulse width.

DELAYED PULSE GENERATION

Two 8T22's connected in series provide a means of delaying an input pulse and varying the pulse width. Shown in Figure 8, 8T22 #1 determines the time T_1 before the initiation of the output pulse, and the 8T22 #2 determines the output pulse width. While the timing cycle is active, the 8T22's $\overline{Q}$ output is low, the Q output low-to high transition at the end of the timing cycle triggers the 8T22 #2. In addition, by returning the $\overline{Q}$ output of the 8T22 #2 to the input of 8T22 #1, a low frequency oscillator with variable duty cycle output may be achieved.

MISSING PULSE DETECTOR

The retriggering capability of the 8T22 can be utilized to provide an indication of a missing pulse in a bit stream. R_X and C_X should be selected to provide a pulse width greater than the maximum time between successive pulses. Figure 9 shows the circuit and associated waveforms.

DOUBLE PULSE DETECTOR

A double pulse may also be detected with the 8T22 as illustrated in Figure 10. Whenever an extra pulse occurs while the one-shot is timing out, the 1/4 7400 gate output will go low indicating the presence of the double pulse.

GATED CLOCK GENERATOR

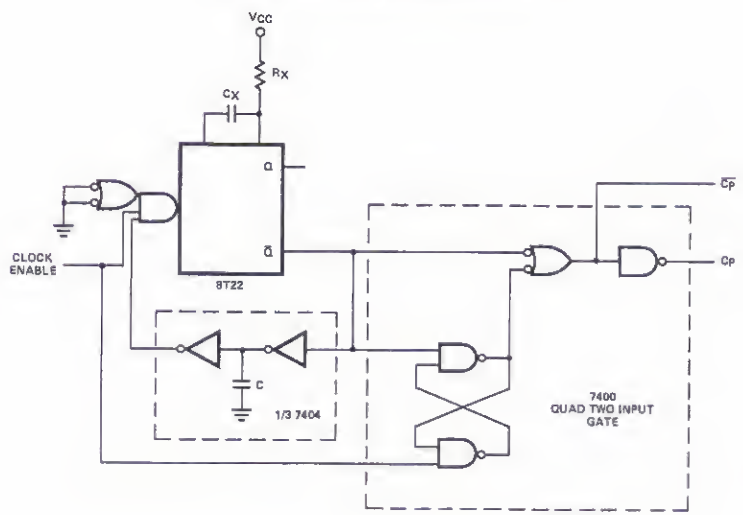


FIGURE 7

DELAYED PULSE GENERATION

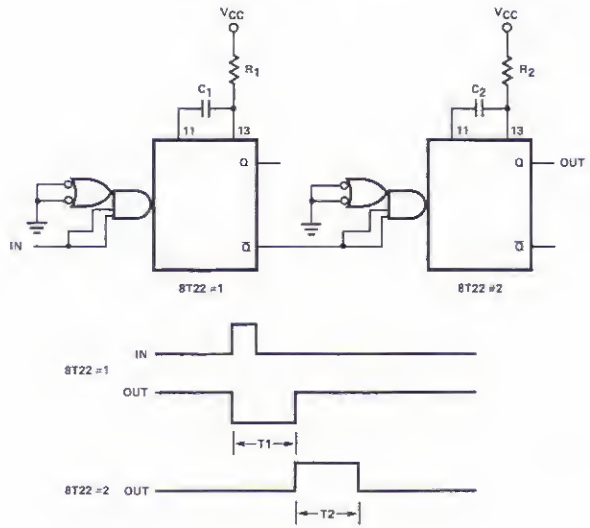


FIGURE 8

MISSING PULSE DETECTOR

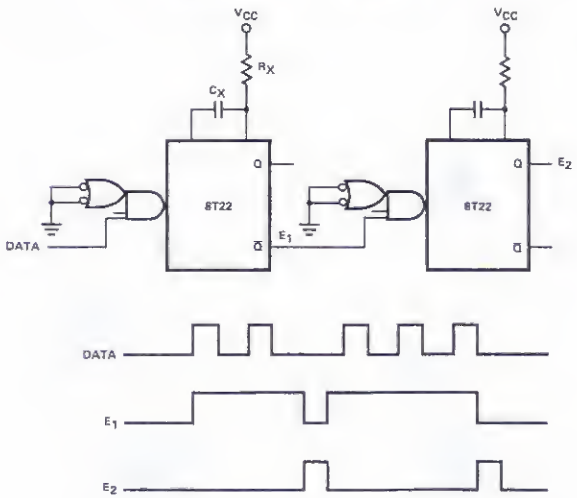


FIGURE 9

DOUBLE PULSE DETECTOR

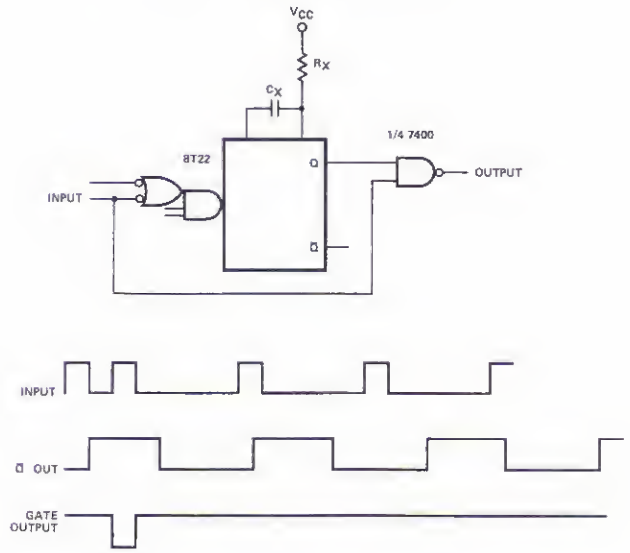


FIGURE 10

VOLTAGE TO FREQUENCY CONVERTER

A linear voltage-to-frequency converter particularly suitable for Voltage-Controlled Oscillator Applications (VCO's) where a high frequency/voltage change ratio is required is shown in Figure 11. Frequency changes of over 10 to 1 have been obtained by this method.

VOLTAGE-TO-FREQUENCY CONVERTER

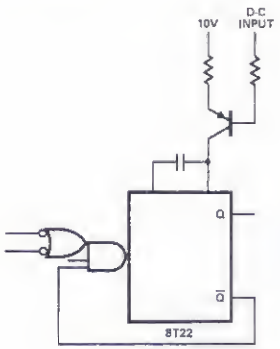


FIGURE 11

PULSE DURATION TRANSMISSION SYSTEMS

Pulse duration modulation can be accomplished with the 8T22 one-shot. Therefore, the device may be used for data transmission which allows both data information and clock pulses to be transmitted over a single line. PDM encoding is done as shown in Figure 12.

PDM MODULATION

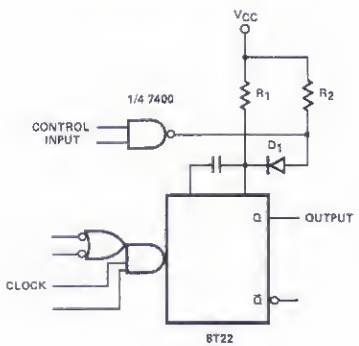


FIGURE 12

Two current supplying resistors are used to provide timing cycle modulation. When R_2 is pulled to ground by the buffer, D_1 becomes reverse biased, thus making the timing cycle a function of R_1 alone and producing a long (logical 1) pulse. When R_2 is released, the effective resistance is lowered, and a shorter (logical 0) pulse.

The decoding of PDM signals is shown in Figure 13. If the input data present a logical 0 (33% duty cycle) to the 8T22 detector, the timing cycle will be longer than the input data pulse. The Q output of the 8T22 joins to its normally low state will clock a logical 0 into the 8270 four-bit shift register. A logical 1 signal (66% duty cycle) will still be high after the 8T22 times out, thereby clocking a logical 1 into the shift register.

PDM DETECTION

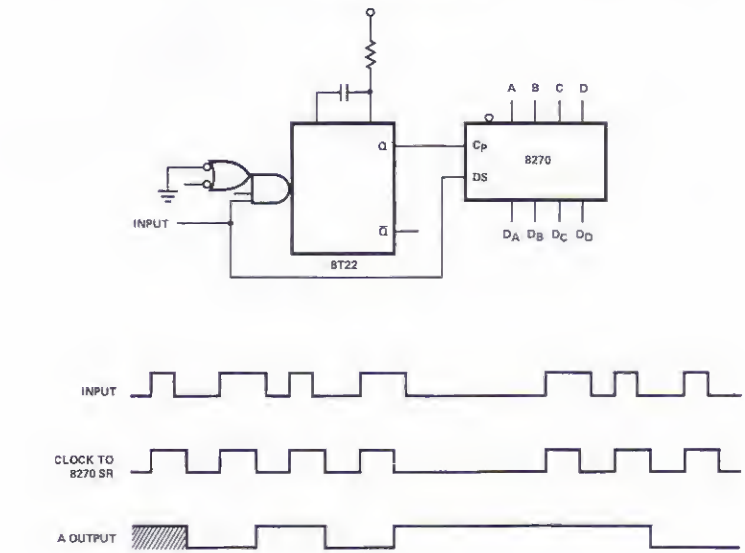


FIGURE 13

8T23 LINE DRIVER/8T24 LINE RECEIVER

INTRODUCTION

The 8T23 Dual Line Driver and 8T24 Triple Line Receiver have been designed to meet the IBM System/360 and System/370 channel to control (I/O) interface specifications. These monolithic interface IC's are particularly useful to computer and peripheral equipment manufactures who must interface with IBM computers and IBM compatible equipment.

The 8T23 and 8T24 are similar to the 8T13 Line Driver and 8T14 Line Receiver in their respective circuit designs and electrical characteristics. Therefore, the reader is referred to the applications memo covering the 8T13 and 8T14 for detailed circuit descriptions and more information pertaining to driving low impedance lines.

In the following discussion, IBM spacifications (GA 22-6974-0) for interface circuits will be compared to the 8T23 and 8T24 electrical characteristics and their systems behavior.

DEVICE DESCRIPTION OF THE 8T23

As shown in Figure 1, the 8T23 consists of two line drivers that each have AND-OR logic to determine the output state of the driver. Both input and output are TTL compatible and the device is operated from a single 5V power supply. The outputs are uncommitted emitter followers with built-in short circuit protection and are capable of driving low impedance transmission lines such as coaxial cable, twisted pair or ribbon conductors. Outputs of 8T23 drivers may be dot-ORed for party-line applications as well as increased drive capability. For reference the typical output current vs. output voltage curve is shown in Fig. 2.

8T23 DUAL LINE DRIVER

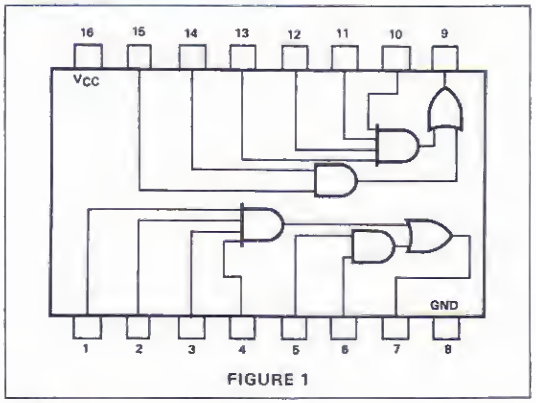


FIGURE 1

TYPICAL OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR THE 8T23

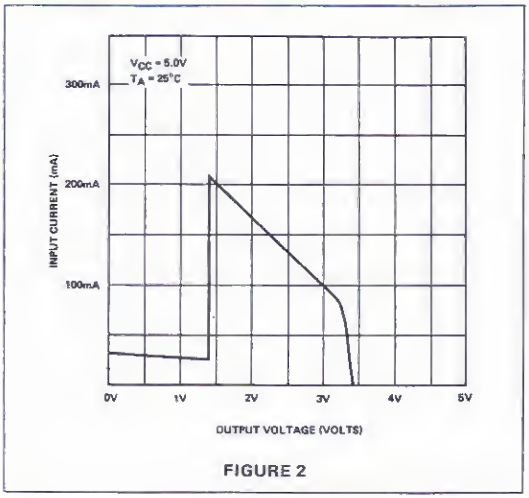


FIGURE 2

LINE DRIVER REQUIREMENTS

In Table I, the general electrical characteristics for the 8T23 line driver are compared to the requirement of the IBM specifications. It can be seen that the logical "1" and "0" level as well as fan-out considerations are met.

Because the 8T23 has uncommitted emitter follower outputs, multiple drivers and receivers can be connected onto one line in party-line applications. As required by the IBM specification, one driver can fan-out to ten receivers and up to ten driver outputs can be connected together (dot-ORed) to drive one receiver.

POWER–UP POWER–DOWN SEQUENCE FOR THE 8T23

The 8T23 line driver has been designed to ensure that no spurious noise is generated during a normal power-up or power-down sequence. Figures 3a and 3b show that the driver output stays in the logical "0" state regardless of the rate of rise or fall of V_{CC}, provided one or more inputs to each AND gate are at a logical "0" during the turn-on or turn-off of the power supply.

Figures 3c and 3d are included for completeness and show the results if a driver is powered-up with a logical "1" state defined at the output. The output will simply follow V_{CC} and not introduce noise.

LINE DRIVER

INTERFACE REQUIREMENT	IBM SPECIFICATION	8T23 SPECIFICATION	MEETS OR EXCEEDS IBM SPECIFICATION
$V_{OUT}(0)$ LOGICAL 0 OUTPUT VOLTAGE AT +240μA*	0.15V(MAX.)	0.15V(MAX.)	YES
$V_{OUT}(1)$ LOGICAL 1 OUTPUT VOLTAGE AT +59.3mA*	3.11V(MIN.)	3.11V(MIN.)	YES
FAN–OUT CAPABILITY	10 RECEIVERS	> 10 RECEIVERS	YES
DOT–OR CAPABILITY	10 DRIVERS	> 10 DRIVERS	YES

* Positive direction of current is out of the driver.

POWER–UP AND POWER–DOWN CHARACTERISTICS OF THE 8T23

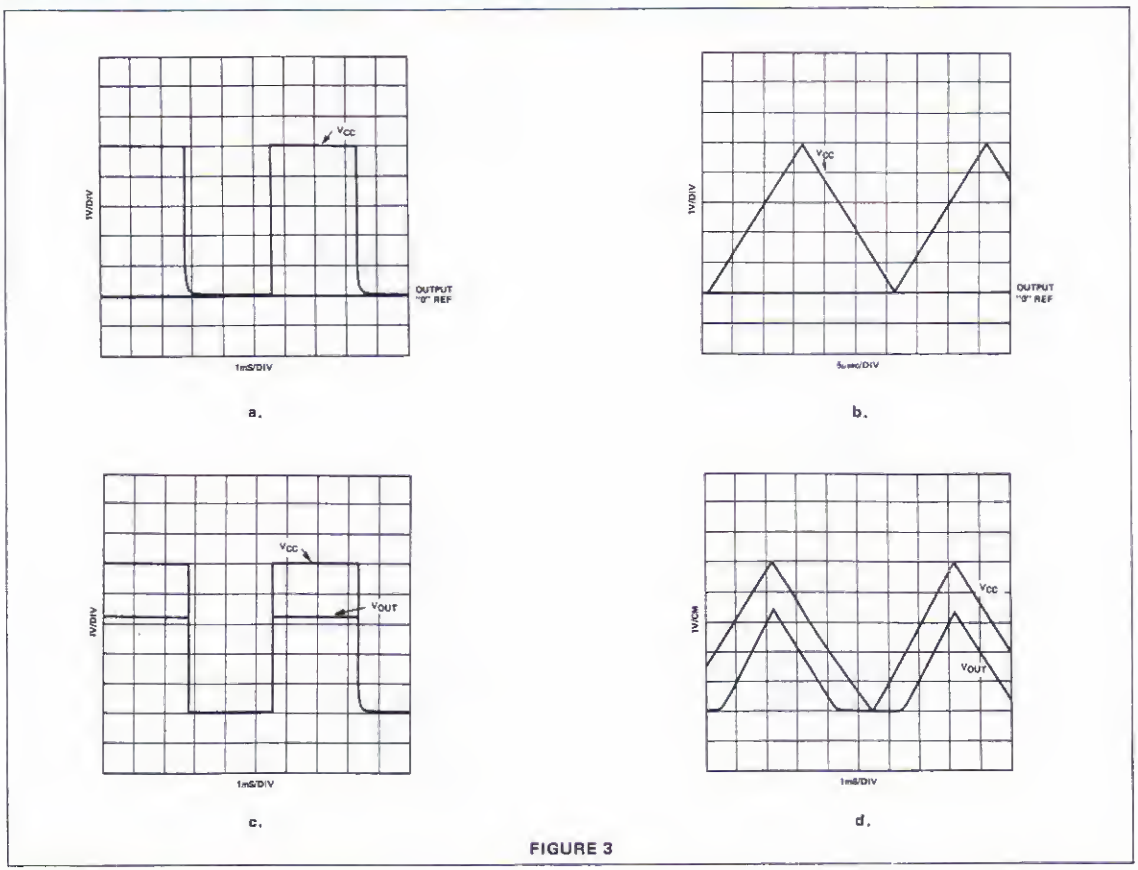


FIGURE 3

DESCRIPTION OF THE 8T24

The logic diagram of the 8T24 triple line receiver is shown in Figure 4. Each receiver may be strobed independently and has additional control logic to allow the output to be forced to a logical "0" by external control signals. Like the 8T23 line driver, the 8T24 line receiver is also TTL compatible and operates from a single 5V power supply.

Because the 8T24 is intended for use at the receiving end of digital transmission lines, the device has built in hysteresis to discriminate against line reflections and noise. The 8T24 has been designed with high input impedance and will contribute insignificant loading effects to the transmission line. This is an important factor when several receivers have to be driven by the same driver as in the party-line applications and bus-oriented systems.

8T24 TRIPLE LINE RECEIVER

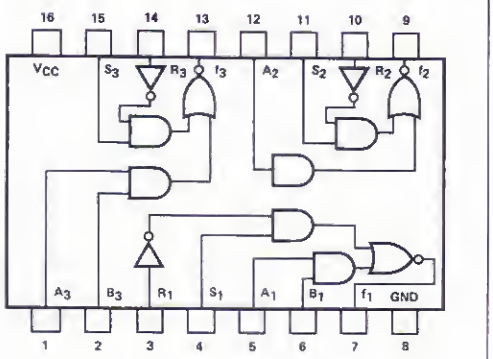


FIGURE 4

LINE RECEIVER REQUIREMENTS

Table 2 shows that the 8T24 meets the electrical characteristics as defined by the IBM interface specifications. As already mentioned under the 8T23 driver characteristics, at least 10 receivers can be driven by one line driver.

One area of the IBM specifications that should be clearly understood is that of threshold voltages. An input voltage of 1.7V or more shall be interpreted as a logical "1", and an input of 0.7V or less shall be interpreted as a logical "0". Therefore, having defined the minimum logical "1" level and the maximum logical "0" level the designer has to decide on the actual transfer curve most desirable.

The 8T24 has been designed with hysteresis since it gives the highest noise immunity possible. Figure 5a shows a transfer curve for a hypothetical receiver without hysteresis whereas the 8T24 transfer curve is shown in Figure 5b. It can be seen that both approaches meet the same specification but that the 8T24 has greatly improved noise immunity as illustrated in Table 3.

LINE RECEIVER

INTERFACE REQUIREMENT	IBM SPECIFICATION	8T24 SPECIFICATION	MEETS OR EXCEEDS IBM SPECIFICATION
$I_{IN}(1)$ LOGICAL 1 INPUT CURRENT AT 3.11V	0.42mA(MAX.)	0.17mA(MAX.)	YES
$-I_{IN}(0)$ LOGICAL 0 INPUT CURRENT AT 0.15V	−0.24mA(MAX.)	+5μA *	YES
$V_{IN}(1)$min MINIMUM LOGICAL 1 INPUT VOLTAGE	1.7V	1.7V	YES
$V_{IN}(0)$max MAXIMUM LOGICAL 0 INPUT VOLTAGE	0.7V	0.7V	YES
V_{IN}(max) MAXIMUM INPUT VOLTAGE POWER-ON	7.0V	7.0V	YES
V_{IN}(max) MAXIMUM INPUT VOLTAGE POWER-OFF	6.0V	6.0V	YES

* With 0.15V applied current direction is into the 8T24.

LINE RECEIVER TRANSFER CURVES

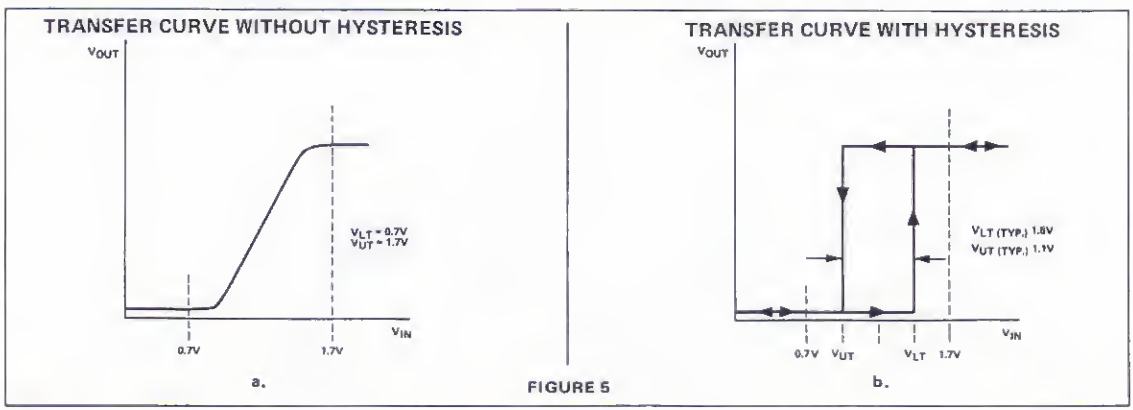


FIGURE 5

RECEIVER WITHOUT HYSTERESIS	SIGNETICS 8T24
$N_1 = V_1 - V_{UT}$, = 3.11V–1.7V, = 1.41V	$N_1 = V_1 - V_{UT}$, = 3.11V–1.1V, =2.01V
$N_0 = V_{LT} - V_0$, = 0.7V–0.15V, = 0.55V	$N_0 = V_{LT} - V_0$, = 1.5V–0.15V, = 1.35V

Where:

N_1 = Logical "1" DC Noise Margin
N_0 = Logical "0" DC Noise Margin
V_1 = Driver output voltage in the logical "1" state
V_0 = Driver output voltage in the logical "0" state
V_{LT} = Input threshold voltage when output is switched from a logical "0" to a logical "1"
V_{UT} = Input threshold voltage when output is switched from a logical "1" to a logical "0"

POWER–UP POWER–DOWN SEQUENCE FOR THE 8T24

The 8T24 line receiver has been designed to ensure that no spurious noise is generated during a normal power-up or power-down sequence. The receiver input will never require more than the specified input current and will not generate transients when turned on or off.

GENERAL SYSTEMS CONSIDERATIONS

A typical application of the 8T23 line driver and the 8T24 is shown in Figure 6. For an IBM interface the line has a characteristic impedance of 92Ω ±10% and is terminated at each end in its characteristic impedance by a terminating network. This may be a resistor presenting an impedance of 95Ω ±2.5% connected between the signal line and ground.

Fault-conditions on the transmission line will not damage 8T23 drivers or 8T24 receivers. When a signal line is accidently shorted the driver will current limit because of its built-in short circuit protection (ref. Figure 2). The receivers will not be damaged by over-voltages as shown in Table 2. In addition ground-shifts or noise up to -0.15V will not damage the receiver.

All communication to and from the channel occurs over a common bus. General considerations for party line applications of multiple drivers and receivers are discussed in the 8T13 and 8T14 applications memo and the reader may make reference to that section.

Selection of a control unit is established by the "Select Out" circuitry consisting of a single line driver and a single line receiver with only the receiver end of the line terminated in the characteristic impedance. The 8T24 meets the "Select Out" receiver characteristics and the 8T23 has been used successfully supplying 41mA with an output voltage of 3.9 volts if the driver is operated with a 6V ±5% power supply. Although no data sheet guarantees are given in this instance most 8T23 units are expected to perform satisfactorily with a 6V ±5% supply voltage.

TYPICAL LINE–DRIVER LINE–RECEIVER APPLICATION

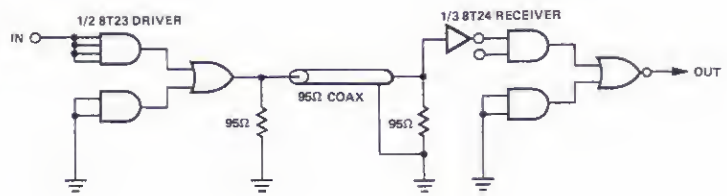


FIGURE 6

INTRODUCTION

The 8T25 is a dual MOS to TTL interface element combining sense amplifiers and bus oriented tri-state latches that operate from a single 5V power supply. The amplifier inputs are ideally suited to sense low level currents such as those available from MOS devices.

The particular applications discussed are oriented towards memory systems design where TTL interfaces with the 2548 2K MOS RAM and the 1103 1K MOS RAM are desired. There are many other applications such as analog to digital interfaces in which the 8T25 may be useful.

DEVICE DESCRIPTION

As shown in Figure 1 the 8T25 consists of two sense amplifiers/latches with common strobe and enable lines. The amplifier inputs are designed to sense current levels and as long as the input current is below 300μA, the internally established threshold, the amplifier output will be a logical "0". If the internally established threshold of typically 300μA is exceeded, the amplifier output will be a logical 1.

8T25 LOGIC DIAGRAM

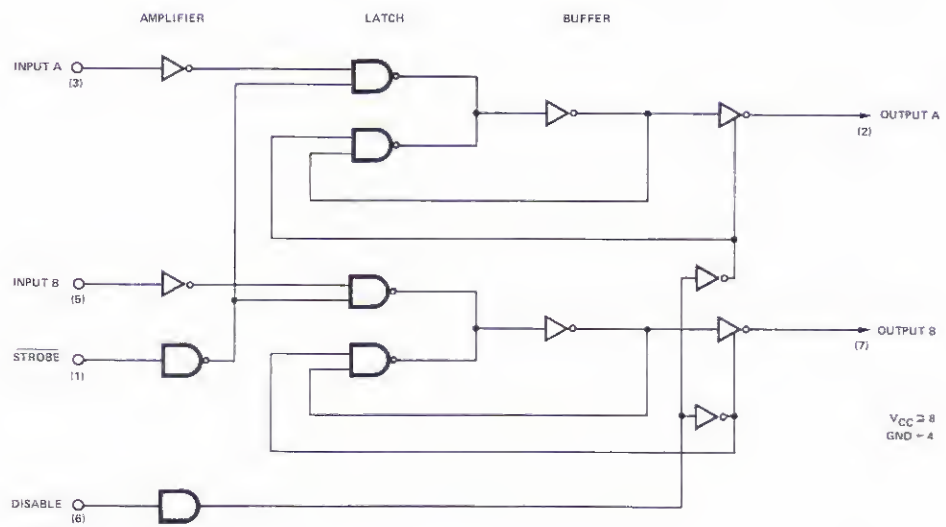


FIGURE 1

Thus, low level currents may be sensed and converted to TTL signals which are presented to the latch. The information from the amplifier may be entered into the latch in accordance with a typical operations sequence as shown in Figure 2. Preceding every data entry operation the latch must be preset by the disable pulse. Notice that as long as the disable line is in the logical "1" state the outputs are disabled, placing them in the high-Z state (i.e., in a bus system the outputs are effectively removed from the bus, except for leakage). When the disable line returns to a logical "0" the output of the latch is preset to a logical "1".

Figure 2 shows that the input current to the amplifier is below 300μA when the strobe pulse is initiated and the output will go to a logical "0" where it will stay after the strobe pulse is removed.

For the next event shown in Figure 2 the latch is preset again by the disable pulse, temporarily placing the output in the high-Z state and then returning it to a logical "1" after the disable pulse is removed. The strobe pulse now samples the input current when it is above threshold (300μA) thus keeping the output high.

TYPICAL DISABLE AND STROBE SEQUENCE

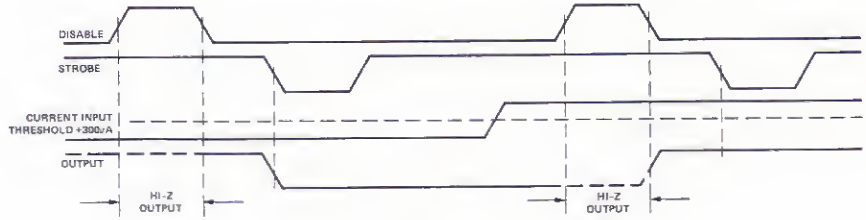


FIGURE 2

INPUT CHARACTERISTICS

For a better understanding of the sense amplifier portion of the 8T25, reference may be made to Figure 3. The theory of operation is as follows:

A current source consisting of Q_1 and Q_2 establishes a 300μA collector current through Q_2. The base-emitter voltage of Q_2 is also impressed across the base-emitter junction of Q_3 which has been designed with a geometry identical to Q_2. As a result Q_3 will try to draw the same collector current as Q_2.

INPUT STAGE OF 1/2 8T25
SENSE AMPLIFIER

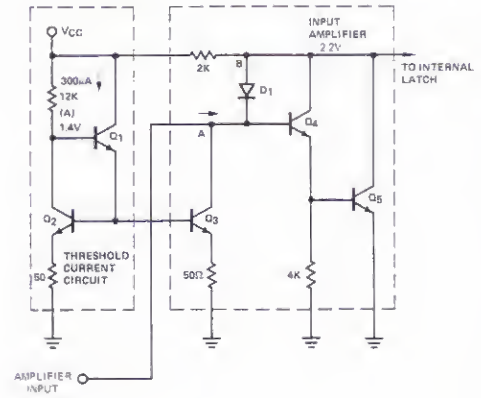


FIGURE 3

In the absence of any external currents into node A, up to 300μA can be drawn from V_{CC} through a 2K ohm resistor and diode D_1. Node B is thus placed 3 diodes drops above ground (approximately 2.2V) which is a TTL logical "1" level.

However current may also be injected at the amplifier input and as long as it is less than 300μA, node A will not rise high enough to allow Q_4 and Q_5 to be turned on. Once the input current exceeds 300μA the voltage at node A will tend to rise since the collector current of Q_2 cannot be higher than 300μA, thus turning on Q_4 and Q_5. Now node B is at the logical "0" state which is fed to the internal latch.

Figure 4 shows the behavior of the amplifier input as a function of current. The device switches at 300μA (point P) and the voltage is two diode drops above ground as established by Q_4 and Q_5 in Figure 3. Note: Excessive current into the amplifier may damage the input since it is clamped at two diode drops above ground. Current limiting should be employed if it is expected that the input current should exceed 10mA in a given application.

TYPICAL AMPLIFIER
INPUT CHARACTERISTICS

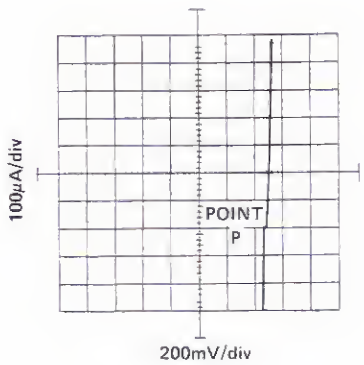


FIGURE 4

OUTPUT CHARACTERISTICS

The outputs of the 8T25 are tri-state outputs which means that they have active pull-ups that together with the current sink transistors may be disabled whenever the device is placed in the high-Z third state.* Leakage currents in the high-Z state are max 100μA when the bus is either in the "1" or "0" state. This feature makes the 8T25 suitable for data bussing applications without the need for pull-up resistors.

APPLICATIONS

Figure 5 shows how 8T25 dual sense amplifiers/latches may be used in a memory system. Inputs as well as outputs may be bus organized. Each memory card is organized as m-devices per row (m columns) by n rows. Either the 2548 2K MOS RAM or the 1103 1K MOS RAM may be used to interface with the 8T25 dual sense amplifier/latches. Since the 8T25 outputs are of the tri-state variety, individual memory cards may be connected onto a common bus without having to use pull-up resistors as shown in Figure 5.

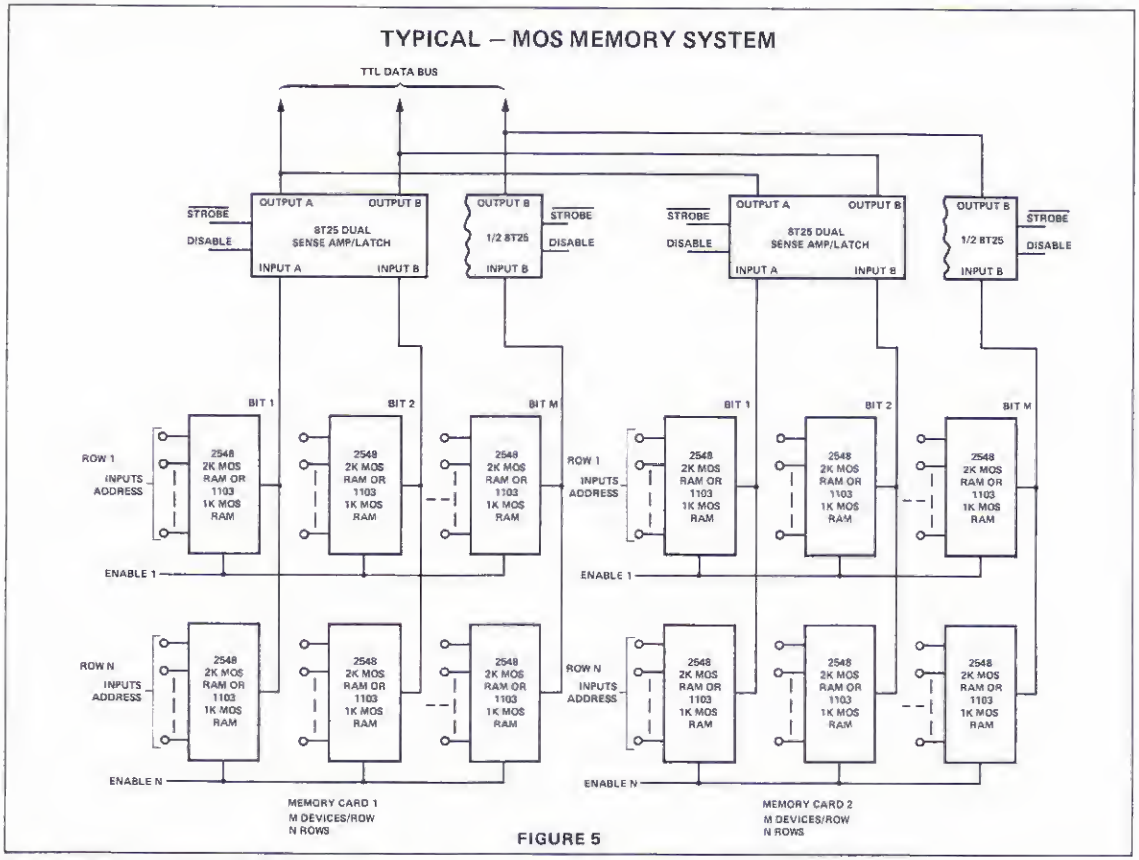


FIGURE 5

NOTE: EACH MEMORY CARD IS AN
N (2K) XM MEMORY FOR 2548 2K MOS RAM
N(K) XM MEMORY FOR 1103 1K MOS RAM

performance characteristics of one-half 8T25 driven by the 2548 2K MOS RAM are shown in Figure 6. The RAM is conditioned to read and write alternately two "1s" and two "0s" into selected locations of the memory (Figure 5A). The 8T25 is strobed during the read cycle but now while writing (waveform Figure 5B). In the particular setup used it proved convenient to preset the output of the 8T25 to a logical "1" (by means of the disable command) during the read and write cycles which does not influence the results. As it can be seen in Figure 5C, a TTL compatible signal reproduces the relevant current waveforms of the 2548 2K MOS RAM output.

Similar results hold true for the 8T25 driven by the output current of an 1103 1K MOS RAM. Although there is more noise generated during writing (Figure 7A) it does not matter in the system since the 8T25 is only strobed during the read cycle when the output current of the 1103 memory is well defined. The strobe pulse is shown in Figure 7B. The output waveforms in Figure 7C show how two "1s" and two "0s" are read out alternately. Again it should be mentioned that the 8T25 sense amplifier/latch has to be preset by means of the disable signal shown in Figure 7D prior to reading information at the output.

*See 8T09 applications memo for detailed description.

In conclusion, the strobe and disable waveforms shown in Figures 6 and 7 are easily obtained from the three clock phases in a dynamic MOS memory system. The principles of operation of the 8T25 that have been discussed here are also helpful in applying the device to other areas of systems design where current sensing has to be accomplished with a minimum amount of hardware and a single 5V power supply.

8T25 DRIVEN BY 2548 2K MOS RAM

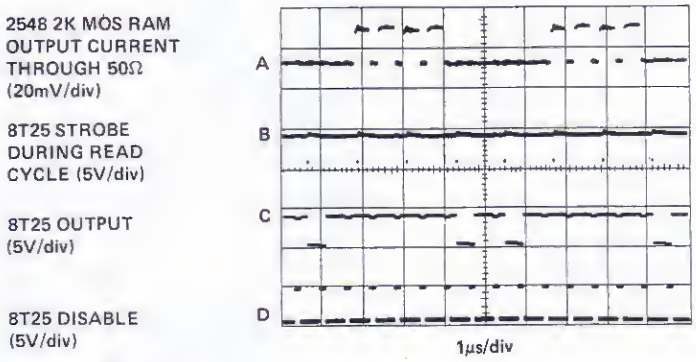


FIGURE 6

8T25 DRIVEN BY 1103 1K MOS RAM

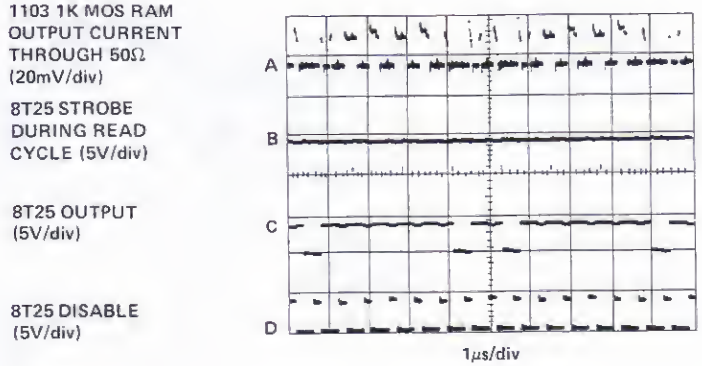


FIGURE 7

DIGITAL 8000 SERIES TTL/MSI
QUAD BUS DRIVER/RECEIVER

INTRODUCTION

The 8T26 Quad Bus Driver/Receiver is a Schottky TTL integrated circuit that has been designed for high speed bus applications. The device is particularly useful in bi-directional* data busses since it increases speed and reduces hardware compared to conventional implementations. Because of its unique design features, the 8T26 can be used in many other interface applications.

Tri-state outputs permit data bussing without the need for pull-up resistors. With an active pull-up structure with high current drive capability, line driving is facilitated even if bussing techniques are not required. In addition, low current high breakdown PNP input transistors eliminate the design constraints imposed by multiple emitter transistor inputs. This feature allows up to 200 8T26's to be driven on the same bus and also permits interfacing with data sources that cannot sink TTL input currents, particularly MOS.

Applications such as high speed I/O multiplexing, memory busses, MOS interface and various transmission line characteristics will be discussed.

LOGIC DIAGRAM

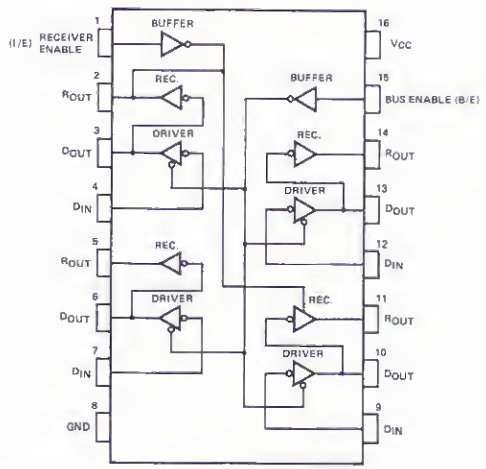


FIGURE 1

*for uni-directional busses see also 8T09 applications memo

LOGIC DESCRIPTIONS

The 8T26 consists of four driver/receiver pairs together with their enable logic as shown in Figure 1. For maximum versatility bus enable and receiver enable controls are brought out separately and buffered. A "1" on the bus enable input (B/E) allows D_{IN} data to pass through the bus driver and appear inverted at the D_{OUT} terminals. A "0" on the B/E input will force the driver output to the high impedance state and will also disable the PNP input resulting in negligible input current. The receivers are enabled by a "0" on the receiver enable (I/E) allowing data from the bus to appear inverted at the receiver output (R_{OUT}). The receiver may be forced to the high impedance state by a "1" on the I/E terminal, effectively disabling the receiver input and output. For convenience Table 1 summarizes the logic operation of the control lines.

TRUTH TABLE FOR 8T26 CONTROL LINES

TABLE 1

B/E	I/E	OPERATION
0	0	Driver Disabled, Receiver Enabled
0	1	Driver Disabled, Receiver Disabled
1	0	Driver Enabled, Receiver Enabled
1	1	Driver Enabled, Receiver Disabled

DEVICE CHARACTERISTICS

The 8T26 is a Schottky TTL design that like the 82S MSI series has PNP input transistors. As shown in Figure 2, PNP emitter followers require very little "0" level input current which is specified at max -200μA. This is significantly lower than that of standard TTL (i.e., 1.6mA) giving the systems designer a great degree of freedom when driving a large number of 8T26 inputs or when interfacing with circuits that have a low drive capability. The maximum "1" level input current is 25μA, a little lower than the 40μA of standard TTL. In addition the PNP inputs are Schottky-diode clamped to eliminate any negative ringing that may occur in systems usage.

SIMPLIFIED PNP INPUT OF 8T26

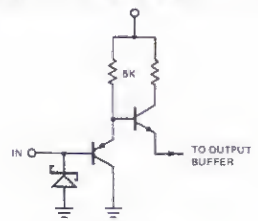


FIGURE 2

Although not shown in Figure 2 or specified on the data sheet, the PNP input transistors are also disabled when the corresponding driver or receiver is placed in the high-Z state resulting in a negative leakage current in the zero state as well (typically less than 25μA).

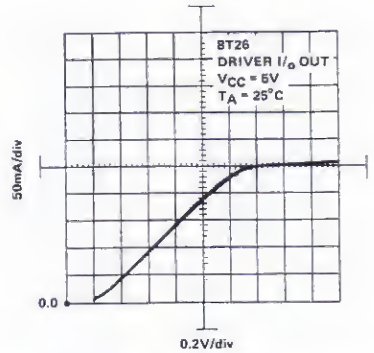
The bus driver has excellent current drive capability and is guaranteed in the data sheet at I_0 OUT = 40mA at 0.5V and at I_1 OUT = -10mA at 2.6V.

The receiver, since it generally does not have to drive long lines, is specified at I_0 OUT = 16mA and I_1 OUT = -2mA at 2.6V. For those extended range applications where typical curves of the output drive capability are desired, reference may be made to Figure 3.

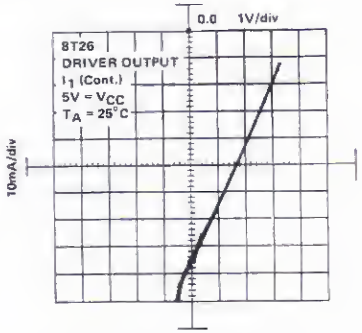
Both the driver and receiver output may be disabled when they are placed in the high-Z state which effectively removes them from the circuit except for some leakage in either the "1" state ($I_{1\ (off)}$ = -100μA at 2.6V) or in the "0" state ($I_{0\ (off)}$ = 100μA at 0.5V).

Notice that the 8T26's output drive capability is almost entirely available to accomodate current sinking from pull-up resistors or terminators when driving long lines and to provide good capacitative drive capability when many devices are on the same bus.

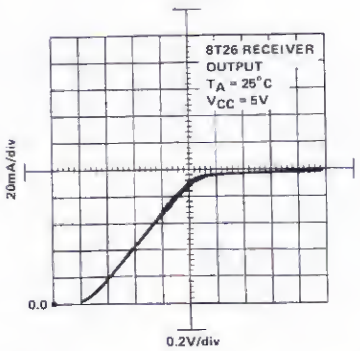
TYPICAL 8T26 OUTPUT CHARACTERISTICS



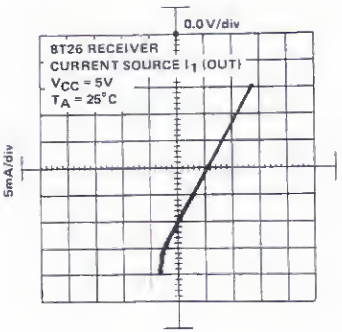
a.) TYP. CURRENT SINK CHARACTERISTICS OF BUS DRIVER



b.) TYPICAL CURRENT SOURCE CHARACTERISTICS OF BUS DRIVER



c.) TYP. CURRENT SINK CHARACTERISTICS OF BUS RECEIVER



d.) TYP. CURRENT SOURCE CHARACTERISTICS OF BUS RECEIVER

FIGURE 3

APPLICATIONS

GENERALIZED BUS INTERFACE

The most generalized way of using the 8T26 Quad Bus Driver/Receiver to its full capability is shown in Figure 4. In this application data may be interchanged over busses in either direction by attaching 8T26 driver/receiver combinations resulting in a party-line bus. This may be the case in multiplexed I/O busses or when interfacing memory boards in memory systems. Control lines may be conditioned in accordance with Table 1.

Generally speaking, the input current requirements of 8T26's is so low that systems performance is limited only by wiring capacitance and input capacitance (typically 3-5pF) but not by the number of 8T26s that can be tied onto the bus. Calculations given in Figure 5 relate the max. DC drive capability in the "1" state as well as in the "0" state to the input current requirements of an 8T26.

Using worst case data sheet conditions, 100μA of leakage in both the "1" and "0" state for a disabled 8T26 unit on the bus (B/E = 0, I/E = 1) at least 100 8T26s can be tied onto the bus. This still leaves 30mA current sink capability of the driver available to drive terminations when using long lines.

For those applications where more than 100 8T26 units must be tied onto the bus the "0" level drive capability permits to drive at least 200 enabled receiver inputs (B/E= 0, I/E = 0). It has been found in practice that the typical "1" level leakage is much lower than the data sheet guarantee of 100μA. Although no data sheet guarantees are given, 200 receiver inputs have been driven successfully in the "1" state. However as mentioned earlier the large bus capacitance will slow down operations considerably.

BIDIRECTIONAL DATA BUS

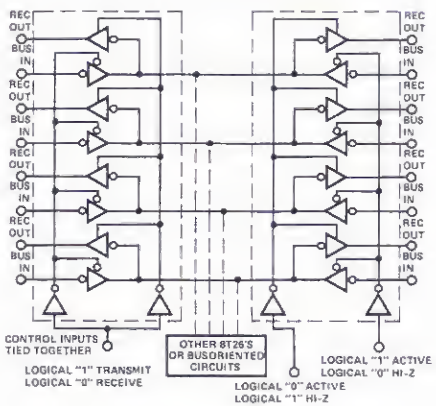
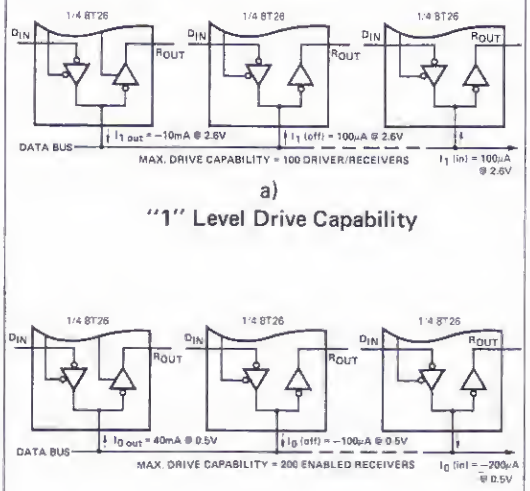


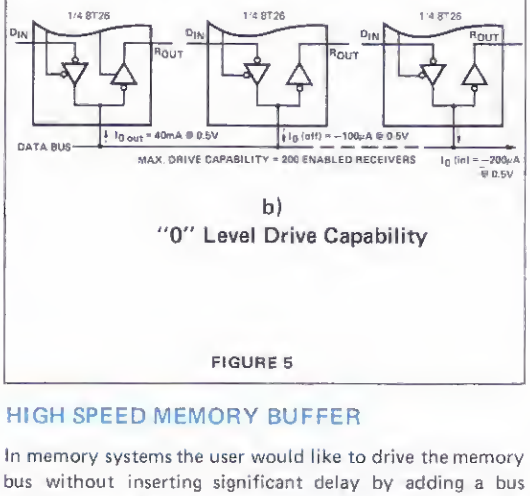
FIGURE 4

DRIVE CAPABILITY OF THE 8T26



a)

"1" Level Drive Capability



b)

"0" Level Drive Capability

FIGURE 5

HIGH SPEED MEMORY BUFFER

In memory systems the user would like to drive the memory bus without inserting significant delay by adding a bus driver while at the same time it is desirable to preserve modularity of the system by being able to expand memory without a loss in speed or systems modifications.

The 8T26 driver is an extremely fast power driver suitable to drive 300pF under full fan out (30 ohms to 2.6V) with less than a max. delay of 17ns. In addition, its tri-state outputs and low current PNP inputs allow large modular memory systems to be implemented while staying within 17ns propagation delay.

The example shown in Figure 6 illustrates that a typical memory card may be organized as a 512 X 16 array using thirty-two 82S07 256-bit bipolar RAMs and four 8T26 drivers/receivers. The memory may be made available in a 4K X 16 bits organization (i.e., 8 memory cards) but subsequently it may have to be doubled to 8K 16-bit words. Assuming that each 8T26 buffer terminal including the connector represents 10pF, even the 8K X 16 organization consisting of 16 memory cards will only represent 160pF of capacitance and delay will be less than the data sheet maximum of 17ns. Notice that the DC fan-out is much larger as shown in Figure 5 and does not have to be considered.

TRANSMISSION LINE CONSIDERATIONS

It has been mentioned that one of the advantages of the 8T26 driver outside of its tri-state capability is its higher source current capability (10mA at 2.6V) and high current sink capability (40mA at 0.5V). Since each input has Schottky-diode clamps negative ringing on long lines is eliminated and over 12 feet of unterminated cable has been driven reliably. Furthermore low value bus pull-up resistors can be used to alleviate positive overshoots because the 8T26 driver can sink large currents. Even if the 8T26 is not used as a bus-ORed driver/receiver combination, it proves useful in many applications where only the driver is needed.

To obtain the highest speed possible from the 8T26 driver/receiver, termination should be considered above 18 inches since then the bus starts to look like a transmission line. Several termination schemes can be used. For highest speed parallel termination is the most useful, whereas series termination requires the lowest power but can be used on unidirectional busses.

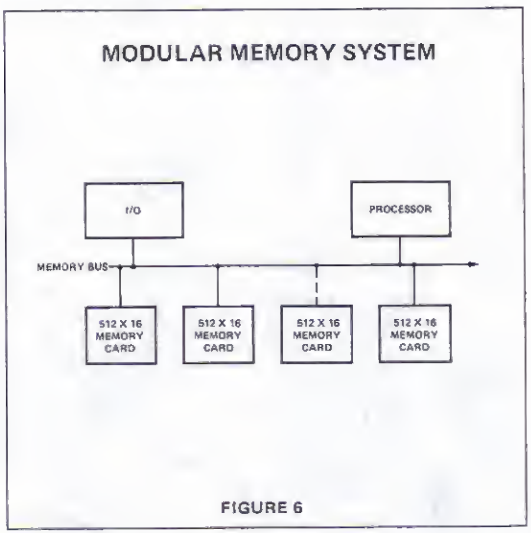


FIGURE 6

Figure 7 shows the driver of the 8T26 driving 12 feet of flat ribbon cable (char. impedance approximately 100 ohms with alternate signal and ground wires). If only uni-directional data transmission has to be considered, one terminator suffices. The line is terminated such that its Thevenin equivalent circuit looks like 130 ohms to 2.8V. Higher values of resistors may be used even if this does not terminate the line perfectly since it limits the power dissipation. Waveforms A through D in Figure 7 show the performance of the line.

For a long bi-directional data bus terminators must be placed on both ends. As shown in Figure 8 two 130 ohms equivalent circuits are placed at both ends of the transmission line. Now 8T26 driver/receiver units can be placed anywhere on the bus in a party-line fashion. Waveforms A through F in Figure 8 show the behavior of the bus.

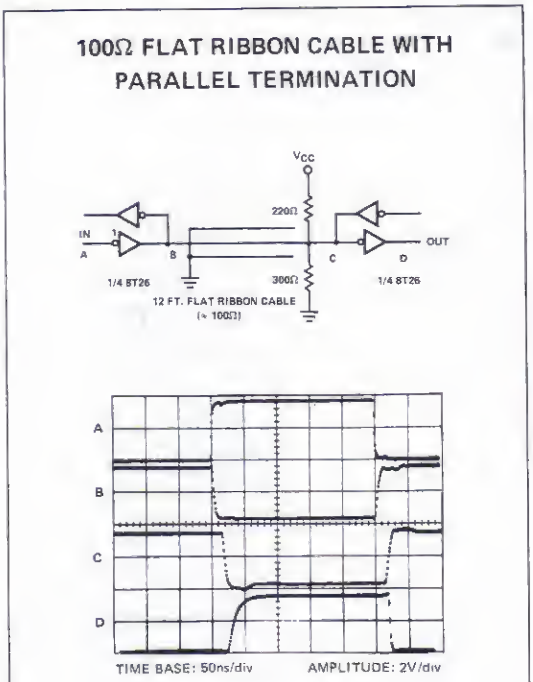


FIGURE 7

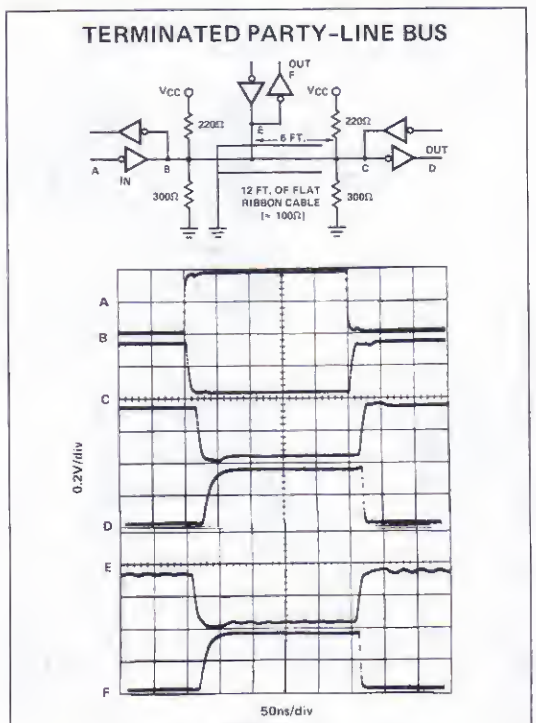


FIGURE 8

In uni-directional busses where highest speed is not necessary the 8T26 may be used with another termination scheme as shown in Figure 9. A termination resistor that together with the output resistance of the driver approximates 50 ohms, series (reverse) terminates the line. The series terminator attenuates the output amplitude by one-half at Point B Figure 9 according to transmission line theory. Since the end of the line, Point C, looks essentially like an open circuit, the amplitude doubles because of complete reflection resulting in a perfect waveform there.

COAXIAL DATA BUS WITH SERIES TERMINATION

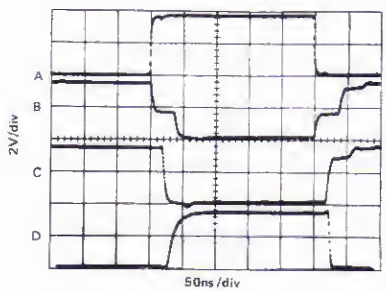
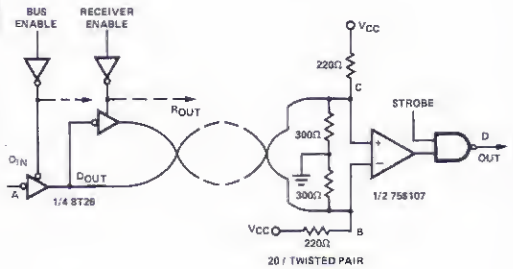


FIGURE 9

The 8T26 has also been used successfully as 4 differential line drivers as shown in Figure 10, making use of all 4 buffers as drivers. Together with the 75S107* line receiver differential data transmission up to 90 MHz has been achieved. Waveforms A through D in Figure 10 illustrate the performance of this differential transmission system.

*New Signetics Linear Circuit

DIFFERENTIAL DATA TRANSMISSION



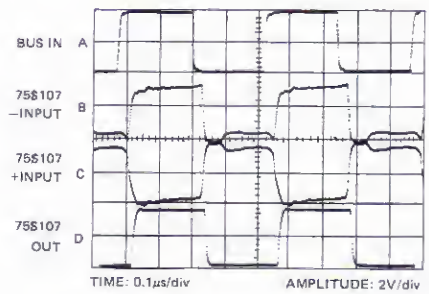


FIGURE 10

MOS INTERFACE

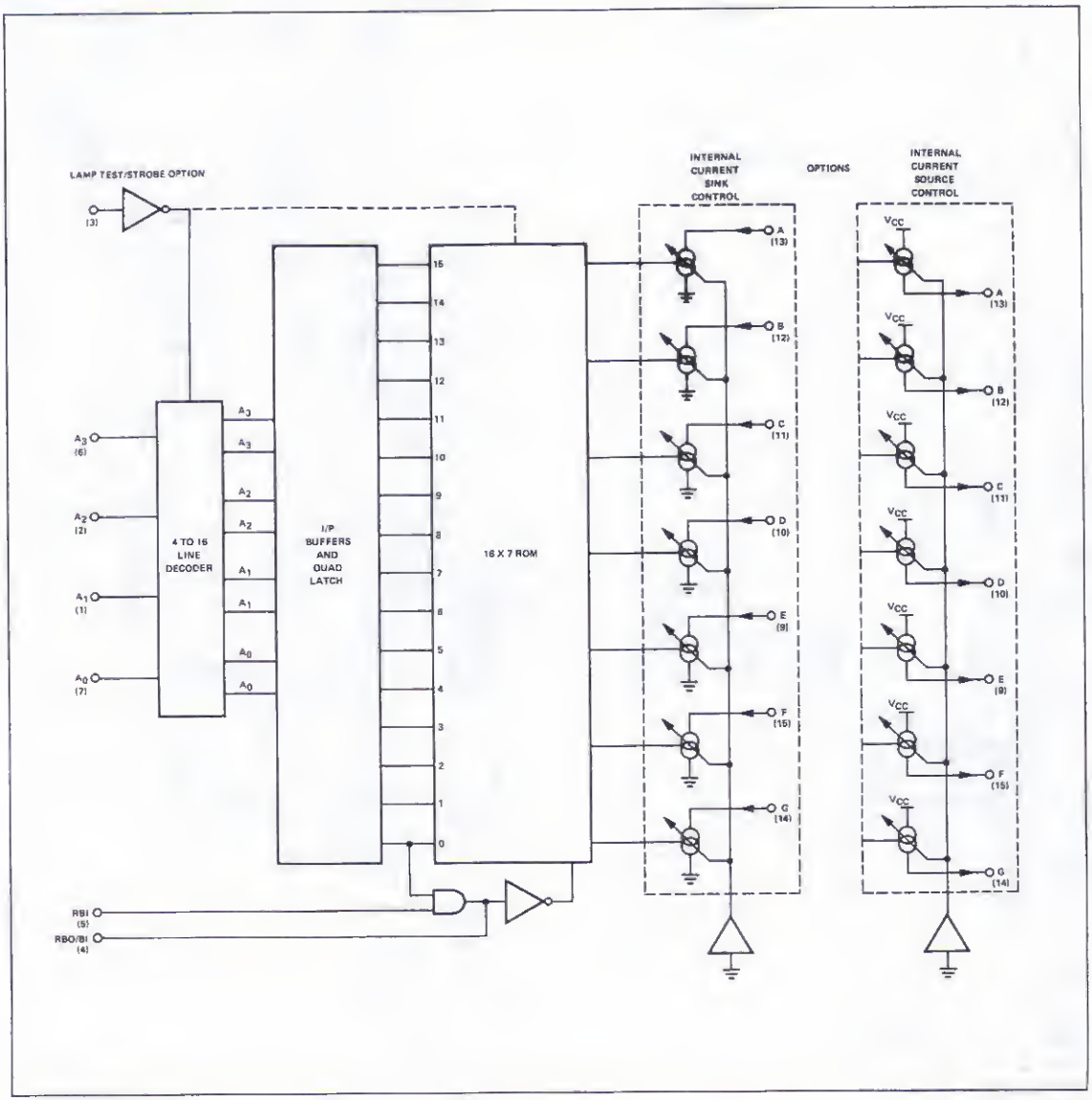
The low current PNP inputs of the 8T26 make it ideally suitable for interfacing with MOS, especially since the breakdown of the bus driver PNP inputs (pin 4, 6, 9, 13) is typically above 20V.

Although many MOS devices have been made TTL compatible by using large geometry output transistors this is not always possible in high complexity custom chips such as microprocessors or complementary MOS logic. In the past interfacing had to be done with low power TTL at the cost of sacrificing speed. However, the low "0" level input current (max 200μA at 0.4V) of the 8T26 makes it possible to use a high speed logic interface.

DESCRIPTION

The 8T50 and 8T70 series of LED Drivers are designed to interface with a wide variety of LED displays. The 8T70 series includes an internal data latch to minimize external logic requirements. The 8T50 devices have a lamp test feature to test the operation of each of the LED segments.

LOGIC DIAGRAM



CONSTANT CURRENT SINK VERSIONS

NON-LATCH	LATCH
8T54 20 mA (CM 5110 Replacement)	8T74 20 mA (CM 5111 Replacement)

CONSTANT CURRENT SOURCE VERSIONS

NON-LATCH	LATCH
8T51 5 mA (CM 5112 Replacement)	8T71 5 mA (CM 5113 Replacement)
	8T75 20 mA (FSC 9368 Replacement)
8T59 50 mA (CM 5114 Replacement)	8T79 50 mA (CM 5115 Replacement)

TRUTH TABLE FOR 8T50/70 SERIES

DECIMAL OR FUNCTION	INPUTS						BI/RBO+	SINK VERSION OUTPUTS							SOURCE VERSION OUTPUTS							NOTE
	LT/ST	RBI	D	C	B	A		a	b	c	d	e	f	g	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	
11	H	X	H	L	H	H	H	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	
13	H	X	H	H	L	H	H	OFF	ON	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	
BI	H	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT/ST*	L	X	X	X	X	X	X	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	4,5

NOTES

1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input. BI should not be forced high, when inputs A,B,C,D and RBI are low.
3. When the ripple blanking input (RBI) is at a low level and the inputs A,B,C, and D are at a low level with the lamp test input (LT) high (for the 8T50 series) or when a binary zero is stored in the latches (8T70 series) all segment outputs go off and the ripple blanking output (RBI) goes to a low level (response condition).
4. When a low is applied to the lamp test input (LT) of the 8T50 series devices all segment outputs are on. The 8T70 series devices do not have a lamp test input but a strobe input instead.
5. The 8T50 series devices have a lamp test input (LT) whereas the 8T70 series devices have a strobe input (ST). Input data is directly transferred to the outputs when the strobe is low and is stored when the strobe is high.

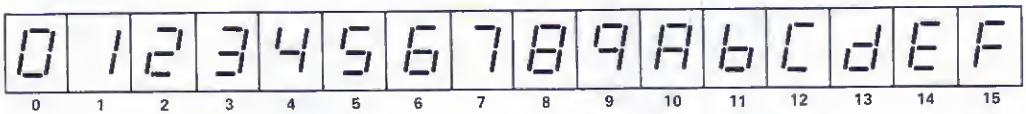
H = High Level, L = Low Level, X = Irrelevant, + BI/RBO is wired AND logic, serving as a blanking input (BI) and/or ripple blanking output (RBO) *8T50 Series has lamptest (LT) 8T70 Series has strobe (ST).

SEGMENT IDENTIFICATION

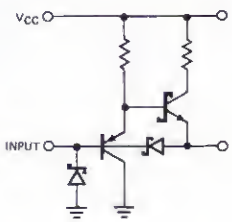
RESULTANT DISPLAY PATTERNS

SINK VERSION (8T54/74)

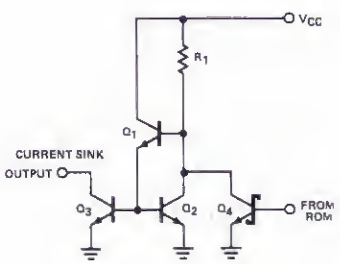
SOURCE VERSION (8T51/71; 8T75, 8T59/79)



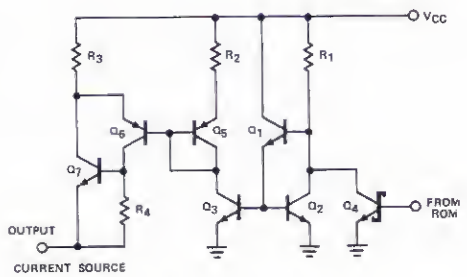
LOW CURRENT PNP INPUT STRUCTURE



CONSTANT CURRENT OUTPUT STRUCTURES



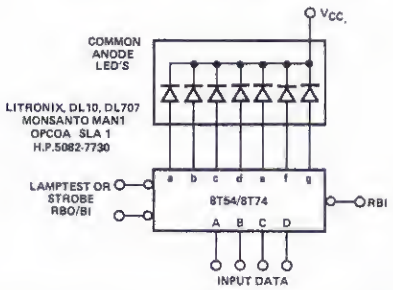
a. Current Sink Version



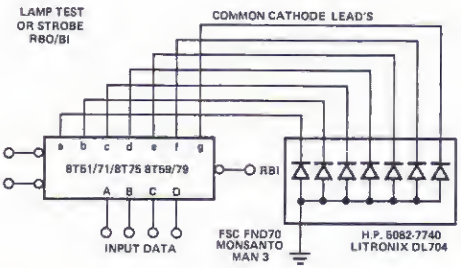
b. Current Source Version

TYPICAL APPLICATIONS OF CONSTANT CURRENT LED DRIVERS

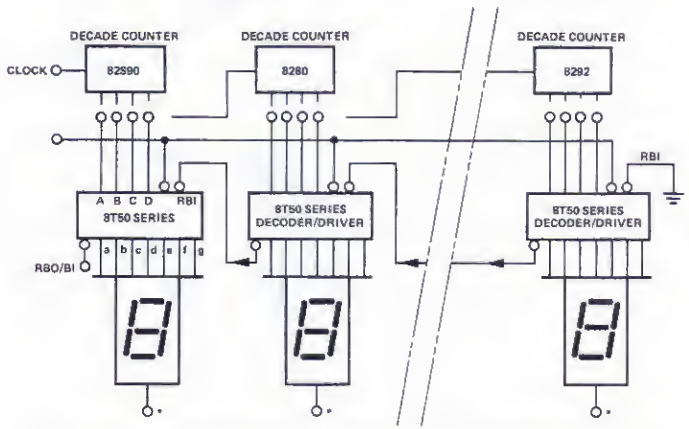
DRIVING COMMON ANODE LED'S (CONSTANT CURRENT SINK VERSION)



DRIVING COMMON CATHODE LED'S (CONSTANT CURRENT SOURCE VERSION)

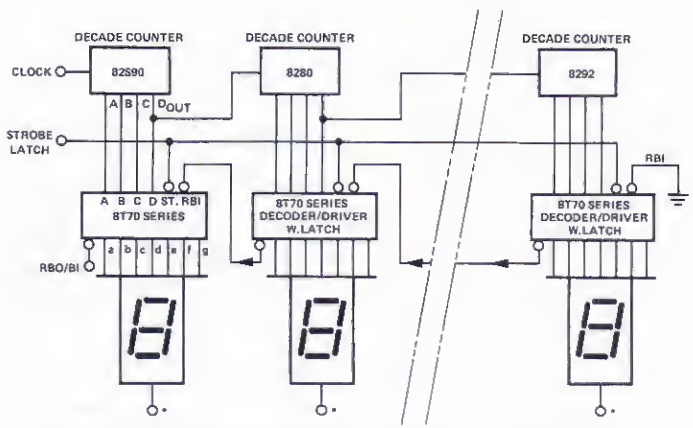


8T50 SERIES WITH LAMP TEST (LT)



*TIE TO V_{CC} FOR COMMON ANODE LED'S; OTHERWISE TIE TO GROUND FOR COMMON CATHODE LED'S.

8T70 SERIES WITH INTERNAL LATCH USED IN FREQUENCY COUNTER



*TIE TO V_{CC} FOR COMMON ANODE LED'S; OTHERWISE TIE TO GROUND FOR COMMON CATHODE LED'S.

DIGITAL 8000 SERIES TTL/MSI

8T80, 8T90 AND 8T18 INTERFACE ELEMENTS

INTRODUCTION

TTL integrated circuits must, from time to time, communicate with external circuits and input-output hardware such as relays and lamps. Typically these devices may operate at higher voltage and/or power levels. Frequently, the need also exists to transmit digital data through areas with high noise levels. Thus, there is a need for interface circuits to communicate between logic and the external environment.

The 8T80 Quad 2-input interface gate and the 8T90 Hex-interface buffer can couple low level (typically 5V and 25mW) logic to a higher level (typically 28V and 280mW). Thus, the power level has been raised by over a factor of ten. The noise susceptibility has been reduced by a factor of ten and the signal is more closely matched to the medium power output requirements. The 8T80 and 8T90 couple low level logic information out of the protected logic area and provides the buffer isolation plus the advantage of power amplification. The information can now be transmitted through the high noise environment. If a signal needs to enter or re-enter a low logic area then the process needs to be reversed. The 8T18 performs the high to low level voltage translation. The 8T18 has an extremely stable (6.5V minimum) logic threshold and can entirely eliminate up to 6.5V of noise riding on top of the information signal. Thus, the 8T18 effectively couples the high signal down to the lower level while providing digital threshold noise separation and buffer isolation.

The 8T80 and 8T90 schematic and logic diagram are shown in Figure 1. These devices provide translation from TTL logic signals to high voltage output transistors. The input structure is a multiple emitter input transistor with only one input for the 8T90. The bare collector outputs permit a wide variety of loads to be used and, in addition, they facilitate paralleling of two or more devices to perform collector logic or driving higher current loads. The LV_{CO} voltage for the outputs is tested to be greater than 40 volts and this limit should not be exceeded even on a transient basis.

8T80 AND 8T90 SCHEMATIC AND LOGIC DIAGRAM

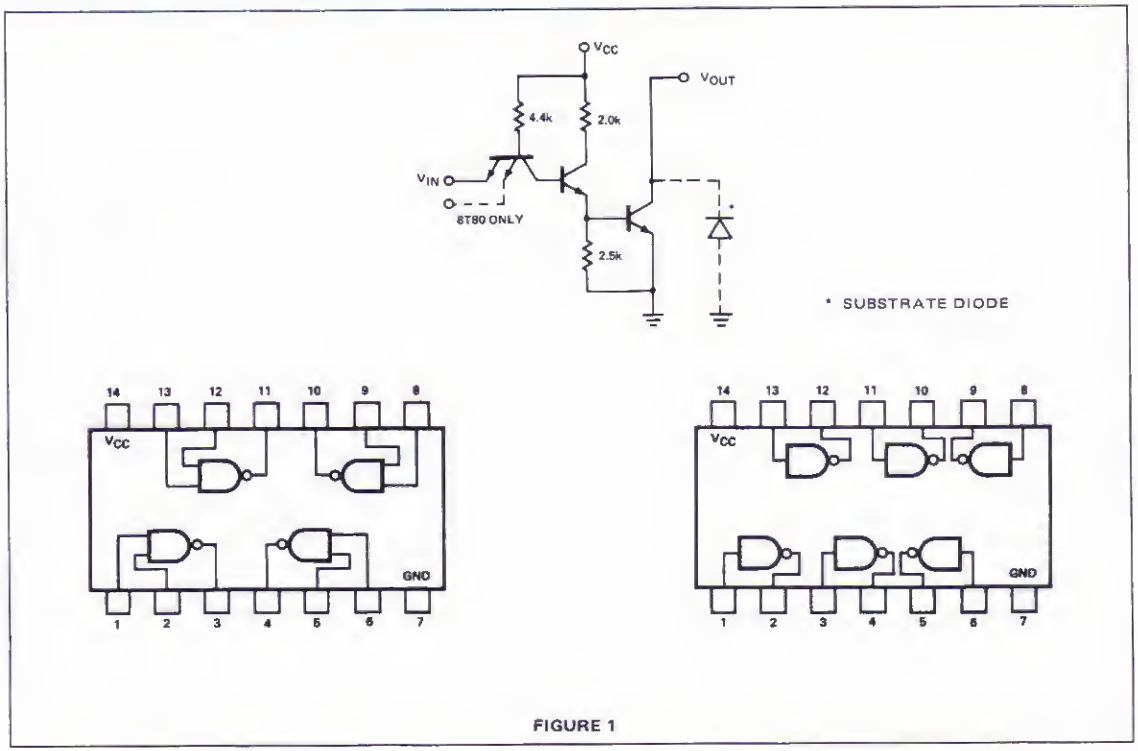
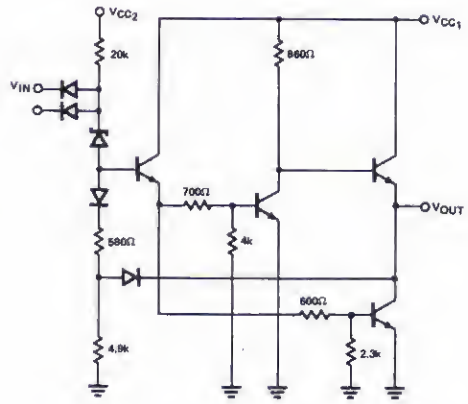


FIGURE 1

8T18 SCHEMATIC AND LOGIC DIAGRAM



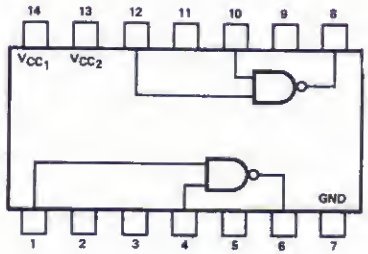


FIGURE 2

The 8T18 interface element complements the 8T90 in performing the opposite translation from high level to low level signals. Figure 2 shows the schematic and logic configuration. The terminal V_{CC_2} is returned to a power supply of 15V or more. If the V_{CC_2} voltage exceeds 30V a series current limiting resistor (limit current <2mA) or a shunt 20 to 30V Zener diode must be used. The input diodes are rated at 50V reverse breakdown. If input signals exceed or equal 50V, another diode must be added externally in series to protect the internal diodes from breakdown. An important fact about the 8T18 is that its threshold voltage (typically 7.4 to 7.8V) is independent of temperature. The various junctions being equal in number and opposite in polarity. Thus, the 8T18 is an accurate high level threshold detector.

APPLICATIONS
HIGH LEVEL BUFFER INTERFACE

The most general application for the 8T80/90 and 8T18 interface is as buffer elements to provide isolation between low level integrated circuit logic and the high level noisy outside world. The most common causes of output to input noise are shown in Figure 3. In Figure 3a, logic is being transmitted to a typical electromechanical device such as a typewriter, tape punch, printer, tape reader, etc. The electromechanical device frequently will have high energy solenoids, SCR, etc., that tend to generate a noise voltage between the logic ground and the device ground. Logic output lines are well isolated from the internal logic because the 8T90 and 8T18 are used.

Note that the 8T90 collector pull-up resistor is connected at the receiving end (i.e., near the 8T18). This helps to lower the 8T18 input impedance. Since there is no connection back into the logic area (even the power supply is isolated) the collector noise is not coupled into the low level logic. The most critical interface is the connection from the electromechanical device or transmitting end into the low level logic area. Here the noise source is in series with signal and looks directly into the logic input circuitry. Without the 8T18 high threshold buffer element, the noise would only have to overcome the normal 1 to 2V threshold to cause false inputs. However, the 8T18 has an input threshold guaranteed to be at least 6.5V worst case and conducted noise spikes up to 6.5V will not cause false inputs.

COMMON SOURCES OF NOISE

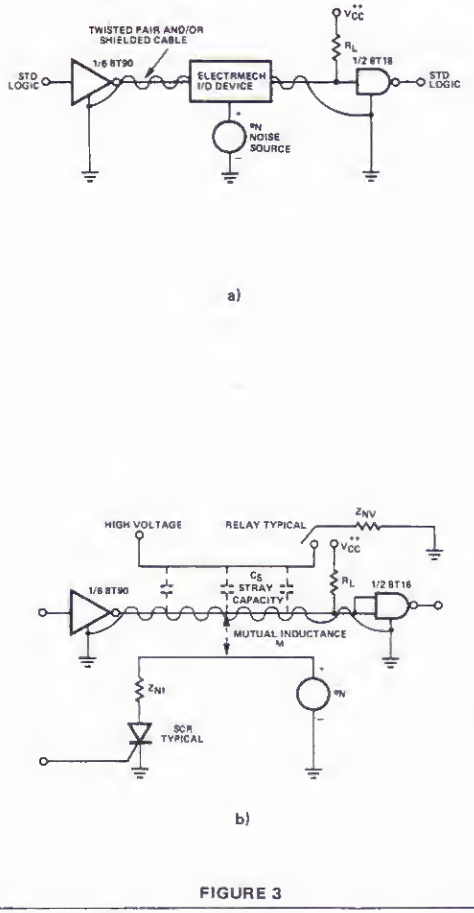


FIGURE 3

Figure 3b depicts an application where one logic area is connected to another logic area. The distance between the two areas may be as much as one hundred feet or more and may pass through areas of high electric and magnetic fields. The magnetic and electric fields plus conduction are responsible for almost all noise coupling, but seldom is electromagnetic radiation the source of noise coupling. The electric field couples via stray capacitance and Figure 4 shows the stray capacitance coupling noise from a voltage source e_n. The noise source could be a voltage being switched by relays, or any potential varying rapidly in time with respect to ground which will couple some voltage into the signal line via the stray capacity.

ELECTRIC FIELD COUPLING

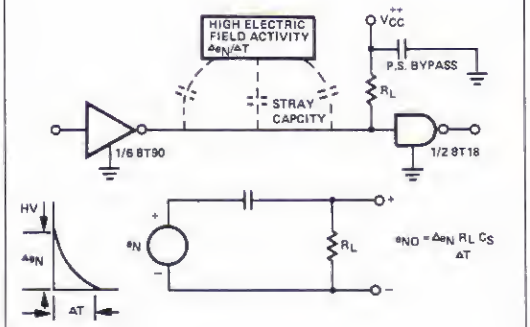


FIGURE 4

The stray capacity can be minimized by separating signal line physically apart from potential varying circuits and by shielding. Some stray capacitance will remain, however, and the voltage coupled can be approximated by

$$e_{no} = \frac{\Delta e_n R_L C_S}{\Delta T}$$

Where Δe_n is the change in potential, R_L is the logic load resistor (8T90 collector pull-up resistor), C_S is the residual stray capacity, and ΔT is the time it takes the voltage to change.

The noise is coupled during the logic "1" level. During the logic "0" level, R_L is shunted by the 8T90 collector saturation resistance.

Considering the example in Figure 5, the logic signal line is run in the proximity of a high voltage line that is switching 10mA by a relay. A switch speed limiting network consisting of a 150 ohm resistor and a .0067μF capacitor has been added to slow the switching speed and has a time constant of 1μs.

Given the following information:

e_n = 150V
T = 150 X 0.0067 X 10^{-6} = 1μs
e_{no} = 6.5V max. permissible
R_L = 1.9K min. at 28V

EXAMPLE ELECTRIC FIELD COUPLING

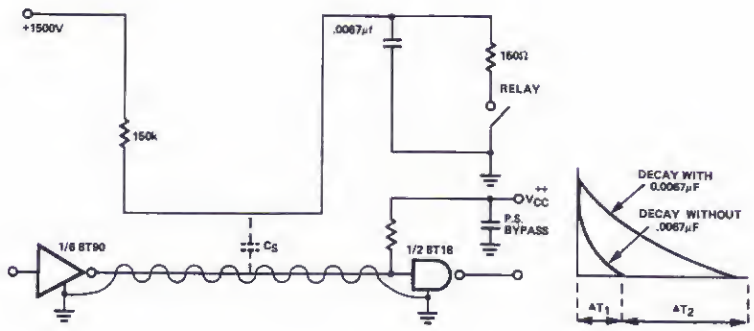


FIGURE 5

The maximum permissible stray capacitance is:

$$C_S = \frac{6.5 \times 10^{-6}}{1.5 \times 10^2 \times 1.9 \times 10^3} = 23pF$$

Good layout techniques will easily hold the stray capacitance below this value.

The above example illustrates the mechanism of electric field interference coupled into signal lines and the techniques used to minimize the coupling. In summary, the following action will minimize electric field coupling:

1. Minimize stray capacitance C_S
   (a) Avoid bringing signal lines close to conductors with varying potentials.
   (b) Use as much shielding as is economically feasible.
2. Slow rate of electrostatic field collapse, ΔT, by use of networks as shown in the example.
3. Hold the resistive impedance, R_L, as low as practically feasible.
4. Use the high threshold gate, 8T18, to provide the highest possible voltage margin.

To understand the mechanism of inductive noise coupling into the logic lines consider the circuit in Figure 6a. All circuits must have self inductance just as all circuits must have capacitance. There exists then some mutual inductance between the signal circuit and the current noise source I_n. Mutual inductance is defined as:

$$M = k\sqrt{L_S L_N},$$

MAGNETIC FIELD COUPLING

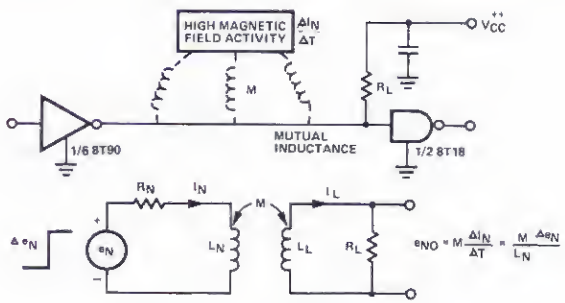


FIGURE 6

Where k is the coefficient of coupling and L_S and L_N are the signal and noise circuit self inductances. The best defense against noise is to keep the mutual coupling low. The coefficient of coupling is reduced by using twisted pair wires and magnetic shielding of both the noise circuit and the signal circuit. The self inductances are minimized by using twisted pairs and the largest wire size economically feasible. A simplified equivalent circuit is shown in Figure 6b. Note that the induced voltage due to inductive coupling appears only during the "0" level. During the "1" level, R_L is in series with the off resistance of the 8T90. The analysis assumes that the mutual inductance is very much smaller than the self inductances. The result indicates that the induced voltage is directly proportional to the current switched, the mutual coupling and inversely proportional to the time taken to switch. Written in another form the equation indicates that the induced voltage is proportional to the mutual inductance divided by the noise circuit's self inductance times the voltage being switched. Note that the induced voltage is not a function of R_L, the signal lead resistive impedance. From these equations, one can summarize the following:

1. Keep signal lines physically separated (reduce coefficient of coupling or mutual inductance).
2. Minimize the signal inductances by using largest practicable wire size and using twisted pair or coax where necessary.
3. Slow down the current switching rate T (e.g., insert charging reactors thereby increasing L_N).
4. Use the high threshold logic element 8T18 to increase noise margin.

TYPICAL OUTPUT VOLTAGE VS. OUTPUT CURRENT

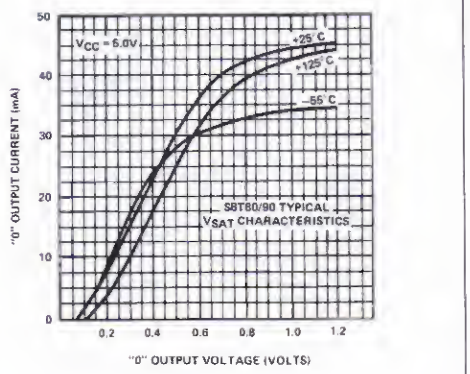


FIGURE 7

ALL PURPOSE DRIVER

The 8T90 is the most versatile integrated circuit device for output interface applications in the 8000 family. To utilize the element to its utmost capability, some understanding of the limitations of output voltage and current are necessary. A curve of typical output current versus saturation voltage and temperature is shown in Figure 7. The driver current rating at a specific operating point is given in the data sheet. However, if other operating points are desired, then the curve of Figure 12 indicates output currents expected versus saturation voltages. In designing for maximum current rating the maximum device dissipation rating of 310 milliwatts at 125°C must not be exceeded for the dual-in-line silicone A package.

This figure was arrived at by substituting design data into the relationship:

$$T_{j\,max} = T_A + P_{max} \times \Theta_{J\text{-}A}$$

Where:

T_j max = max. allowable junction temperature (175°C for A package)

T_A = ambient temperature

P_{max} = maximum allowable power dissipation

$\Theta_{J\text{-}A}$ = junction to ambient thermal impedance (0.16°C/mW for A package)

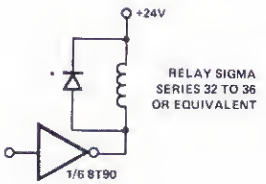
Since each gate draws 20mA from the V_{CC} power supply when turned on with zero collector current, the total available collector power dissipation can be calculated. If all six inverters are on at the same time, the IC is dissipating (6 X 20) = 120mW and 310mW – 120mW or 190mW are available for collector circuit dissipation at 125°C before thermal considerations become important.

RELAY DRIVER

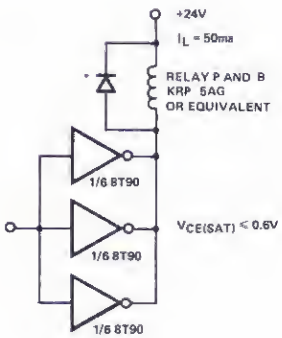
Figure 8 shows the 8T90 used in a relay driver application. The free wheeling diode is used to dissipate the energy stored in the relay inductance. When the relay is released the 8T90 collector current is diverted through the IN3064 diode, thereby restricting the induced voltage. Due to the three transistor TTL structure of the 8T90 (Figure 1), the reverse transfer is negligible and noise existing on relay wiring, etc., will not be coupled back into the logic. Thus, the inverter performs the function of interfacing and provides buffer isolation.

In Figure 8a, a low power relay is driven by a single inverter stage. In Figure 8b, three drivers are paralleled to drive a 10 ampere double throw general purpose relay. The expected saturation voltage is less than 0.6V and the total dissipation in the three circuits is 3 X 20 + 30 = 90 milliwatts, below the total power dissipation capability.

8T90 RELAY DRIVER APPLICATION



a.



b.

* Diode IN 3064

FIGURE 8

LAMP DRIVER

Another application of the 8T90 Hex Inverter is as an incandescent lamp driver shown in Figure 9. For lamps requiring less than 20mA drive, one driver is sufficient but if more current is required, drivers may be paralleled. Since the output transistors are beta-limited as illustrated in Figure 7, the inrush-current restrictions are not severe because a natural current-limiting effect will take place in the output transistors.

8T90 LAMP DRIVER APPLICATION

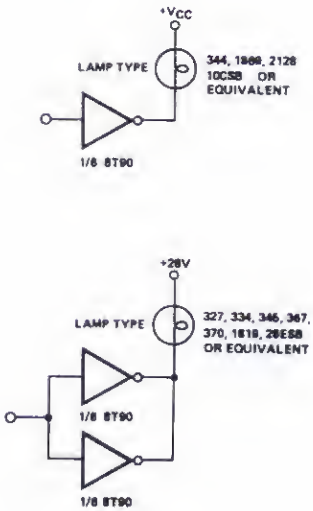


FIGURE 9

MILLER INTEGRATOR

The 8T90 may be used as a Miller integrator. The basic circuit is shown in Figure 10. The down ramp is independent of the load resistor R_L. This circuit is valuable for use as an integrator for lamp circuits and in general slowing down the output driver. The ramp can be approximated as shown in Figure 10.

BASIC INTEGRATOR CIRCUIT

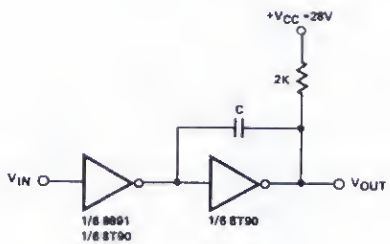


FIGURE 10

BASIC INTEGRATOR CIRCUIT (Cont'd)

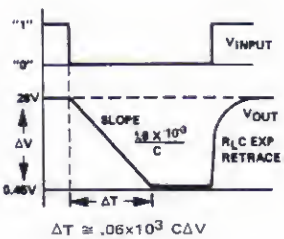


FIGURE 10 (Cont'd)

8T80 QUAD GATE INTERFACE ELEMENT

The 8T80 is a quad 2-input NAND gate whose output structure and drive capability is identical to that of the 8T90. Since there are two less stages per package the 8T80 can dissipate proportionately more power per stage relative to the 8T90. Figure 11 shows some latching-driver applications of the 8T80.

8T80 QUAD GATE APPLICATIONS

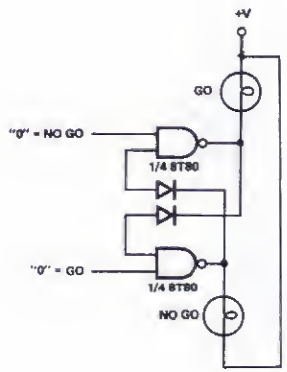
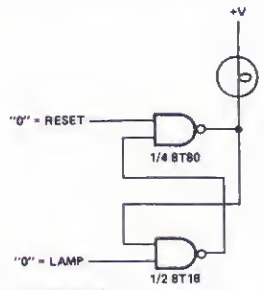


FIGURE 11

8T80 QUAD GATE APPLICATIONS (Cont'd)



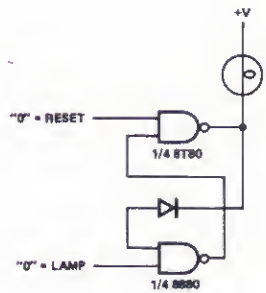
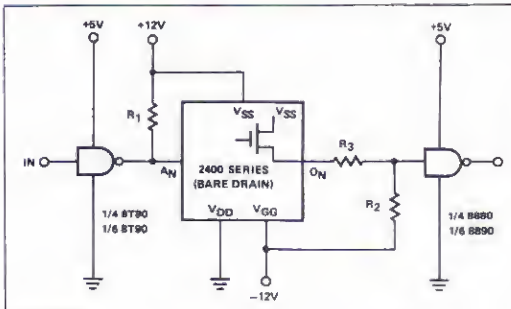


FIGURE 11 (Cont'd)

TTL–MOS–TTL INTERFACE

To interface with metal gate MOS circuits the 8T80 and 8T90 are very useful since output swings of 12V can be easily accommodated. To translate from the MOS output to TTL only a standard 8880 gate is needed. An application is shown in Figure 12.

TTL–MOS–TTL INTERFACE



NOTES:
1. R_1 may range from 680Ω to 33K, typically 3.3K is satisfactory.
2. R_2 6.8K for a standard TTL (I_0 IN = 1.6mA)
3. R_3 = 2.2K

FIGURE 12

POSITIVE TO NEGATIVE VOLTAGE TRANSLATOR

The 8T18 high-to-low voltage interface elements work perfectly in this application if the following connections are made: ground to a -5V ± 5% supply, V_{CC1} to ground and V_{CC2} to a +15V ± 5% supply for -55°C to +125°C operation or V_{CC2} to a +10V ± 5% supply for -25°C to +125°C operation. See Figure 13a. Thus, the designer has the capability of going from +5V supply digital systems such as TTL or DTL to -5V supply systems. An external PNP can be added to the output permitting large voltage swings (Figure 13b).

POSITIVE TO NEGATIVE VOLTAGE TRANSLATOR

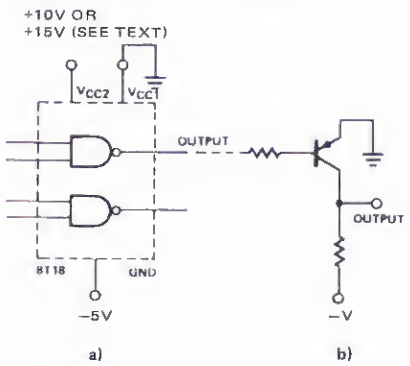


FIGURE 13

The 8T80 and 8T90 can be used to translate from negative to positive voltage logic systems as shown in Figure 14. The inputs to the 8800 gates have diffused input clamping diodes to limit negative input excursions.

NEGATIVE TO POSITIVE VOLTAGE TRANSLATOR

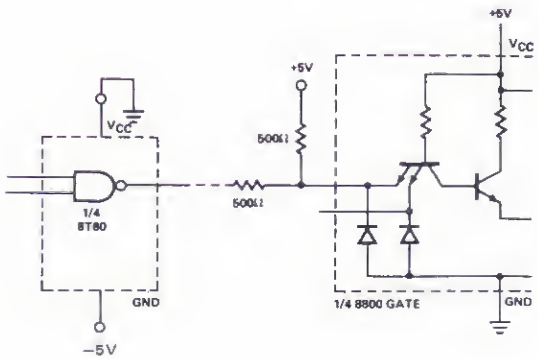


FIGURE 14

DIGITAL 8000 SERIES TTL/MSI
DUAL ZERO-CROSSING DETECTOR

APPLICATIONS

- ZERO-CROSSING DETECTOR
- HIGH STABILITY ONE-SHOT
- BI-DIRECTIONAL ONE-SHOT
- FREQUENCY DOUBLER
- STABLE-LOW FREQUENCY OSCILLATOR
- LINEAR AMPLIFIER
- FREQUENCY TO VOLTAGE CONVERTER

INTRODUCTION

The 8T363 is a monolithic dual zero-crossing detector, consisting of a differential amplifier input and a TTL compatible output. The input amplifier is referenced to zero volts and employs temperature compensation to ensure stable thresholds. Low level analog waveforms may be converted to digital signals as long as they exceed ±30mV, the input uncertainty region.

As shown in Figures 1 and 2, the 8T363 operates from two power supplies. These may be +5V, −6V and ground or +5V, −12V and ground. In the −6V configuration, the −12V pin must be tied to the −6V pin. When used in the −12V configuration, the −6V pin must be left open. The −6V and −12V terminals must never be connected simultaneously, or the internal zener diode will be destroyed.

LOGIC DIAGRAM AND PIN-OUT

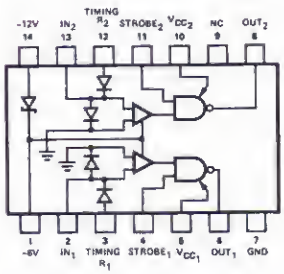
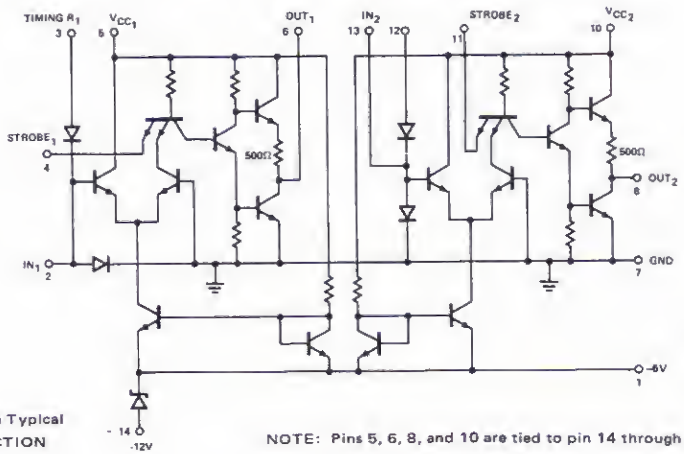


FIGURE 1

DUAL ZERO-CROSSING DETECTOR



Component Values are Typical
PIN 3 — NO CONNECTION

NOTE: Pins 5, 6, 8, and 10 are tied to pin 14 through isolation diodes.

FIGURE 2

ZERO–CROSSING DETECTOR

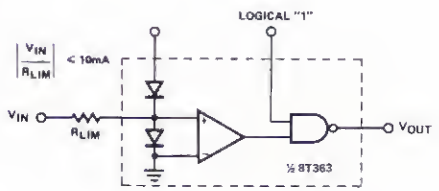
An application of the 8T363 as a zero-crossing detector is shown in Figure 3a. Since the device is internally referenced to ground, the output changes state each time the analog input signal passes through zero. The input signal is therefore converted into a TTL compatible square wave as illustrated in Figure 3b.

This "infinite" clipping of the input signal virtually eliminates distortion caused by amplitude fluctuations and noise. Further data processing is simplified through the use of digital techniques.

FREQUENCY DOUBLER

A variation of the zero-crossing detector is a circuit that produces a pulse every time the input signal pulses through zero. The result is a frequency-doubler as shown in Figure 4a. The duration of the pulse is determined by the time required to pass through the threshold limits which can be calculated from the equations below. This circuit will not work with square wave inputs having fast rise and fall times because there is not enough time between thresholds for the 8T363 to respond. Figure 4b shows the pulse train resulting from a sine wave input.

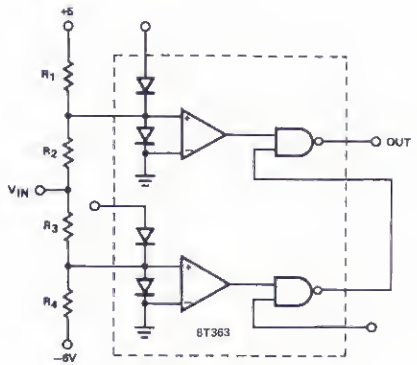
ZERO CROSSING DETECTOR



a

FIGURE 3

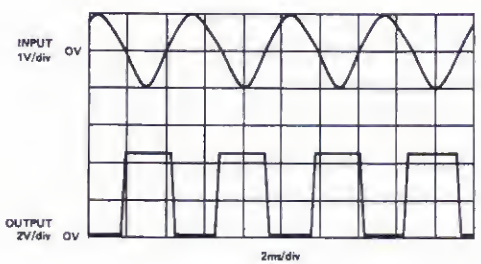
FREQUENCY DOUBLER



a

FIGURE 4

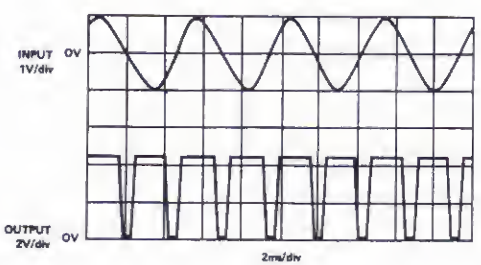
INPUT AND OUTPUT WAVEFORMS OF ZERO CROSSING DETECTOR



b

FIGURE 3

WAVEFORMS FOR FREQUENCY DOUBLER



b

FIGURE 4

Positive and negative thresholds for the frequency doubler are defined as follows:

Positive Threshold (V_{THpos})

$$V_{THpos} = \frac{0.03\,(R_3 + R_4)}{R_4} - \frac{(V^-)\,R_3}{R_4}$$

Negative Threshold (V_{THneg})

$$V_{THneg} = \frac{0.03\,(R_1 + R_2)}{R_1} - \frac{V_{CC}\,R_2}{R_1}$$

with these limits:

$$\frac{V_{(1)in}}{R_2} \leqslant 10mA, \quad \frac{V_{(1)in}}{R_3} \leqslant 10mA,$$

and a bias current $I_B = \dfrac{V_{CC} - (V^-)}{R_1 + R_2 + R_3 + R_4} > 200\mu A$

Example: For $R_1 = 24K\Omega$, $R_4 = 30K\Omega$, $R_2 = 1K\Omega$, $V_{CC} = 5V$, $R_3 = 1k\Omega$, $V^- = -6V$

$$V_{THpos} = \frac{0.03\,(31K\Omega)}{30K\Omega} - \frac{(-6V)\,1K\Omega}{30K\Omega} \cong 0.23V$$

$$V_{THneg} = \frac{0.03\,(25K\Omega)}{24K\Omega} - \frac{(-6V)\,1K\Omega}{24K} \cong -0.24V$$

$$I_B = \frac{5V - (-6V)}{24K\Omega + 1K\Omega + 1K\Omega + 30K} = \frac{11V}{56K\Omega} \cong 200\mu A$$

HIGH STABILITY ONE–SHOT

A one-shot that is insensitive to temperature and supply voltage variations may be implemented using 1/2 8T363 zero-crossing detector and 1/4 8T380 Schmitt-Trigger. The circuit implementation is illustrated in Figure 5. Output pulse width (t_w) may be calculated as follows:

$t_{w(sec)} = 0.69\,R_2C_1$ where: R in ohms
C in farads
R_2 max. ≅ 50KΩ
C_1 may be polarized as shown

HIGH STABILITY ONE-SHOT

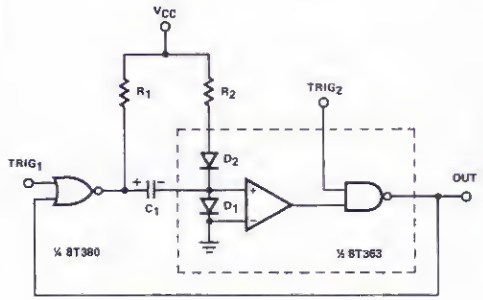


FIGURE 5

Until the logic "1" level is reached, the recovery time of the one-shot is determined by the internal current-limiting resistor of the 8T380 Schmitt Trigger. From the output "1" level to V_{CC} the recovery time is determined by the combination of R_1 and C_1. To initiate the one-shot timing period, a positive-going level must be applied at $Trig_1$ with the $Trig_2$ input disabled (logical "1"). A negative-going logic level at $Trig_2$ with $Trig_1$ disabled (logical "0") will have the same effect. Although the circuit will operate with shorter trigger pulse widths due to the overdrive conditions, conservative design practices require 75ns pulse widths.

When the output of the 8T380 is high, the capacitor charges from V_{CC} through R_1, C_1 and diode D_1 to ground (Figure 6). The voltage drop across D_1 causes the input of the 8T363 to be high. With $Trig_2$ input high, the output of the 8T363 will be low.

CHARGE PATH DURING RECOVERY TIME

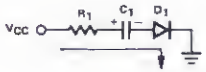


FIGURE 6

The timed period is initiated when the output of the 8T380 NOR-gate is forced low. When the NOR-gate's output saturates, the negative-going transition causes a similar transition at the input of the 8T363. The resulting negative voltage at the input causes the output of the 8T363 to go high. This signal is returned to the input of the 8T380 to hold its output low until the timed period is ended. The capacitor charges from $-(V_{CC} - V_{D1} - V_{CE(sat)})$ to $+(V_{CC} - V_{D2})$ through R_2, C_1 (Figure 7). When the 8T363 input voltage has reached 0V, the output goes low and the timed period ends.

CHARGE PATH DURING TIMED INTERVAL

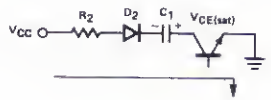


FIGURE 7

The pulse width stability is better than 1% because the threshold of the 8T363 is centered between the extremes of the voltage, independent of V_{CC}. Since the diode drops V_{D1} and V_{D2} are matched because of monolithic construction, the pulse width stability is also relatively independent of temperature.

Figure 8 shows the calculated charging curve of capacitor C_1 (dotted). The measure voltage at the input of the 8T363 is shown by solid lines in the same figure.

WAVEFORM AT INPUT OF 363

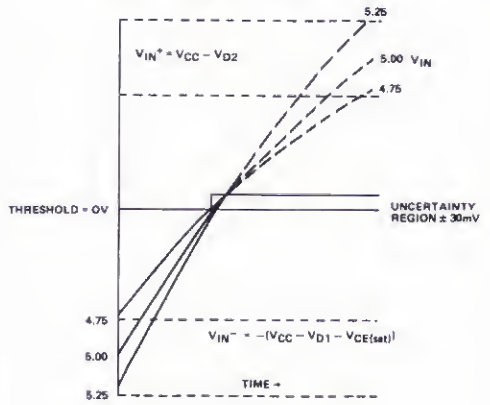


FIGURE 8

BI–DIRECTIONAL ONE–SHOT

A variation of the one-shot circuit which will produce a pulse each time the input changes state is shown in Figure 9. In this circuit, each half of the 8T363 functions as a one-shot, however one half triggers on a positive-going input and the other half triggers on a negative-going input. The outputs of the one-shots then go to a NOR Schmitt Trigger which produces an output pulse each time any one of the inputs goes to a high level. As in the previous example, output pulse width (t_w) is calculated as:

$$t_w = 0.69\ R_2C_1$$

BI-DIRECTIONAL ONE-SHOT

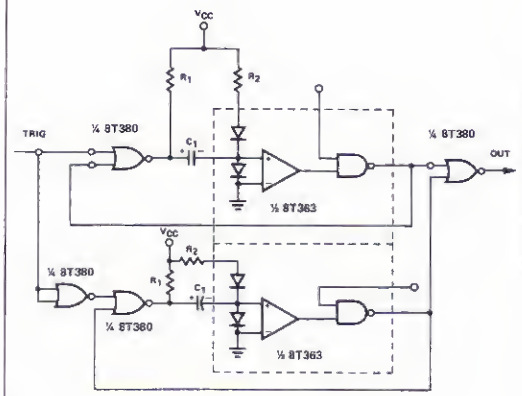


FIGURE 9

LOW FREQUENCY OSCILLATOR

Due to its stable thresholds and high input impedance, the 8T363 performs well as a low frequency oscillator. The circuit shown in Figure 10 requires one half of an 8T363 and two 380 NOR-gates.* The frequency is determined by R_1 and C_1 and may be calculated by the approximate formula below. Using a 100KΩ resistor and a 1μf capacitor, a frequency of about 5Hz can be obtained.

* SIGNETICS UTILOGIC II SERIES

$$f_o \cong \frac{1}{2\tau} \qquad \tau = R_1C_1$$

where: $R_1 \leqslant 100K$

LOW FREQUENCY OSCILLATOR

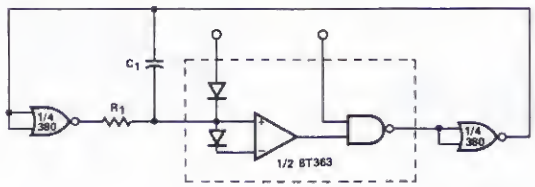


FIGURE 10

FREQUENCY TO VOLTAGE CONVERTER

A practical method of detecting a frequency modulated (FM) signal using a pulse counting discriminator, is possible using two integrated circuits. No inductors are required for this design.

The circuit diagram of the FM detector, or as it is sometimes called a Frequency to Voltage converter, is shown in Figure 11. A variable input frequency up to 2MHz is applied through a current limiting resistor to one half of the 8T363, which acts as a limiter. The output drives a one-shot which is the other half of the 8T363 input. Constant width output pulses are obtained at a rate determined by the input frequency. The timing resistor is adjusted to give the best linearity for the input frequency range.

FREQUENCY TO VOLTAGE CONVERTER

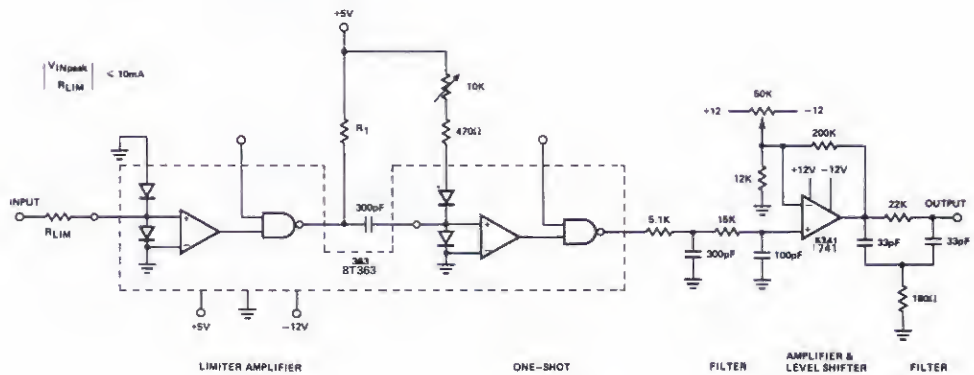


FIGURE 11

The original signal may now be recovered by passing the constant width pulses from the 8T363 through an RC filter network. Since the demodulated signal is superimposed on an average positive DC level, an operational amplifier, 741, is used to level shift and amplify the demodulated signal. A 50KΩ potentiometer nulls the average positive DC level which is well within the common mode range of the 741. The output of the amplifier is the demodulated signal amplified and restored to an average DC level of OV. To attenuate the remaining carrier components, the output is filtered through a bridge-T network.

When used as an FM discriminator with a carrier frequency of 1.5MHz and a deviation of ± 80KHz, the system has a 3db Bandwidth of 5Hz to 35KHz. Distortion at 1KHz is less then 1%. Figure 12 shows a comparison of the modulating signal and the signal recovered at the output of the frequency to voltage converter.

COMPARISON OF MODULATING SIGNAL AND RECOVERED SIGNAL

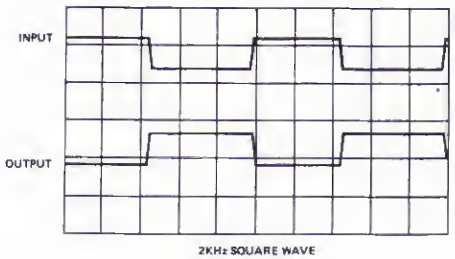


FIGURE 12

LINEAR AMPLIFIER

Since the 8T363 has a differential input stage, it performs well as a small signal linear amplifier. By creating feedback through R_1 as shown in Figure 13, the 8T363 will bias itself in the linear region. A small offset bias must be applied to the input through R_3 to level shift the output since the output cannot swing below ground. Resistor R_3 should be adjusted for a quiescent output level of about 2V. The gain of the amplifier is then determined by the resistor ratio $\frac{R_1}{R_2}$

LINEAR AMPLIFIER

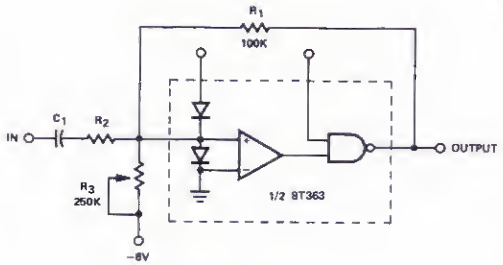


FIGURE 13

8200 MSI Functional Index

INTRODUCTION

A shift register consist of an arbitrary number of flip-flops which are used primarily for temporary storage of digital data. There are four basic shift register classifications: (1) serial input to serial output, (2) serial input to parallel output, (3) parallel input to serial output, and (4) parallel input to parallel output, or buffer registers. Buffer registers may be divided into two categories: (a) clocked flip-flop elements, and (b) strobed latch flip-flops. All the registers to be discussed are produced from D-type flip-flops. The binary level ("1" or "0") present at the D or Data input appears at the true (Q) output upon activation of the CLOCK or STROBE.

The MSI shift and buffer registers to be discussed in this note will be: the 8270 and 8271, 4-Bit Universal Shift Registers, the 8276 Serial Input to Serial Output 8-Bit Shift Register*, the 8200, 8201, 8202 and 8203 10-Bit D-type Clocked Buffer Register, and the 8275 D-Type Strobe Quadruple Bistable Latch. Some specific applications are mentioned in the latter part of this note.

8270 AND 8271 4-BIT UNIVERSAL SHIFT REGISTER

The 8270/8271 is a 4-bit serial and parallel synchronous entry shift register with serial and parallel outputs. Figures 1 and 2 illustrate the logic diagram and circuit diagram, respectively. The buffered LOAD and SHIFT inputs control the four input AND-OR-INVERT gates of the 8270/8271 permitting either serial or parallel data to be synchronously entered on the falling edge of the Clock, as shown in Table 1. There are four modes of operation: (1) the 8270/8271 will store information (2) parallel information will be synchronously entered, (3) serial data will be shifted to the right. It is impossible to cause a malfunction while changing modes of operation.

In addition to the 8270 features, the 8271 provides the not-true output for the fourth stage (D_o) and a common asynchronous RESET input (R_D). While RESET is activated, the CLOCK and control inputs are completely inhibited internally.

THE EFFECTS OF LOAD AND SHIFT INPUTS TO THE 8270/8271

LOAD	SHIFT	OPERATING MODE
0	0	Store (with clock running)
1	0	Synchronous parallel load
0	1	Shift right
1	1	Shift right

TABLE 1

LOGIC DIAGRAM

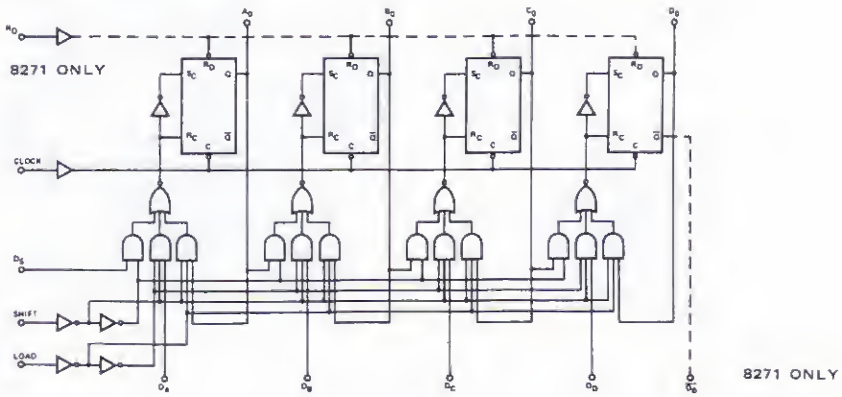


FIGURE 1

*A Dual 8-Bit Shift Register, the 8277 is also available.

CIRCUIT DIAGRAM (8270/8271)

8270/8271

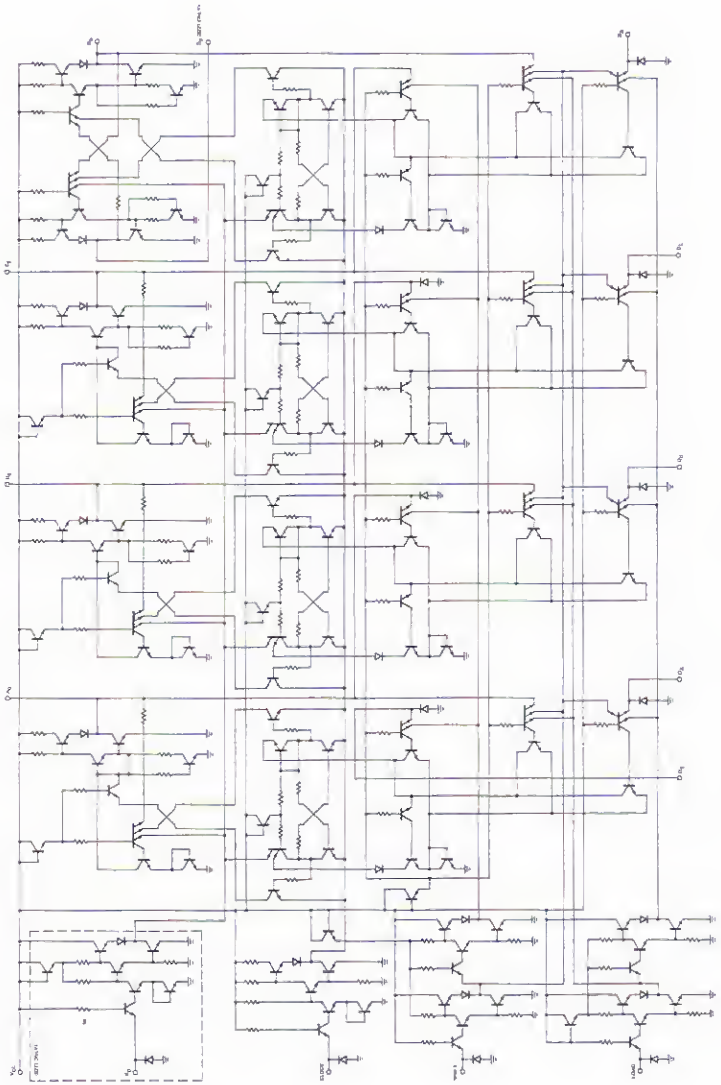


FIGURE 2

SYSTEM IMPLEMENTATION

Many system malfunctions will be precluded by conservative of V_{CC} to GROUND bypassing. Each 8270/8271 should have at least 0.01μF of ceramic disc capacitance located as near to the package as possible from a practical standpoint.

SIGNAL PROCESSING/CLOCK INPUT REQUIREMENTS

The clock pulse width should be greater than 20ns at the 1.5 volt level. The 8270/71 shift registers are designed to be level sensitive at the clock input. However, for reliable system operation rise and fall times greater than 1 μs are not recommended.

The 8270/71 has a diode clamp on the clock input and is immune to negative going noise pulses which might otherwise cause a system malfunction.

The control inputs, LOAD and SHIFT, should be driven from a low impedance source in order to maintain good noise immunity. A low impedance source can be V_{CC}, GROUND or an 8000 series gate, or equivalent. If a function such as shift right (Mode 3) is desired, the SHIFT input should be tied to V_{CC}, and the LOAD input can be connected to V_{CC} or GROUND. The RESET input (R_D) of the 8271 should be tied to V_{CC} (if unused) or driven by a DTL/TTL gate. The data inputs (D_S, D_A, D_B, D_C and D_D) should also be tied to a low impedance when in use or when unused, may be left open. However, conservative design techniques dictate that all inputs to an MSI device must be connected to a low impedance source at all times. This precaution eliminates the possibility of having noise capacitively coupled onto the highly complex MSI array through an open input terminal. The logic levels at the control inputs must be present 30ns before a clocking transition to operate properly. The data inputs (D_S, D_A, D_B, D_C and D_D) should be present 15ns preceding the clock. These data inputs require 0ns hold time. After the clock falls, data is transferred to the outputs.

8276 8-BIT SHIFT REGISTER

The 8276 is a serial-input/serial-output 8-bit shift right shift register. The basic die contains eight R-S, master-slave flip-flops input gating for both TRANSFER INHIBIT and enable DATA, and an inverting clock driver. The logic diagram is shown in Figure 3.

The DATA INPUT and DATA ENABLE (inputs A and B) are inputs to the same NAND buffer and may be interchanged (see Figure 3). An internal inverter provides the complement to the first R-S binary of the shift register. Each input (A, B, CP, and I_X) is fully buffered and appears as only one TTL input load.

SIGNAL PROCESSING/CLOCK INPUT REQUIREMENTS

The internal clock driver/inverter produces a single transfer or shift of data from one bit to the next on the positive-going or rising edge of the input clock pulse.

The TRANSFER INHIBIT input is buffered, as is the CLOCK input, with an inverting driver. A "1" or high level on the TRANSFER INHIBIT line prevents the transfer of data from the master to the slave sections.

The information presented at the A and B input gate 25ns before the clock input goes high will appear at the Q output eight "0" to "1" clock input transitions later. The transfer rate or clock frequency is typically greater than 20 MHz.

SYSTEM IMPLEMENTATION

The clock driver/inverter is a classic TTL gate (as are the Q and $\overline{Q}$ output structures). Due to positive feedback paths and current spike inherent to all medium and high speed TTL structures, the clock inverting buffer will oscillate if the clock input rise and fall times are too long. These oscillations on the rising and falling edge of the clock pulse will gnerate an indeterminate number of clocking transitions. A classic symptom of this problem is the appearance of the input data at the Q output after only one or two clock pulses. If the clock input pulse has a rise and fall time of less than 200ns and an amplitude of greater than 2.6V, oscillation will not occur in the clock buffer.

The V_{CC} to GROUND bypass capacitor should be greater than 0.01μF. The DATA ENABLE input should be connected to V_{CC} when not in use. If the TRANSFER INHIBIT is not being utilized, it must be grounded. Positive or open TRANSFER INHIBIT input prevents the transfer of data.

MAXIMUM CAPACITIVE LOADING

The Q and $\overline{Q}$ outputs are buffered which eliminates a capacitive loading problem. The only consideration to output capacitance loading should be the desired rise and fall times.

LOGIC AND FUNCTION DIAGRAM (8276)

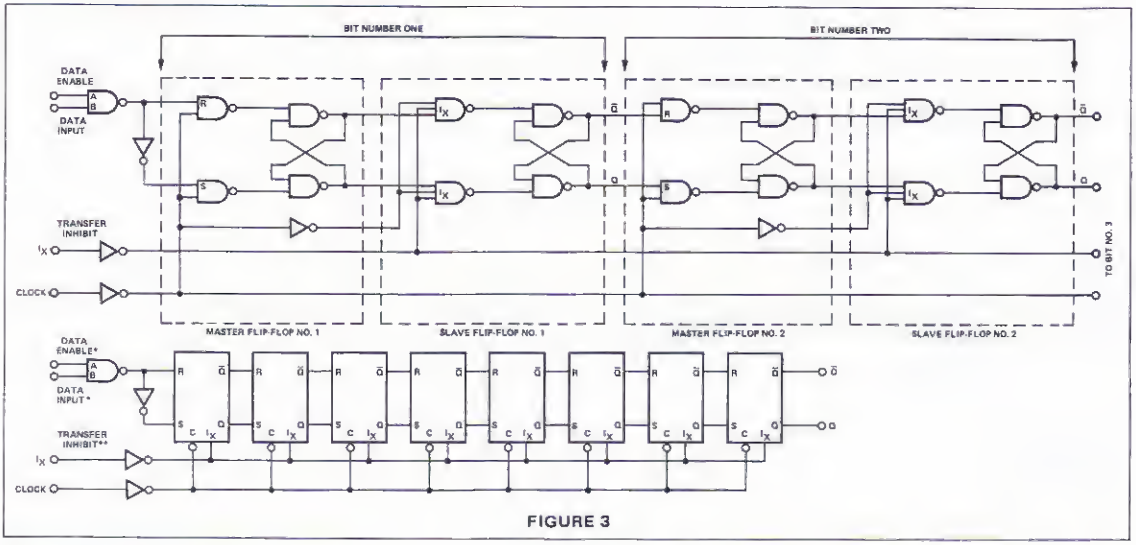


FIGURE 3

TRUTH TABLE FOR THE 8276

t_n A (Data Enable)	B (Data Input)	$t_n + 8$ Q
0	0	0
0	1	0
1	0	0
1	1	1

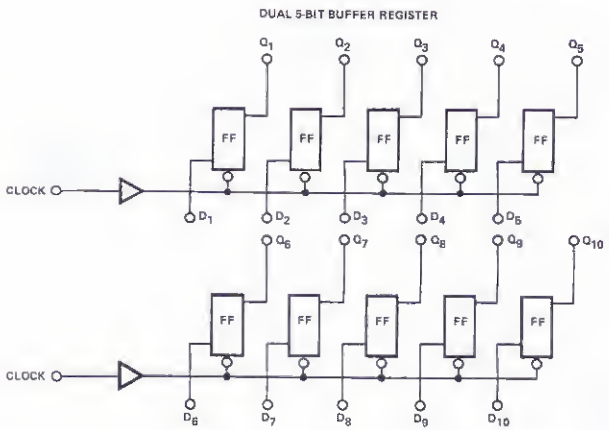
NOTES

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

8200 DUAL 5-BIT BUFFER REGISTER (D-TYPE); 8201 DUAL 5-BIT BUFFER REGISTER ($\overline{D}$-TYPE); 8202 10-BIT BUFFER REGISTER (D-TYPE); 8203 10-BIT BUFFER REGISTER ($\overline{D}$-TYPE)

Four I/O buffer registers, the 8200/8201/8202/8203, are fabricated from the same die with four metal variations. The D or $\overline{D}$ input and Q output are brought out from all ten flip-flops. All four combinations of dual 5-bit, single 10-bit, D-type and $\overline{D}$-type (D-complement) are made available. The dual 5-bit configurations have two CLOCK inputs and no reset. The single 10-bit configurations have a single CLOCK and a single RESET input driving all ten flip-flops.

8200



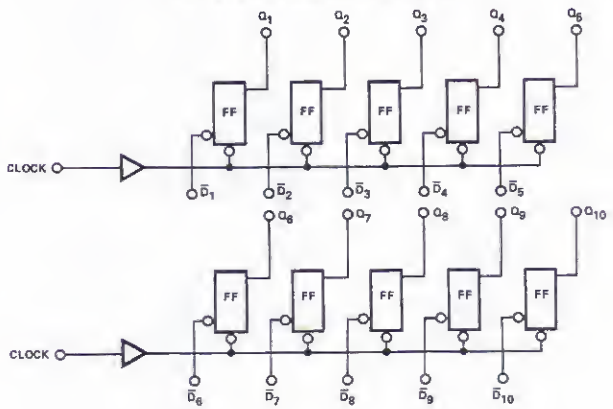
TRUTH TABLE

D_n	$Q_n + 1$
1	1
0	0

FIGURE 4

8201

DUAL 5-BIT BUFFER REGISTER—INVERTED INPUTS



TRUTH TABLE

$\overline{D}_n$	$Q_n + 1$
1	0
0	1

FIGURE 5

OPERATIONS OF THE 8200/8201/8202/8203

The logic diagrams for the 8200/8201/8202/8203 are shown in Figures 4, 5, 6 and 7, respectively. Figure 8 illustrates the composite circuit diagram of a single flip-flop with clock and reset buffers, it is a DC coupled master-slave type. The D and D-complement inputs may be interchanged depending upon the application without producing a propagation time-differential. This characteristic is made possible through the unique D/$\overline{D}$-complement gating connection in conjunction with the master latch.

When the CLOCK input is "0" the clock buffer output is "0" or less than 0.4V, and the D/D-complement inputs are locked out. This locking out of the data inputs occurs because the collectors of either the A or B transistors when turned on are held at about 1V (one $V_{CE(SAT)}$ and a diode drop). Thus, only when the clock goes high can the input (D or $\overline{D}$) control the master. The clock line, upon going low again, turns on either transistor C or D (depending on the state of the master latch) and locks out the D or $\overline{D}$ input. If C is turned on, the output (Q) goes to a "1" level. The output attains a "0" state when the D transistor is turned on.

SIGNAL PROCESSING/CLOCK INPUT REQUIREMENTS

The binaries of the 8200/8201/8202/8203 are DC-clocked master-slave elements which respond to the negative-going threshold of the input clock. The clock rise and fall times should be less than 200ns with an amplitude of 2.5V to prevent clock buffer Oscillations. The minimum clock pulse width should be greater than 17ns.

The RESET (R_D) input must be tied up to V_{CC} when not in use. The R_D can also be driven by a TTL gate, but should not be left floating. Both the clock and reset lines are only one (1.6mA) TTL "0" level load.

The propagation delays of the CLOCK input to Q output "1" and "0" levels and RESET (R_D) to Q output "0" levels are typically less than 30ns. The maximum transfer rate is typically 35 MHz. The D/$\overline{D}$ input set-up time is 15ns, and the input may be changed as the CLOCK falls (0ns hold time).

8202

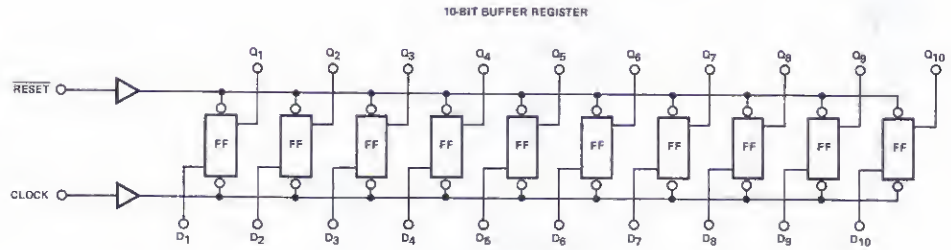


FIGURE 6

TRUTH TABLE

8202		
D_n	$\overline{RESET}$	Q_n+1
1	1	1
0	1	0

$\overline{RESET} = 0 => Q = 0$
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n + 1 IS TIME FOLLOWING CLOCK

TRUTH TABLE

8203		
$\overline{D}_n$	$\overline{RESET}$	Q_n+1
0	1	1
1	1	0

$\overline{RESET} = 0 => Q = 0$
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n + 1 IS TIME FOLLOWING CLOCK

8203

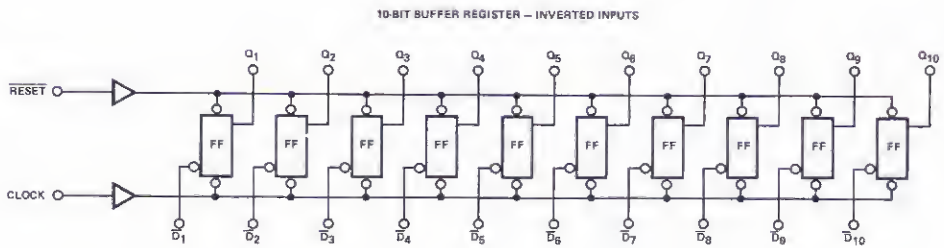


FIGURE 7

COMPOSITE CIRCUIT DIAGRAM (8200/8201/8202/8203)

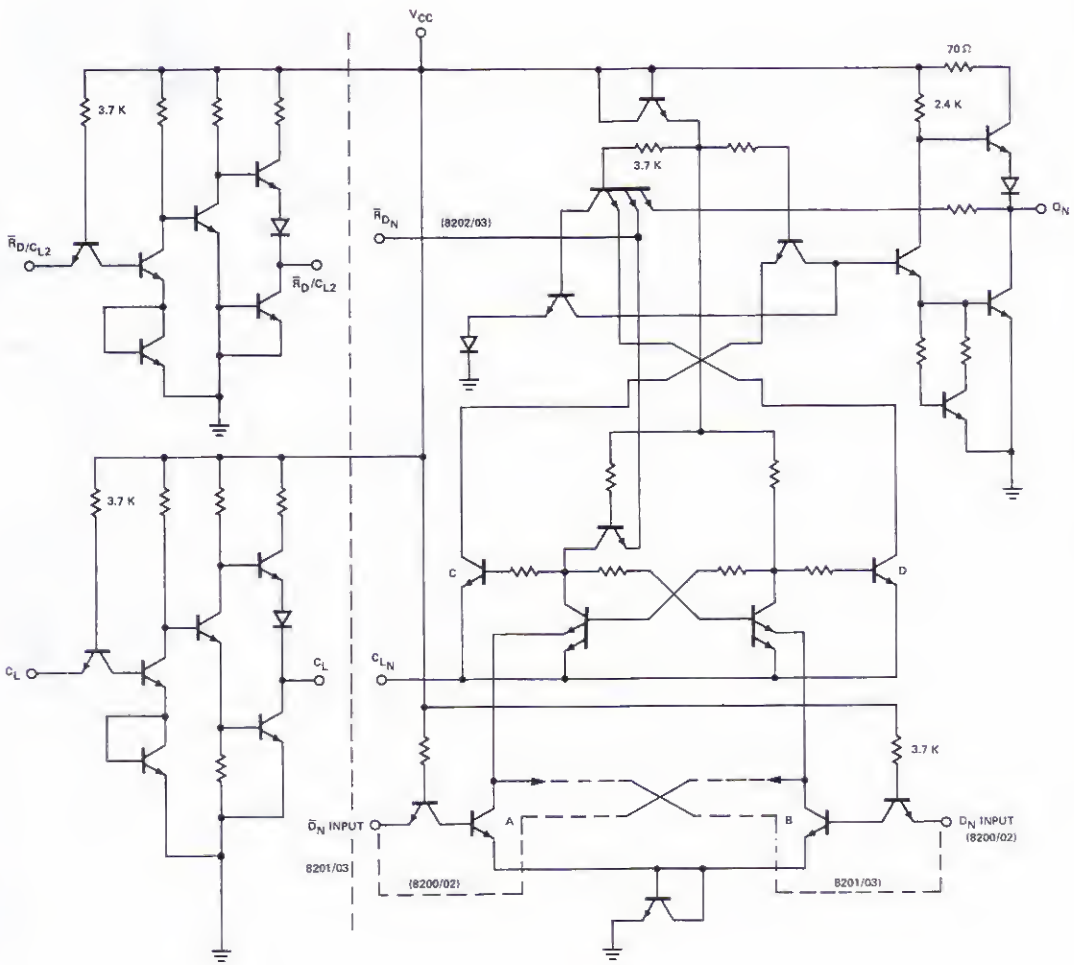


FIGURE 8

AC CHARACTERISTICS OF THE 8200/8201/8202/8203

FIGURE 9, 10, 11

Shows the typical clock pulse width vs. frequency for both positive- and negative-going clock pulses. Typically, a 17ns negative-going clock pulse width is required to clock the device as opposed to a 9ns positive-going clock pulse. By using a negative-going 20ns clock pulse (normally "1") as opposed to using a positive-going 20ns clock pulse (normally "0"), a typical power saving of 55mW may be realized as shown in Figure 10. The 50% duty cycle clock is also shown on this curve.

I_{CC} vs. Frequency for a Squarewave Clock for the 8202 is shown in Figure 11. All outputs are fully loaded and $T_A = 25°C$.

MINIMUM PULSE WIDTH VS. FREQUENCY FOR THE 8202

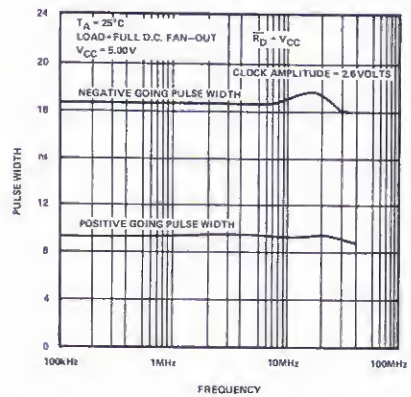


FIGURE 9

I_{CC} VS. FREQUENCY FOR NEGATIVE AND POSITIVE GOING PULSE FOR THE 8202

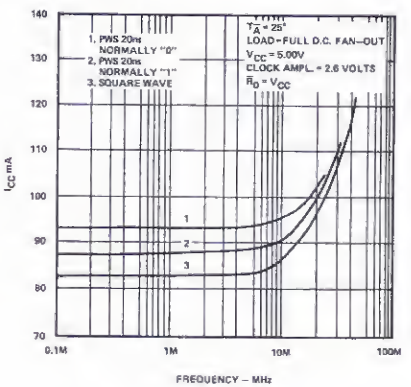


FIGURE 10

I_{CC} VS. FREQUENCY FOR A SQUARE WAVE CLOCK FOR THE 8202

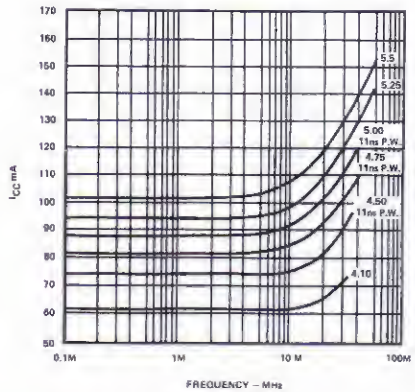


FIGURE 11

MAXIMUM CAPACITIVE LOADING

Even though the slave latch is not buffered, high capacitive loading of the 8200/8201/8202/8203 outputs does not significantly alter the operation of the register. When the CLOCK is low, the output is effectively only a buffer for the master latch. The master is disconnected from the slave latch when the CLOCK is high ("1").

8275 QUADRUPLE BISTABLE LATCH

The 8275 is a quadruple gated latch. Each latch has the complementary outputs, Q and $\overline{Q}$ available. The Q output follows the D input while the ENABLE input is high ("1") and retains the information which is present at the D input 20ns before the ENABLE goes low ("0"). Figure 12 shows the logic diagram of 1/4 of the 8275 quad-latch. Figure 13 shows the circuit diagram for the 8275.

LOGIC DIAGRAM

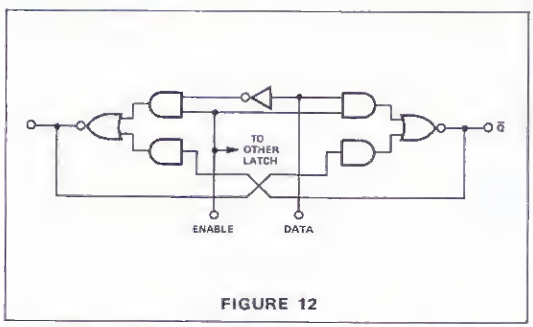


FIGURE 12

TRUTH TABLE FOR THE 8275 (Each Latch)

t_n	$t_n + 1$	
D	Q	$\overline{Q}$
1	1	0
0	0	1

1/4 8275 CIRCUIT DIAGRAM

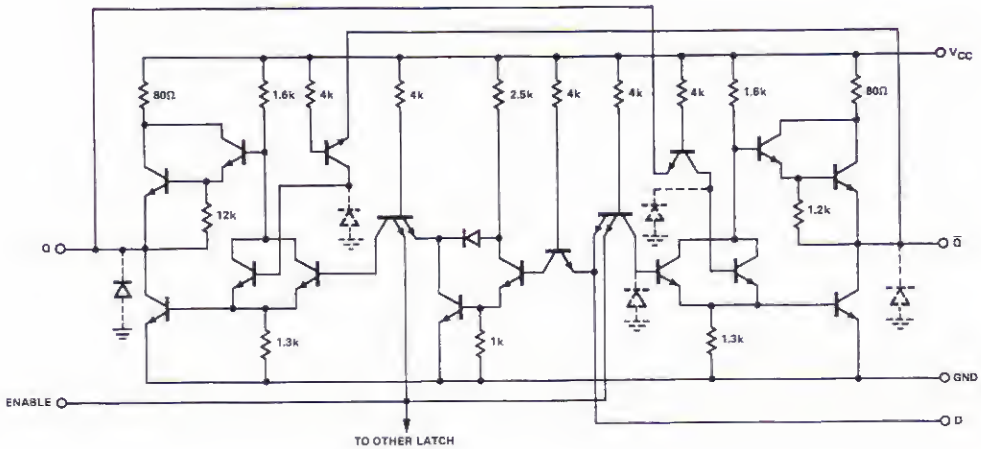


FIGURE 13

The V_{CC} to GROUND ceramic disc bypassing capacitor should be 0.02μF because of the eight totem pole output structures of the 8275.

MAXIMUM CAPACITIVE LOADING

The unbuffered latch of the 8275 limits the amount of load capacitance to less than 300pF in very short strobe pulse applications. If the strobe is held high long enough for the device to latch, the only limitation to output capacitive loading is the desired rise and fall times.

AC CHARACTERISTICS OF THE 8275

Minimum strobe pulse vs. temperature (T_A) is the typical minimum strobe pulse width required to strobe a "1" or a "0" as a function of temperature is shown in Figure 14.

D-input to enable falling edge set-up time vs. temperature is shown in Figure 15. This is the required time that the D-input information must be present and stable before the ENABLE can fall.

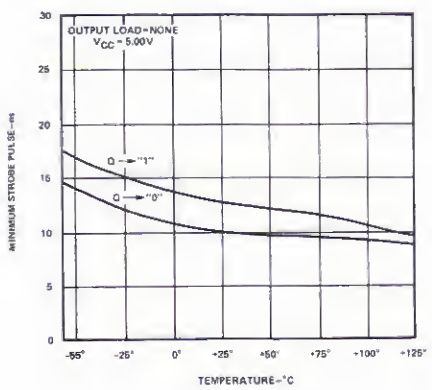


FIGURE 14

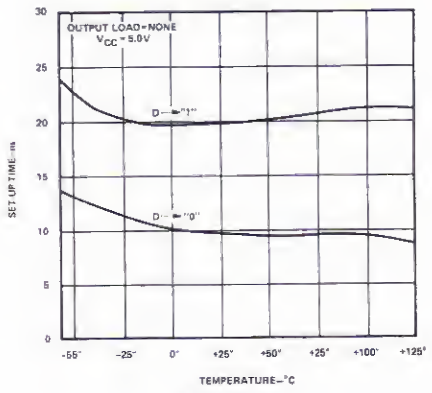


FIGURE 15

SHIFT REGISTER APPLICATIONS

SIMPLE 8-BIT RIGHT SHIFT REGISTER

Figure 16 shows two 8271 4-bit shift registers cascaded.

Let us assume first that the shift register flip-flops are reset to zero, by applying a logic low to the $\overline{R}_D$ input. Now the first bit X_1 (X_1 = 1 or 0) using the series data input is shifted in the first flip-flop, A_{10}, by the first falling transition of the CLOCK signal. The second trigger pulse of the clock shifts the first bit X_1 to the second flip-flop B_{10} and at the same time, the second bit X_2 is loaded in the first flip-flop A_{10}. For further clarification, an example with the series data (X_1 X_2, X_3, 0 0 0 . . . 0) is shown in Figure 17.

The power supply bypass should be in excess of 0.05μF.

SIMPLE 8-BIT RIGHT SHIFT REGISTER

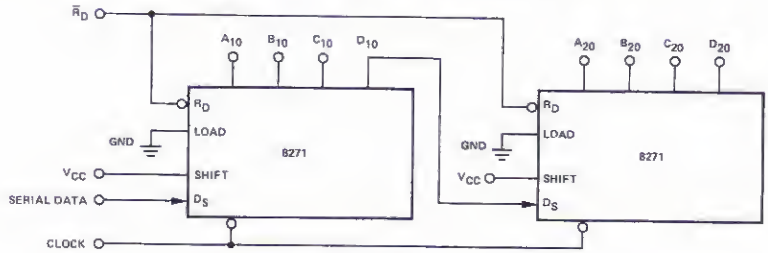


FIGURE 16

8-BIT SHIFT REGISTER SEQUENCE

CLOCK PULSE	STATE	SERIAL DATA (X_1 X_2 X_3 00...0)	FLIP-FLOP A_{10}	B_{10}	C_{10}	D_{10}	A_{20}	B_{20}	C_{20}	D_{20}
		RESET								
	0	X_1	0	0	0	0	0	0	0	0
→	1	X_2	X_1	0	0	0	0	0	0	0
→	2	X_3	X_2	X_1	0	0	0	0	0	0
	3	0	X_3	X_2	X_1	0	0	0	0	0
	4	0	0	X_3	X_2	X_1	0	0	0	0
	5	0	0	0	X_3	X_2	X_1	0	0	0
	6	0	0	0	0	X_3	X_2	X_1	0	0
	7	0	0	0	0	0	X_3	X_2	X_1	0
	8	0	0	0	0	0	0	X_3	X_2	X_1
	9	0	0	0	0	0	0	0	X_3	X_2
	10	0	0	0	0	0	0	0	0	X_3
	11	0	0	0	0	0	0	0	0	0

FIGURE 17

PARALLEL LOAD/SERIAL SHIFT

To demonstrate the parallel loading and serial shift operations of the 8270/71 we intend to preload the shift register with the data (D_A, D_B, D_C, D_D) = (1,0,0,0). Therefore, we apply a logic "1" to the pin D_A and a logic "0" to the pins D_B, D_C, D_D as shown in Figure 18. A logic "0" at the control input SHIFT enables the falling clock signal to transfer the data (D_A, D_B, D_C, D_D) = (1,0,0,0) to the shift register. To shift right now, the SHIFT input must go to a "1" and stay a logic "1" level permanently. The diagram in Figure 19 results. Since the D_0 output is feed back to the serial data input, D_s an elementary ring counter results:

ELEMENTARY RING COUNTER

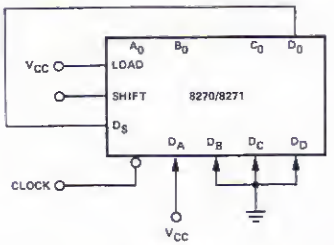


FIGURE 18

ELEMENTARY RING SEQUENCE

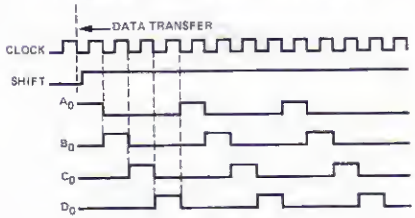


FIGURE 19

RING COUNTERS

A ring circuit is applied successfully if gating problems can be solved. A modified version of a ring circuit with self-correcting feature is shown in Figure 20.

SELF CORRECTING RING CIRCUIT

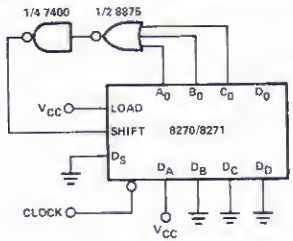


FIGURE 20

We start with an arbitrary state (A, B, C, D). After a maximum three shift pulses, we reach the state (0, 0, 0, A) and for this state, the SHIFT input is low. Thus, the word (1, 0, 0, 0) is preloaded by the next negative-going transition of the clock signal. The truth table for the ring circuit is given in Figure 21.

RING COUNTER TRUTH TABLE

1	0	0	0	preloaded data
0	1	0	0	
0	0	1	0	
0	0	0	1	feedback logic detects this state
1	0	0	0	preloaded data

FIGURE 21

A ring counter built with an n-stage shift register counts through 2n states. For n = 4, the eight states are listed below:

STATE	A	B	C	D	BCD	REMARK
1	1	1	1	1	15	FEEDBACK LOGIC
2	0	1	0	1	5	DETECTS THIS
3	0	0	1	1	3	STATE AND (0111)
4	0	0	0	1	1	IS PRELOADED
5	0	0	0	0	0	
6	1	0	0	0	8	
7	1	1	0	0	12	
8	1	1	1	0	14	END OF PERIOD
1	1	1	1	1		

Note, another stable loop exists with the remaining unused states which may be a matter of concern.

STATE	A	B	C	D	BCD	REMARK
1	1	0	1	1	11	FEEDBACK LOGIC
2	0	1	0	1	5	DETECTS THIS
3	0	0	1	0	2	STATE AND (0111)
4	1	0	0	1	9	IS PRELOADED
5	0	1	0	0	4	
6	1	0	1	0	10	
7	1	1	0	1	13	
8	0	1	1	0	6	END OF PERIOD
1	1	0	1	1	11	

With an additional feedback loop, the ring counter will correct itself from stable loop conditions which exist in the unused states and the circuit in Figure 22 results.

SELF CORRECTING RING COUNTER

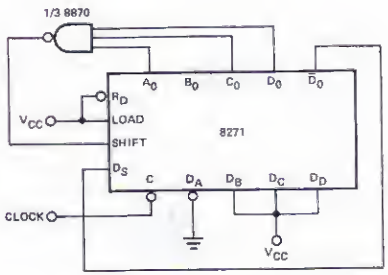


FIGURE 22

LEFT-RIGHT SHIFT REGISTER 8270/8271

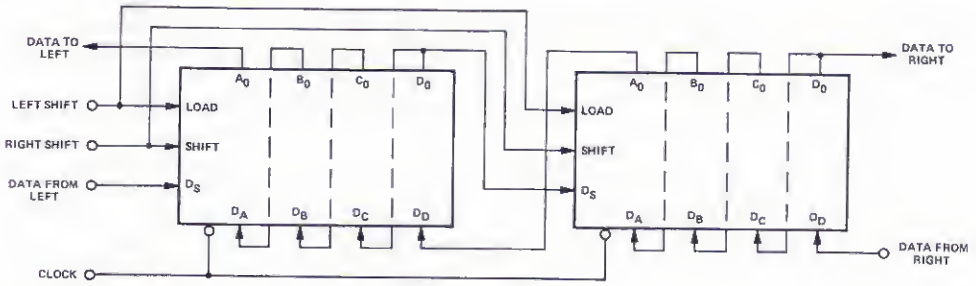


FIGURE 23

BI-DIRECTIONAL SHIFT REGISTER

The example shows an 8-bit serial-entry, left-right shift application in Figure 23. Note that a free-running clock can be applied.

TRUTH TABLE FOR LEFT/RIGHT SHIFT (Fig. 23)

LOAD	SHIFT	REMARK
0	0	Data Stored
0	1	Data Shifted Right
1	0	Data Shifted Left
1	1	Data Shifted Right

A left-right shift register with parallel entry can be obtained by using an 8233 multiplexer and is shown in Figure 24.

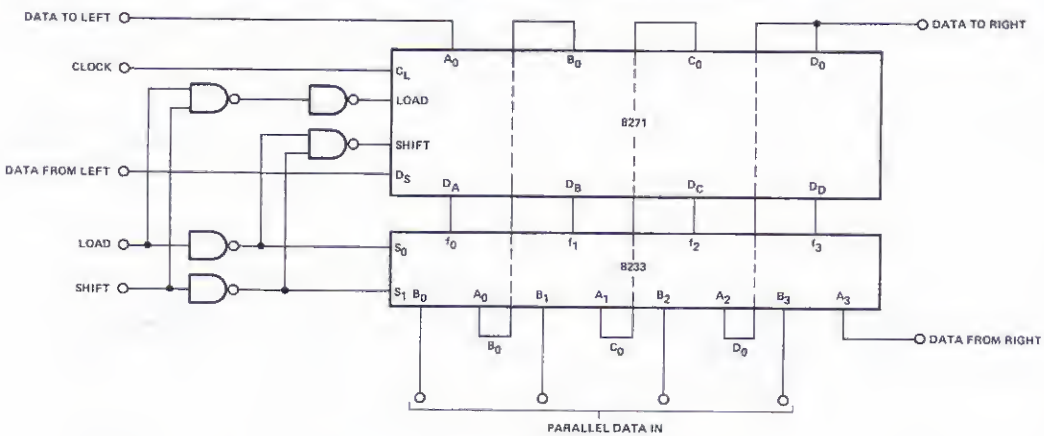
VARIABLE 4-BIT MODULO N COUNTER ($2 \leq N \leq 15$)

It is well-known that an n-stage binary shift register, when provided with suitably designed feedback paths, can count through 2^n-1 distinct states without any external input. For $n = 4$, there are two linear recurrences for a maximum period $p = 2^4 - 1 = 15$.

$$X_1 = A_0\bar{D}_0 + \bar{A}_0 D_0 \qquad (\bar{X}_1 = \bar{A}_0\bar{D}_0 + A_0 D_0)$$

or

SHIFT-RIGHT/SHIFT-LEFT/PARALLEL ENTRY SHIFT REGISTER



TRUTH TABLE

LOAD	SHIFT	FUNCTION
0	0	Hold
0	1	Shift Left
1	0	Parallel Load
1	1	Shift Right

FIGURE 24

$X_1 = C_o\bar{D}_o + \bar{C}_oD_o$ $\quad (\bar{X}_1 = \bar{C}_o\bar{D}_o + C_oD_o)$

X_1 = Generated bit, which is fed back to the first flip-flop.

As an example, we note the different states for the recurrence $\bar{X}_1 = \bar{C}_o\bar{D}_o + C_oD_o$, starting with $A_oB_oC_oD_o$ = (0 1 1 1).

We note that only the state 1 1 1 1 is not generated. Starting with 1 1 1 1 and applying the rule $X_1 = C_oD_o + \bar{C}_o\bar{D}_o$, the combination 1 1 1 1 will be generated once again. Therefore, it is obvious that the long period cannot include this state.

To implement a variable modulo N counter, we preload the shift register with the logic configuration N = ($A_oB_oC_oD_o$) whenever the end of the period (1 1 1 0) is reached. (For N, see Figure 25.

STATE TABLE FOR VARIABLE MODULUS COUNTER

STATE	$X_i = A_o$	B_o	C_o	D_o	N
1	0	1	1	1	15
2	1	0	1	1	14
3	1	1	0	1	13
4	0	1	1	0	12
5	0	0	1	1	11
6	1	0	0	1	10
7	0	1	0	0	9
8	1	0	1	0	8
9	0	1	0	1	7
10	0	0	1	0	6
11	0	0	0	1	5
12	0	0	0	0	4
13	1	0	0	0	3
14	1	1	0	0	2
15	1	1	1	0	–
16 = 1	0	1	1	1	

$\bar{C}_o\bar{D}_o + C_oD_o = 1 = \bar{X}_1$
FOR STATE 2

FIGURE 25

The counter can be locked at the end of each period with the control input LOAD. Further, the counter has a self-correcting feature for all N, because every possible state leads back to the original period (truncated period for $2 \leqslant N \leqslant 14$). Note, that the special state (1 1 1 1) influences the shift input as well as the state (1 1 1 0). The design is shown in Figure 26.

ERROR-CORRECTING CODE GENERATOR

A 4-bit shift register with a feedback loop is preloaded with an arbitrary 4-bit number. The shift register feedback path is given by the equation

$$X_1 = A_o \oplus B_o \oplus D_o = Y \oplus D_o = Y\bar{D}_o + \bar{Y}D_o$$

and

$$Y = A_o \oplus B_o = A_o\bar{B}_o + \bar{A}_oB_o$$

The preloaded numbers are shifted seven times, generating the output sequences shown in Figure 27.

The value of this procedure is that the set of sixteen codewords thus generated has the property that any two of them differ in the least three of their 7-bits. Further the additional bits b_1 b_2 b_3 enable to correct the code, if one but only one error occurs.

SHIFT = 0 preload the input information
SHIFT = 1 shift right

VARIABLE MODULO N COUNTER

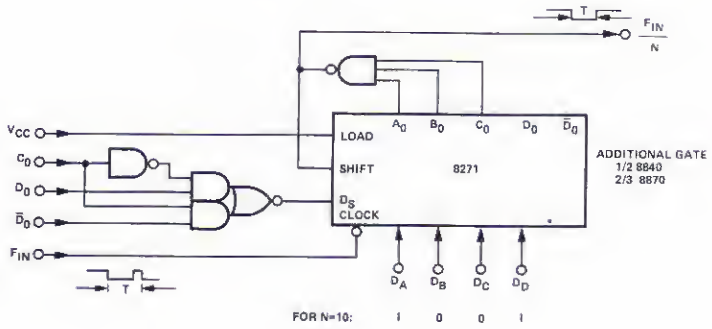


FIGURE 26

OUTPUT SEQUENCES FOR CODE GENERATOR

	INPUT INFORMATION				OUTPUT CODE WORDS							
	A_0	B_0	C_0	D_0	b_1	b_2	b_3	b_4	b_5	b_6	b_7	THE RELATIONS ARE
0	0	0	0	0	0	0	0	0	0	0	0	$b_1 = A_0 \oplus B_0 \oplus C_0$
1	0	0	0	1	0	1	1	0	0	0	1	$b_2 = B_0 \oplus C_0 \oplus D_0$
2	0	0	1	0	1	1	0	0	0	1	0	$b_3 = A_0 \oplus B_0 \oplus D_0$
3	0	0	1	1	1	0	1	0	0	1	1	$b_4 = A_0$
4	0	1	0	0	1	1	1	0	1	0	0	$b_5 = B_0$
5	0	1	0	1	1	0	0	0	1	0	1	$b_6 = C_0$
6	0	1	1	0	0	0	1	0	1	1	0	$b_7 = D_0$
7	0	1	1	1	0	1	0	0	1	1	1	
8	1	0	0	0	1	0	1	1	0	0	0	
9	1	0	0	1	1	1	0	1	0	0	1	
10	1	0	1	0	0	1	1	1	0	1	0	
11	1	0	1	1	0	0	0	1	0	1	1	
12	1	1	0	0	0	1	0	1	1	0	0	
13	1	1	0	1	0	0	1	1	1	0	1	
14	1	1	1	0	1	0	0	1	1	1	0	
15	1	1	1	1	1	1	1	1	1	1	1	

FIGURE 27

To check and correct if necessary the received message, we form the sums

$$S_1, S_2, S_3$$

$$S_1 = b_2 + b_5 + b_6 + b_7$$

$$S_2 = b_1 + b_4 + b_5 + b_6$$

$$S_3 = b_3 + b_4 + b_5 + b_7$$

If each sum is even, no correction is necessary.

If, in an example, S_1 is odd, one of the bits $b_2\ b_5\ b_6\ b_7$ is not correct. Assuming further the sum S_2 is also odd, only one of the bits b_5, b_6 being contained in S_1, as well as in S_2, can be incorrect. If the sum S_3 is even, the bit b_5 has the correct binary value implying b_6 is the erroneous bit. Assigning now the logic value Z = 1 if the corresponding to construct a truth table (Figure 28) for the erroneous bit. The hardware implementation is shown in Figure 29.

PSEUDO-RANDOM SHIFT REGISTER SEQUENCES

Pseudo-Random Bit Sequences (PRBS) appear to be band-limited noise. However, since they are periodic, can be

TRUTH TABLE FOR ERRONEOUS BITS

Z_3	Z_2	Z_1	ERRONEOUS BIT
0	0	0	b_2
0	1	0	b_1
1	0	0	b_3
0	1	1	b_6
1	0	1	b_7
1	1	0	b_4
1	1	1	b_5

INFORMATION

$Z_1 = b_2 \oplus b_3 \oplus b_5 \oplus b_7$

$Z_2 = b_1 \oplus b_4 \oplus b_5 \oplus b_6$

$Z_3 = b_3 \oplus b_4 \oplus b_5 \oplus b_7$

FIGURE 28

SELF CENTERING CODE GENERATOR

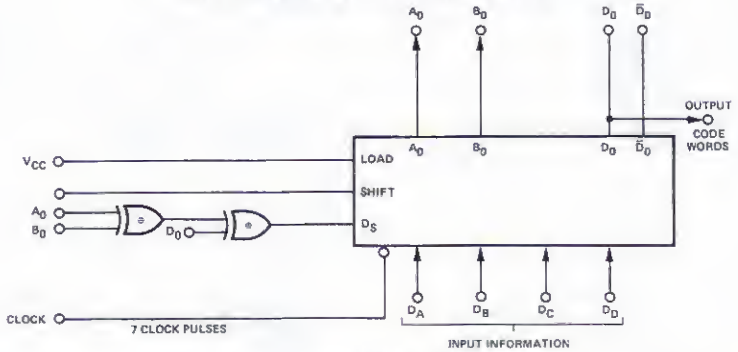


FIGURE 29

generated precisely and have reproducible pseudo-random noise spectra, PRBSs can provide significantly increased accuracy in time/distance measures and testing. By the use of a PRBS, JPL was able to achieve, to a high degree of accuracy, measurements of the distances from the Earth to Venus and the other planets through auto-correlation techniques.

Electronic equipment must function in an environment of random signals. The difficulty with random signals is that they are very difficult to precisely generate repeatedly. Malfunctions of equipment in a random environment are nearly impossible to reproduce but can be very easily reproduced if a failure occurs during a pseudo-random sequence.

An example of a 15-state maximum length generator is shown in Figure 30.

Figure 31 shows how a PRBS generator could be used to encode and decode data in a digital scrambling system. In this as well as the preceding application there are 2^n-1 possible states. For systems (such as the ones shown) where Exclusive-ORs are used in the feedback loop and the true data both in and out of each binary is used, the only prohibited state occurs when all outputs are "0". Two "0"s into an Exclusive-OR gate gives a "0" perpetuating the all "0"s state. This condition can be prevented by gating techniques.

SEQUENCE GENERATOR

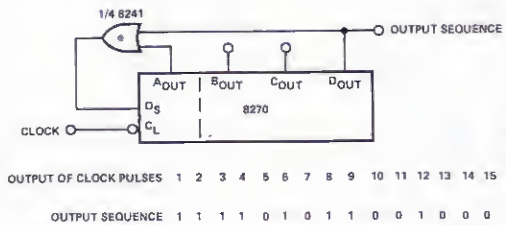


FIGURE 30

ENCODING/DECODING DIGITAL DATA

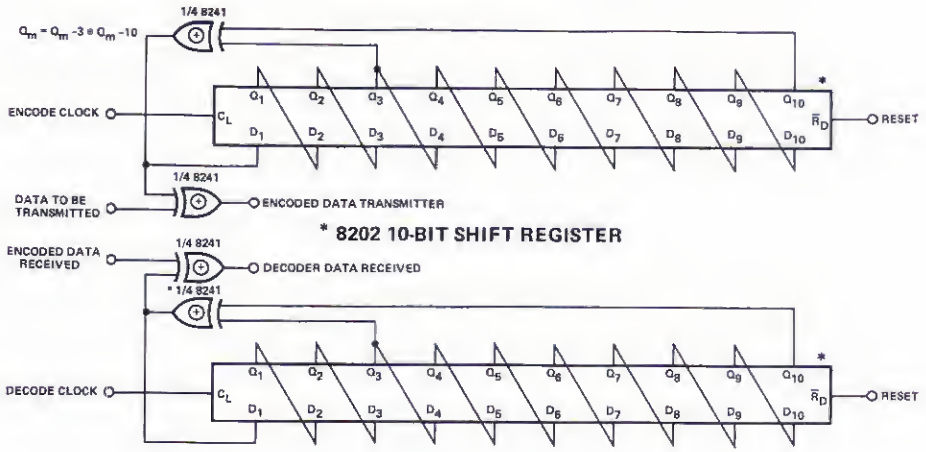


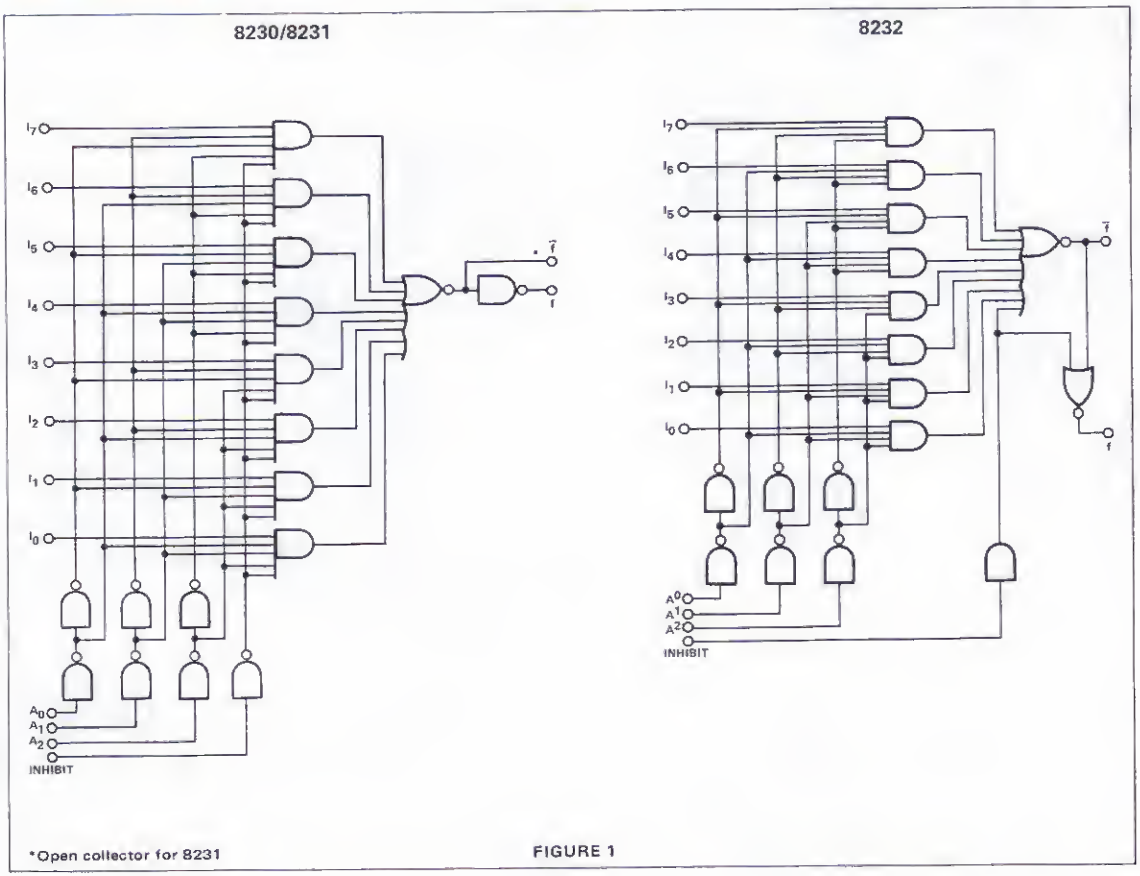
FIGURE 31

NOTE
The ENCODE CLOCK and DECODE CLOCK as well as the Pseudo-Random Sequence in both the Encoder and Decoder Shift Registers are synchronized. There are 2^n-1 or $2^{10}-1$ (1023) states which occur in a Pseudo-Random Binary Sequence.

INTRODUCTION

The 8230, 8231 and 8232 are 8-bit digital multiplexers having internal select decoding and an output inhibit control line. These devices are designed using standard TTL input and output structures (the 8231 is an open collector version): thus, they are compatible with DTL as well as TTL. The 8230 is pin for pin interchangeable with the 9312. The 8231 has the same pins and logic configuration as the 8230, but the $\overline{f}$ output has an open collector structure for systems flexibility.

LOGIC DIAGRAMS



*Open collector for 8231

FIGURE 1

DESCRIPTIONS

Eight multiplex input pins, three select decoding inputs, an output inhibit, f and $\overline{f}$ outputs and V_{CC} and ground are provided. The output inhibit control performs the function described in the logic diagram in Figure 1. As can be seen, the difference between the 8230/31 and 8232 is that the 8230/31 "inhibit" forces f = "0" and $\overline{f}$ = "1", while on the 8232, "inhibit" forces f and f = "0".

The device accepts eight different inputs and gates one-of-eight to the output, depending on the three binary bits that form the input code.

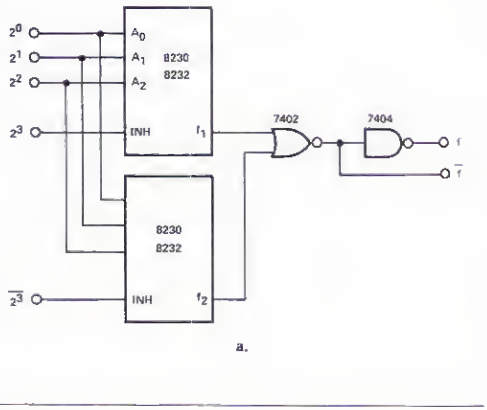
Some applications for the 8-bit multiplexer are as follows:

A. Methods for expansion
B. Variable frequency counter (see Figure 5)
C. Implementation of any four variable Boolean functions (see Figures 6 and 7)

EXPANSION OF THE 8230, 8231, 8232

Sixteen-line to one-line multiplexers are shown in Figures 2A and 2B (data inputs to the multiplexers are not shown). The basic idea is to simultaneously address the same input code line in both multiplexers and enable the output of only one. The 2^3 and $\overline{2^3}$ inputs act as the enable/inhibit control so that only one of the multiplexers is allowed to transmit information at a time. Remember, if the inhibit input is a "1", then the "f" output of the 8230/31/32 is forced to a "0". Therefore, in Figure 2A, one input to the 7402 (NOR gate) is always a logic "0", allowing the other multiplexer to be selected. An advantage of the 8231 (open collector) is that the outputs may be tied common and only an external pull-up resistor is necessary. (The "$\overline{f}$" outputs are used, as illustrated in Figure 2B, since the enable/inhibit line forces $\overline{f}$ to logic "1".

MULTIPLEXER EXPANSION



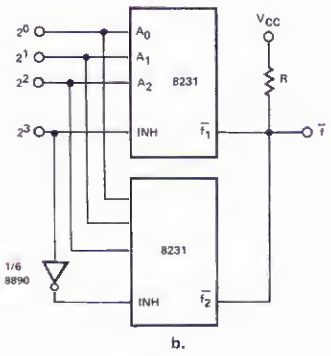


FIGURE 2

Figures 3 and 4 show further expansion using the same technique as in the example of Figure 2. The same address coding techniques may be used to expand the number of data inputs of the 8231. The $\overline{f}$ outputs are tied in common and an external pull-up resistor replaces the NOR and NAND output gating.

32 BIT MULTIPLEXER

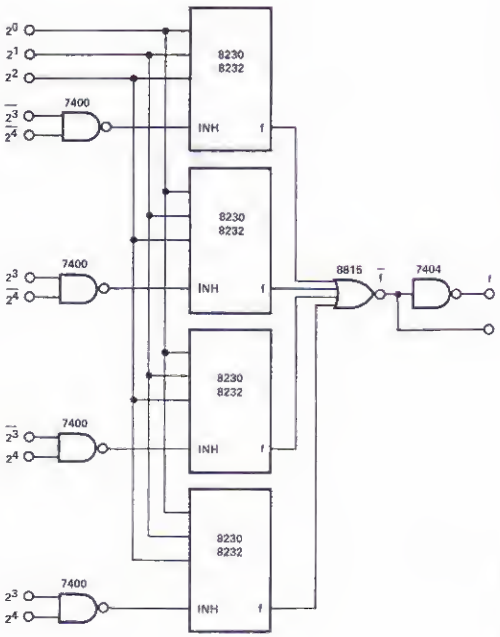


FIGURE 3

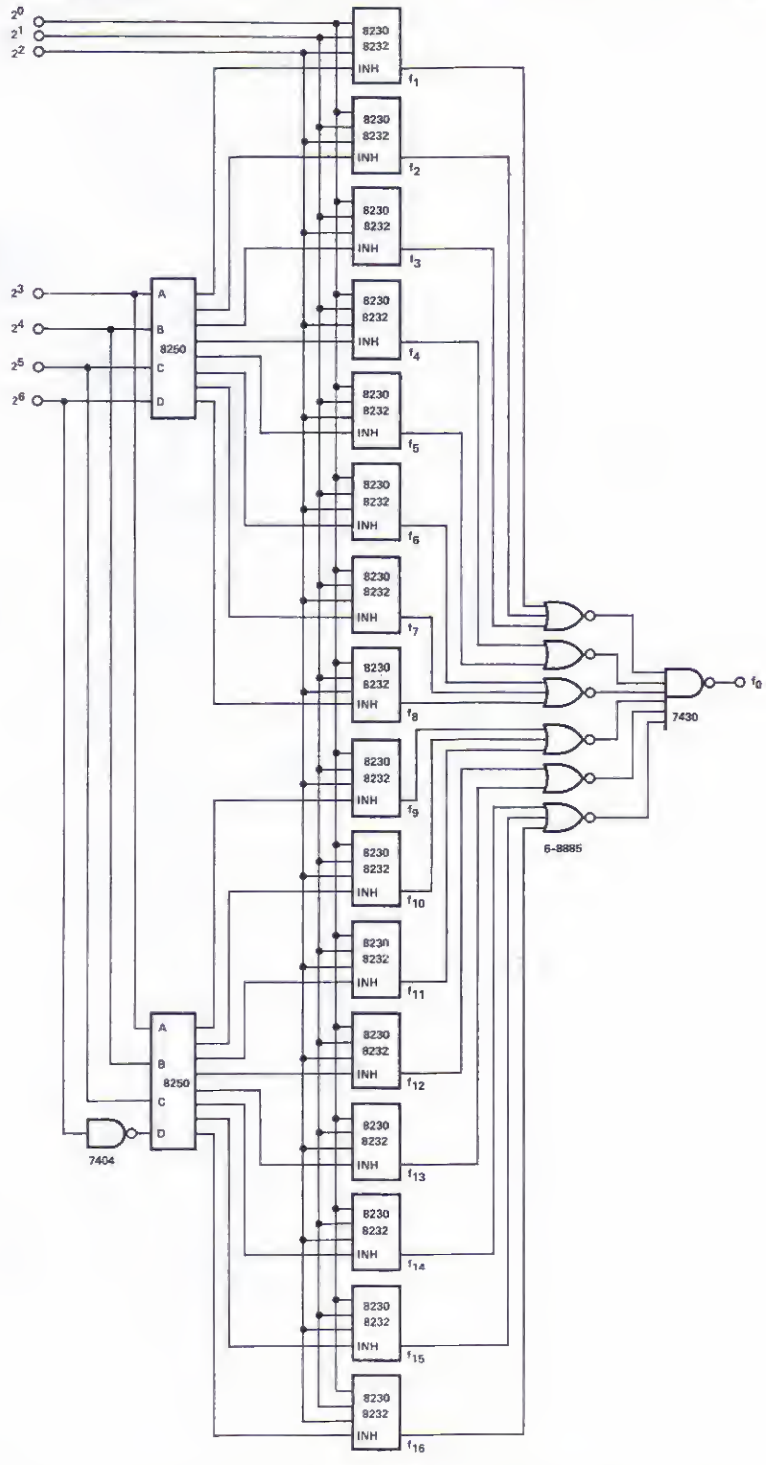

2^0
2^1
2^2
2^3
2^4
2^5
2^6
8230
8232
INH
f_1
f_2
f_3
f_4
f_5
f_6
f_7
f_8
f_9
f_{10}
f_{11}
f_{12}
f_{13}
f_{14}
f_{15}
f_{16}
A
B
8250
C
D
7404
7430
6-8885
f_0

FIGURE 4

VARIABLE FREQUENCY COUNTER

Figure 5 represents a simple frequency selector. Two 8281's (divide-by-16 binary counters) are connected in series. All 8 outputs are fed to the multiplexer. By selective addressing, as shown in Table 1, the various quantitized frequencies are selected.

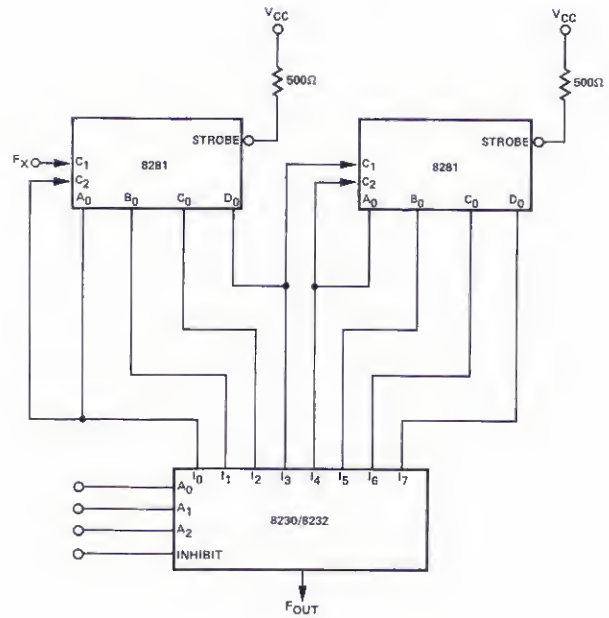


FIGURE 5

TABLE 1

INHIBIT	A_2	A_1	A_0	F_{OUT}
0	0	0	0	$F_X/2$
0	0	0	1	$F_X/4$
0	0	1	0	$F_X/8$
0	0	1	1	$F_X/16$
0	1	0	0	$F_X/32$
0	1	0	1	$F_X/64$
0	1	1	0	$F_X/128$
0	1	1	1	$F_X/256$
1	X	X	X	0

BOOLEAN FUNCTION GENERATOR

The 8230/32 may be used as a Boolean function generator that will produce any four variable Boolean functions.

Figure 6 illustrates how to implement the function generator using an 8271 4-bit shift register, and the 8230 or 8232.

Example: the function that was chosen is:

$$f_{out} = \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}\overline{B}CD + A\overline{B}CD + A\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} \quad \text{(Eq. 1)}$$

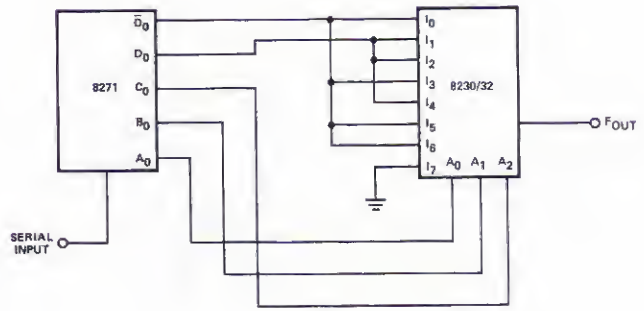


FIGURE 6

This function was arbitrarily chosen and is non-reducible. To implement Eq. 1, Karnaugh maps are used to tell what logic states should be provided to the data inputs and input code lines.

Three of the variables are always applied to the code select pins (A_0, A_1, A_2). The fourth variable is connected to the appropriate data inputs (I_0 through I_7), depending on the Karnaugh maps.

Karnaugh Map No. 1 (Figure 7) is the 4-variable Boolean function that is implemented. Karnaugh Map No. 2 (Figure 7) describes the logic requirments at the data inputs.

PROCEDURE

From Maps 1 and 2, the I_0 through I_7 connections can be determined. The content of the 2 squares (in Karnaugh Map No. 1) associated with an input on Karnaugh Map No. 2 determines which connection is made to that data input.

1. If both squares (Map No. 1) contain "0", ground the input.
2. If both squares (Map No. 1) contain "1" 's, connect the input to V_{CC}.
3. If the squares contain "1" and "0" (Map No. 1), and the "1" occurs in the square associated with the True form of the 4th variable, then connect the True output to the input specified by Map No. 2.
4. If the squares contain "1" and "0" (Map No. 1), and the "1" occurs in the square associated with the Complement form of the 4th variable, connect the Complement to the input specified by Map No. 2.

KARNAUGH MAPS

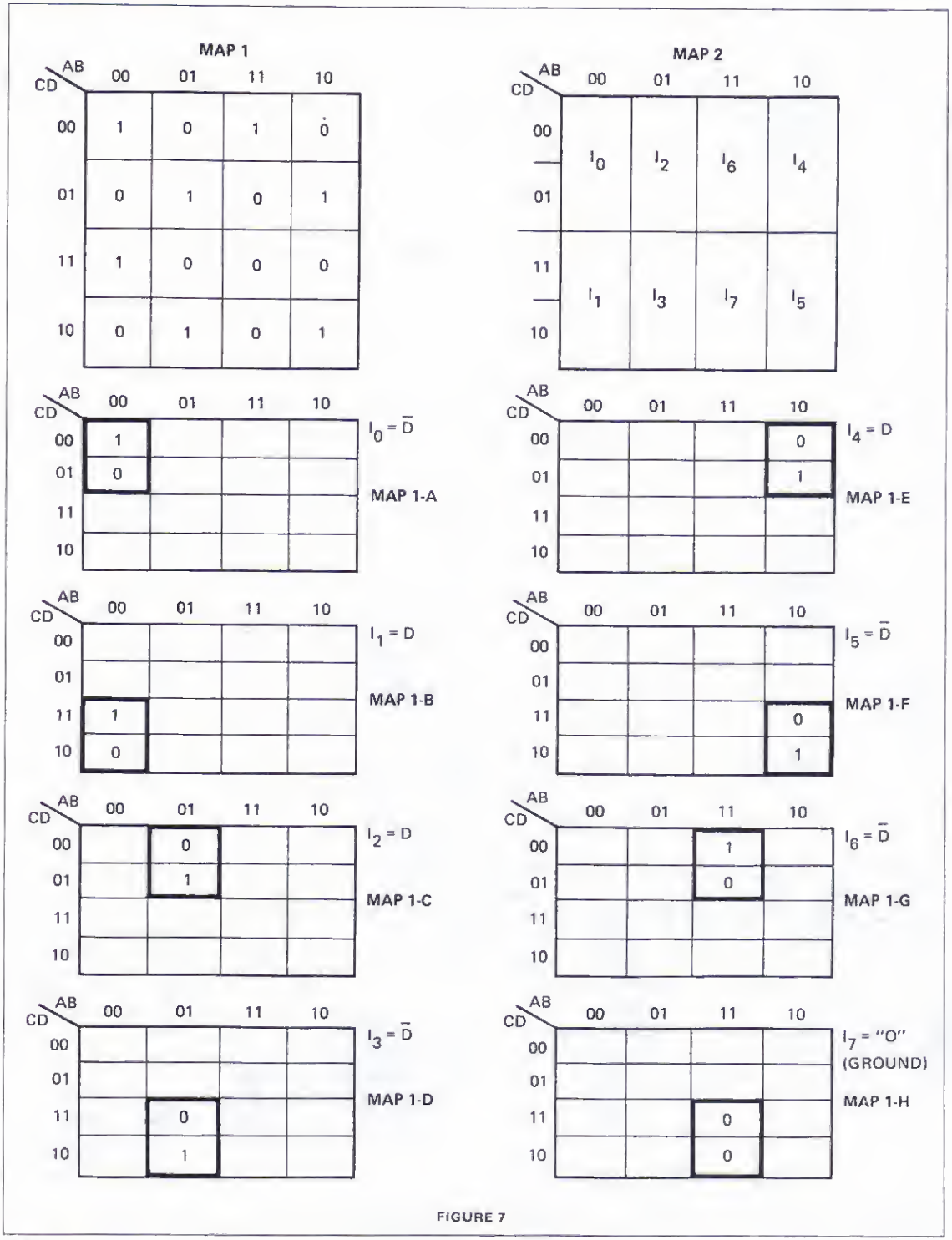


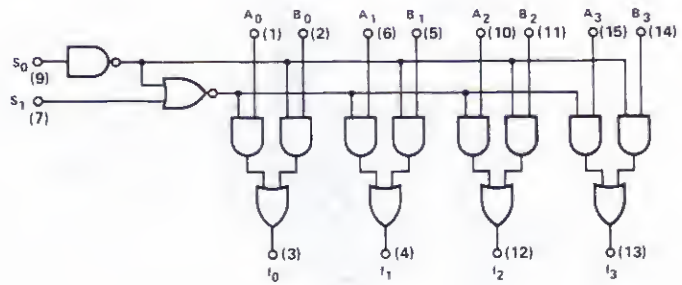
FIGURE 7

INTRODUCTION

The 2-input 4-bit digital multiplexer family has been designed for a wide range of data selection applications. The function of these multiplexers can be viewed analogous to a 4-pole 2 position switch. The 8233 features non-inverting data path while the 8234 features inverting data paths. For easy array expansion and bus applications of the 8234 has open collector outputs. Whereas the 8233/8234 multiplexers are used in general purpose multiplexing applications the 8235 and 8266/67 simplify applicatons where true/complement capability or additional logic flexibility is needed together with multiplex capability. Figure 1 shows the mulitplexer family together with the truth tables. Although no discussed here, 3-input 4-bit multiplexers with true/complement capability are also available from Signetics. These devices, the 8263 and 8264 provide minimum device count when a large number of data sources has to be multiplexed.

LOGIC DIAGRAM AND TRUTH TABLES

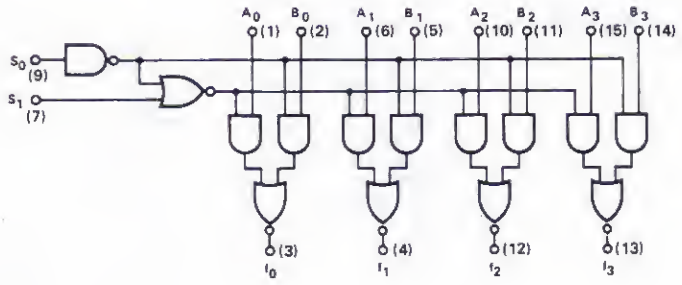
8233 (ACTIVE PULL-UP)



S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8234 (OPEN COLLECTOR)



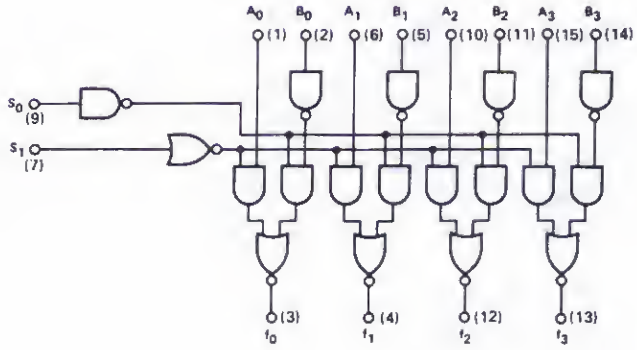
S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

FIGURE 1

LOGIC DIAGRAM AND TRUTH TABLES (Continued)

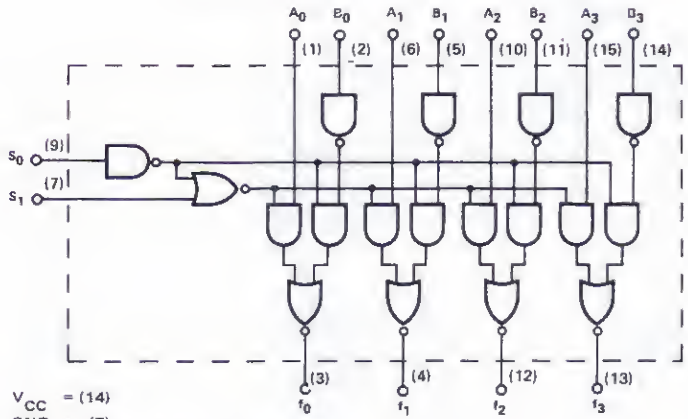
8235 (OPEN COLLECTOR)



S_0	S_1	f_n
0	0	$\overline{A_n}B_n$
0	1	B_n
1	0	$\overline{A_n}$
1	1	1

V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

8266/8267 (8267 OPEN COLLECTOR)



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A_n}$
1	1	1

FIGURE 1 (Cont'd)

APPLICATIONS

If data has to be selected from two registers, it can be done simply with the 8233 multiplexer, shown in Figure 2. Either the contents of register A or register B is selected by means of the S_0 and S_1 inputs. In those applications where more than two data sources are used or where the information is multiplexed onto a data bus, use can be made of the 8234 open collector multiplexer as shown in Figure 3.

2-INPUT 4-BIT MULTIPLEXER

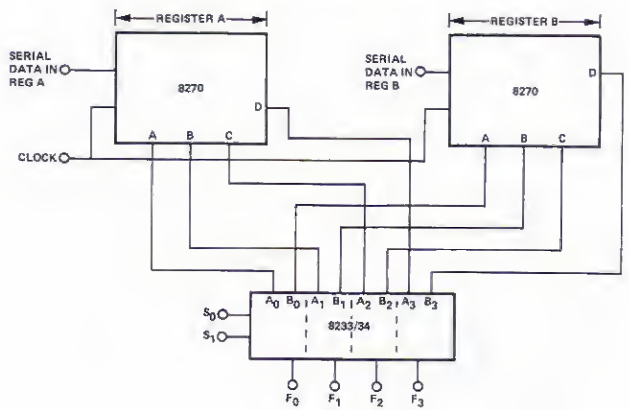


FIGURE 2

4-INPUT 4-BIT MULTIPLEXER

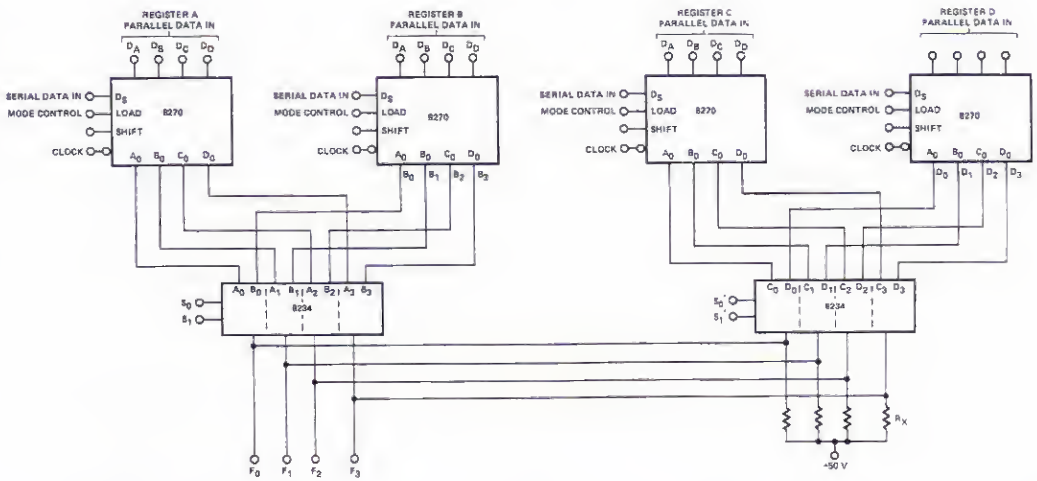


FIGURE 3

The complement capability of the 8235 and 8266/67 makes them useful in a variety of central processor application where in addition to the multiplex mode the true/complement function is often required. When the two inputs A_i and B_i are connected together the 8235 and 8266/67 perform as conditional complementers which are required in conjunction with addition/subtraction circuits.

The subsystem shown in Figure 4 assumes that in the SUBTRACT mode (X-Y), Y (Y_0, Y_1. . . Y_6, Y_7) is always the smaller of the two binary numbers. If Y is not the smaller of the two numbers, correction may be made by detecting the presence of a CARRY term at the most significant bit (MSB), then initiating the appropriate correction procedure.

HIGH SPEED 8-BIT BINARY ADDER-SUBTRACTOR
(2's COMPLEMENT)

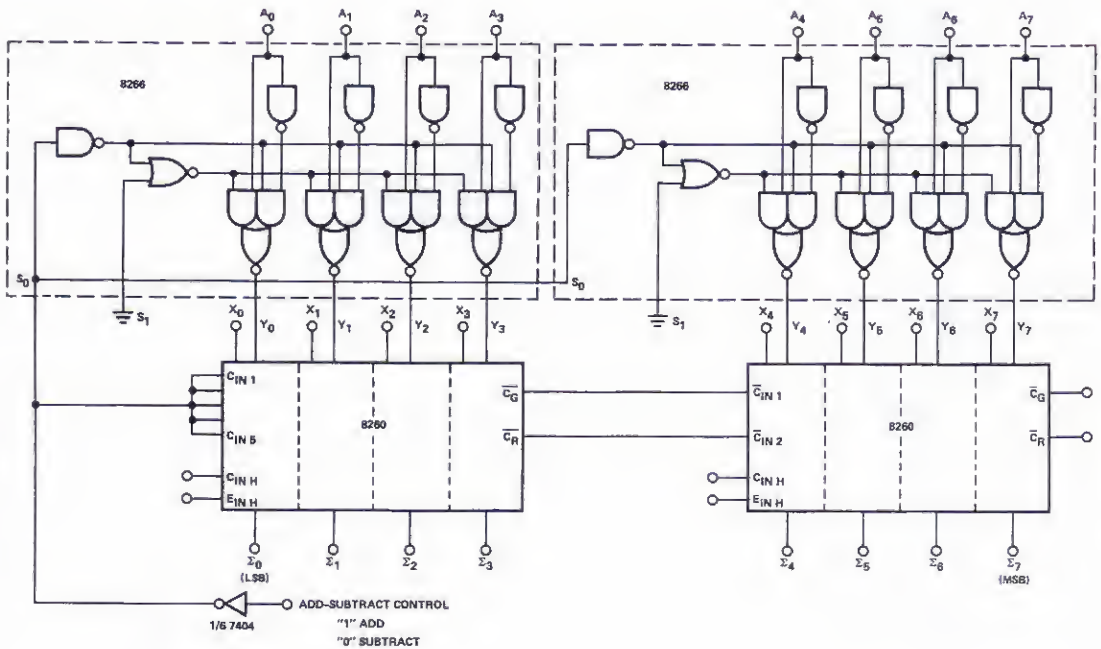
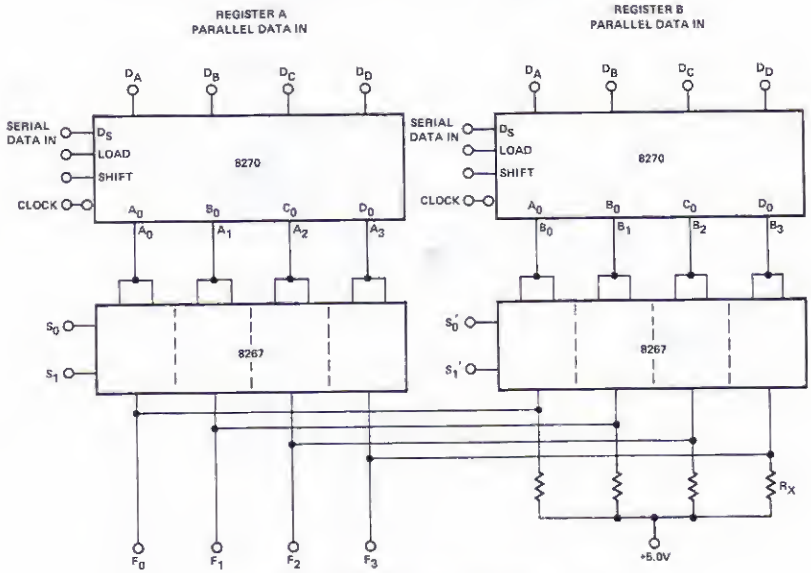


FIGURE 4

The 8267 is well suited for multiplex applications of Conditional Complement terms in ADD-SUBTRACT subsystems as shown in Figure 5.

The 8267 features open collector output switching transistors which may be used to perform the collector AND function, thus increasing the number of input terms to be multiplexed per bit. The maximum expansion requires an external pull-up resistor of 342 ohms and provides a 128-INPUT 4-BIT MULTIPLEXER. Selection of input terms is accomplished by applying the desired code on the S_0 S_1 lines of the appropriate 8267 while S_0 - S_1 - 1 is applied to the unselected 8267's as shown in the truth table in Fig. 1.

2-INPUT 4-BIT MULTIPLEXER/CONDITIONAL COMPLEMENTER



$$F_i = \left[S_0' S_1' (A_i S_0 S_1 + A_i S_0 S_1)\right] + \left[S_0 S_1 (B_i S_0' S_1' + B_i S_0' S_1')\right]$$

FIGURE 5

DEVICE DESCRIPTION (8241)

The 8241 is a quad EXCLUSIVE-OR gate used in a variety of digital comparator and adder systems. The logic diagram is shown in Figure 1 along with its logic symbol and truth table.

LOGIC DIAGRAM

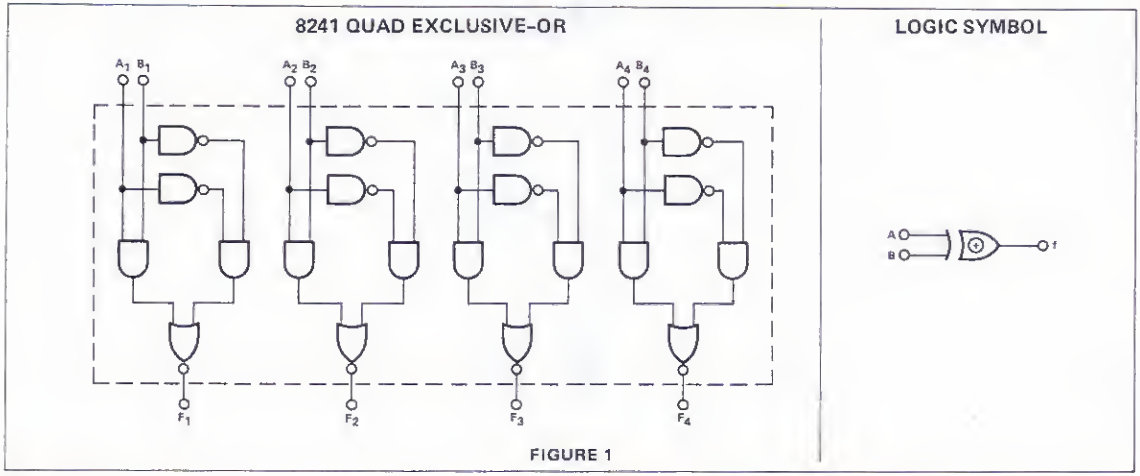


FIGURE 1

TRUTH TABLE (8241)

A	B	f
0	0	0
0	1	1
1	0	1
1	1	0

DEVICE DESCRIPTION (8242)

The 8242 is a quad EQUALITY COMPARATOR or COINCIDENCE gate. Input bits A_nB_n are compared for equality. If $A_n = B_n$, the corresponding output F_n will be a logical "1". If $A_n \neq B_n$ output F_n will be a logical "0".

The logic diagram, symbol and truth table for the 8242 are shown in Figure 2.

LOGIC DIAGRAM

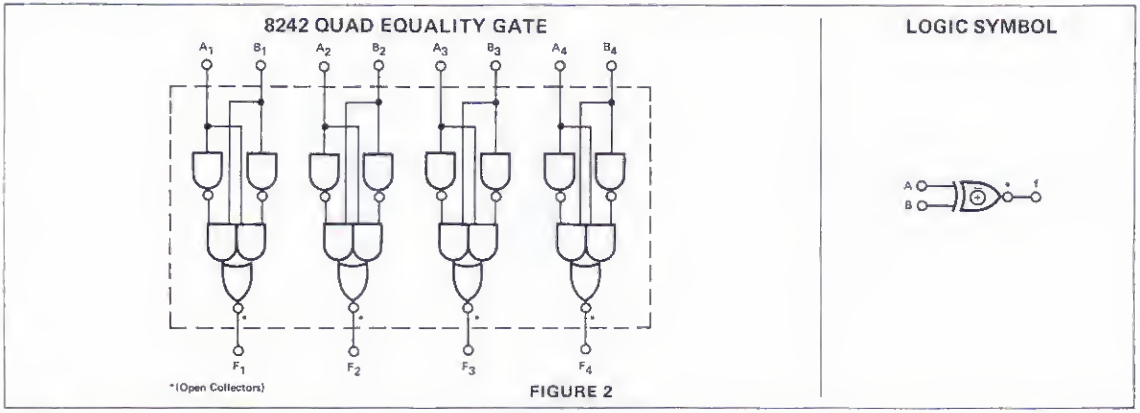


FIGURE 2

TRUTH TABLE (8242)

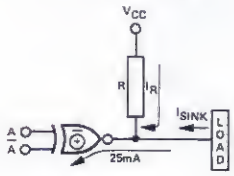
A	B	f
0	0	1
0	1	0
1	0	0
1	1	1

Although TTL circuit design techniques are used in the 8242, the outputs feature open collector switching transistors. This feature allows the designer to select a variety of comparator lengths by tying the outputs F_1, F_2,... F_n together and selecting an external pull-up resistor in accordance with his specific requirements.

When selecting a pull-up resistor the following guidelines are suggested:

1. Determine the maximum current that the 8242 must sink from the load when the 8242 is in the "0" output state.
2. Subtract the required sink current from 25mA, the total sink capability of the 8242. This determines the amount of current which may be allowed to flow through the external pull-up resistor.

8242 OUTPUT = "0"

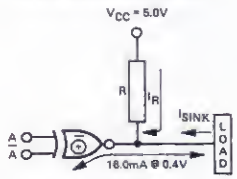


$I_R + I_{SINK} \leq 25mA$

$MAX.\ I_R \leq 25mA - I_{SINK}$

3. Assume V_{CC} = 5.0V and output "0" level = 0.4V max., then calculate the minimum value of the pull-up resistor required to satisfy $I_R + I_{SINK} \leq$ 25mA.

8242 OUTPUT = "0"



$$MIN.\ R \geq \frac{V_{CC} - V_{OUT}\text{ "0"}}{25mA - I_{SINK}}$$

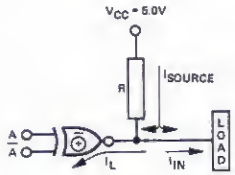
$$\geq \frac{V_{CC} - V_{OUT}\text{ "0"}}{I_R}$$

$$\geq \frac{5.0V - 0.4V}{I_R}$$

$$MIN.\ R \geq \frac{4.6V}{I_R}$$

4. Check to ensure that the pull-up resistor selected is consistent with the "1" output voltage and "1" output current required.

8242 OUTPUT = "1"



I_L = 25mA MAX.

$I_{SOURCE} = I_L + I_{IN}$

"1" OUTPUT VOLTAGE = $V_{CC} - (I_{SOURCE} \times R)$

$MAX.\ I_{SOURCE} \times R$ = V_{CC} − "1" OUTPUT VOLTAGE

= 5.0V − 2.6V

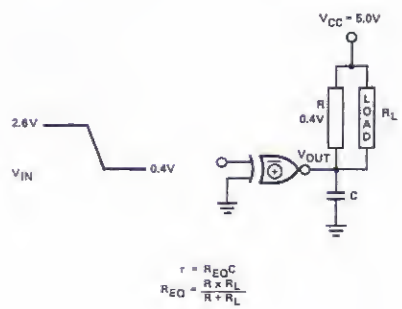
$MAX.\ I_{SOURCE} \times R \leq 2.2V$

$$MAX.\ R \leq \frac{2.2V}{I_{SOURCE}}$$

To ensure that normal "1" level noise margins are maintained, the "1" output voltage should be maintained at 2.6V or above for V_{CC} = 5.0V.

Under light fan-out conditions, a relatively large resistor (≈ 4K to 10K) may be considered by the designer. Two considerations must be weighed in selecting a large value pull-up resistor.

First, rise time into a capacitance load at the output will be directly related to the value of pull-up resistor used. An approximation of the time required for the rising output voltage to reach a defined "1" level (2.0V) is $\tau/2$, or $1/2R_{EQ}C$.



$$\tau = R_{EQ}C$$

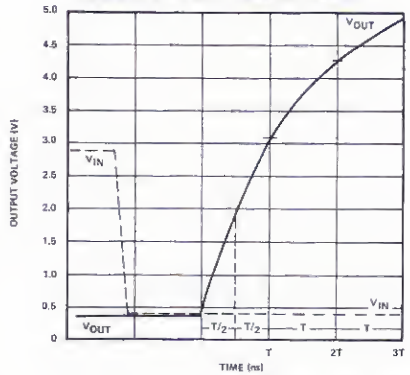
$$R_{EQ} = \frac{R \times R_L}{R + R_L}$$

The voltage level attained in time $\tau \approx 0.63 \times V_{CC} = 3.15V$, well above minimum "1" logic input threshold voltage.

The second consideration which should be given to use of a large value pull-up resistor is the resulting susceptibility to capacitively coupled noise along printed circuit runs or wire interconnects. Since the magnitude of coupled noise is related to the equivalent impedance between the output of the 8242 and its load, care should be taken in the physical layout to isolate the output of an 8242 where a large value pull-up resistor has been chosen. In general, a pull-up resistor of 1KΩ or less is recommended where "0" DC fan-out is less than 10.0mA and power supply drain current is not critical.

There is no current spike associated with the output transition in the 8242 since the active pull-up of classic TTL designs has been removed. It is not necessary to capacitively decouple the 8242.

RISING OUTPUT WAVEFORM UNDER CAPACITANCE LOAD



APPLICATIONS

HIGH SPEED EQUALITY COMPARATORS

The Exclusive-OR may be used to check the equality of two binary coded words. From the truth table (Figure 1), the output of the Exclusive-OR is "1" when the inputs are not equal and "0" when the inputs are equal. By connecting the output of the Exclusive-OR to one input of a NOR gate (Figure 3), the output (f_0) will be "1" if, and only if, all bits of the two words are equal. Figure 4 shows a high speed equality comparator capable of comparing two 4-bit words.

EQUALITY COMPARATOR FOR TWO 4-BIT WORDS

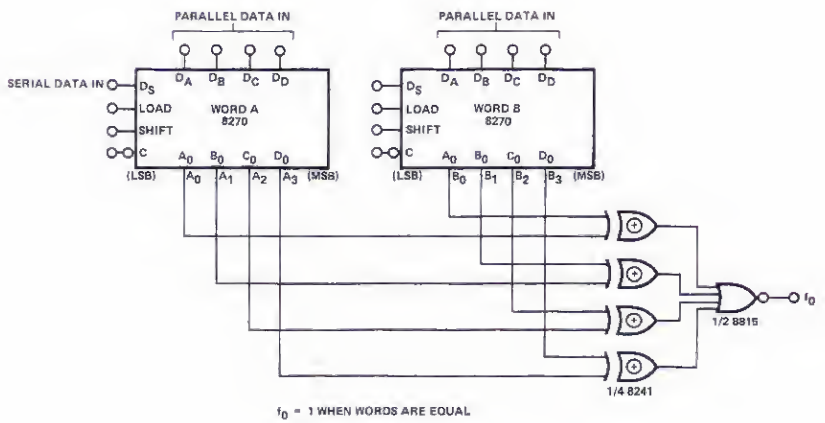


FIGURE 3

Figure 4 demonstrates a method of designing a high speed equality comparator for a 32-bit word length using TTL elements. This method may also be used to design high speed equality comparators for other word lengths between 4-bits and 32-bits. The addition of the single 8-input NAND (8808) provides f_0 = "0" when words A (A_0, A_1, $A_2 \ldots A_{n-1}$, A_n) and B (B_0, B_1, $B_2 \ldots B_{n-1}$, B_n) are equal and f_0 = "1" when words A and B are unequal.

HIGH SPEED 32-BIT WORD EQUALITY COMPARATOR

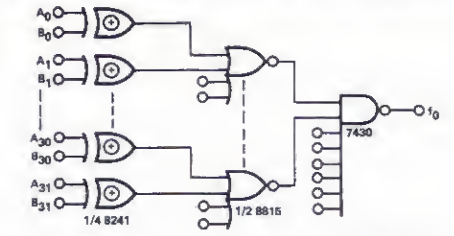


FIGURE 4

MAXIMUM LENGTH EQUALITY COMPARATORS

The 8242 is specifically designed for use in equality comparison of word lengths in excess of 4 bits, while providing minimum device-counts. From the truth table (Figure 2) the 8242 will provide a "1" output when the inputs are equal and "0" when the inputs are unequal. The open collector outputs of the 8242 can be connected together to perform a logical AND of the output terms when returned to V_{CC} through an external resistor.

Guidelines for selecting the pull-up resistor value are given under DEVICE DESCRIPTION: 8242. The can-count reduction for the 32-bit word length equality comparator shown in Figure 4 is demonstrated in Figure 5.

IMPLEMENTATION OF 32-BIT WORD COMPARATOR

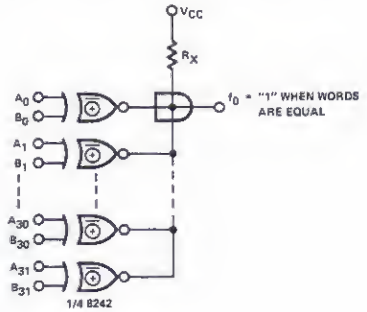


FIGURE 5

PARITY TESTER/GENERATOR*

The Exclusive-OR and EQUALITY COMPARATOR may be used in parity testing or generating applications. Parity generators find wide application in output equipment which records or transmits data. A parity bit is generated to ensure that the total number of logical ones in the word being recorded or transmitted is either even or odd. On the reading or receiving end of the data transmission a parity check is performed on the transmitted data (including the parity bit) to ensure that no word bit has been "dropped" (i.e., no "1" has been lost). Figure 6 shows a general case implementation of parity generation and parity check in the recording or transmission of a 4-bit word. Note that there are five bits of transmitted data, the 4-bit word plus the parity bit.

In data transmissions which inlcude a parity bit, the designer chooses between the EVEN PARITY system and the ODD PARITY system. In the even parity system, an even number of logical ones is always transmitted (data plus parity bit). Therefore, the EVEN PARITY GENERATOR

*SEE ALSO 8262 9-bit comparator applications memo.

GENERAL CASE PARITY GENERATOR AND PARITY CHECK

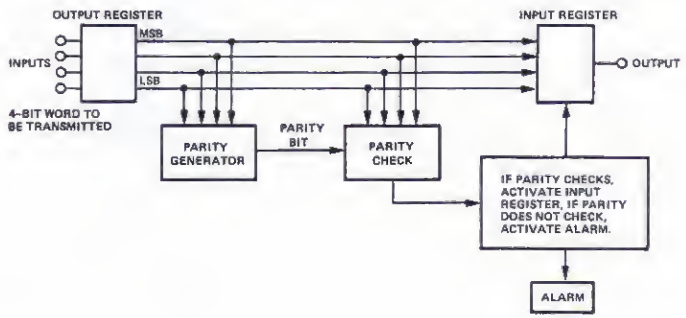
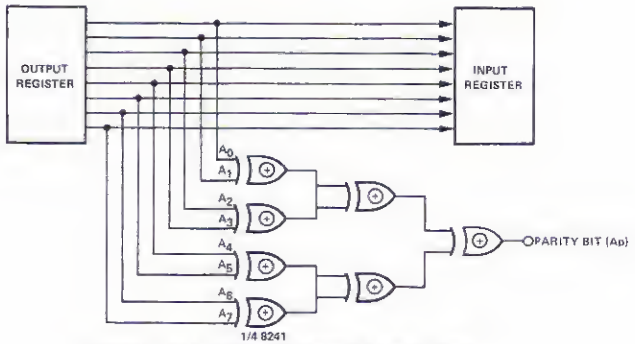


FIGURE 6

examines the data to be transmitted and produces an additional "1" if the data contains an odd number of logical ones. If the data to be transmitted already contains an even number of logical ones, the EVEN PARITY GENERATOR produces a parity bit equal to "0". In either case an even number of logical ones (data plus parity bit) will be transmitted. The 8241 may be used to design an EVEN PARITY GENERATOR, as shown in Figure 7.

EVEN PARITY GENERATOR USED WITH 8-BIT WORD



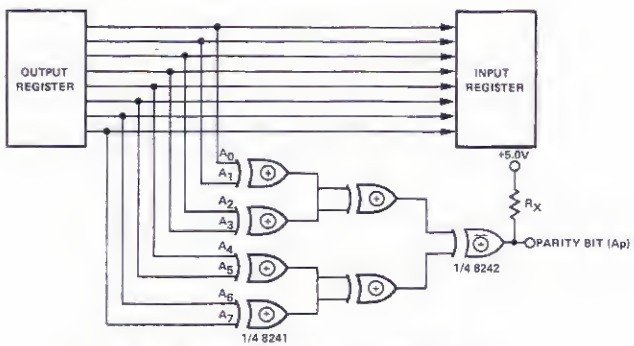
"1" WHEN A_0 THRU A_7 CONTAINS ODD NUMBER OF LOGICAL ONES
"0" WHEN A_0 THRU A_7 CONTAINS EVEN NUMBER OF LOGICAL ONES

FIGURE 7

Conversely, the ODD PARITY GENERATOR examines the terms in the data to be transmitted and produces a "0" when the data already contains an odd number of logical ones. If, however, the data contains an even number of logical ones, the odd parity generator produces an additional "1". In either case the total number of logical ones (data and parity bit) transmitted is odd. An advantage of odd parity is that transmission of "0" data is not mistaken for no information (always have one "1" bit).

The odd parity generator is shown in Figure 8. It differs from the even parity generator only in the output stage which incorporates 1/4 of an 8242.

ODD PARITY GENERATOR USED WITH 8-BIT WORD



"1" WHEN A_0 THRU A_7 CONTAINS ODD NUMBER OF LOGICAL ONES
"0" WHEN A_0 THRU A_7 CONTAINS EVEN NUMBER OF LOGICAL ONES

FIGURE 8

As described in Figure 6, the receiving equipment must check all incoming lines to ensure that no bits have been dropped in data recording or transmission.

In the even parity system, an EVEN PARITY CHECKER examines all incoming terms (data plus parity bit) and provides a "1" output if there are still an even number of logical ones contained in the data received. If a bit has been dropped and an odd number of logical ones is received, the output of the even parity checker will be "0". An example of an even parity checker is shown in Figure 9.

EVEN PARITY CHECKER USED WITH 8-BIT WORD

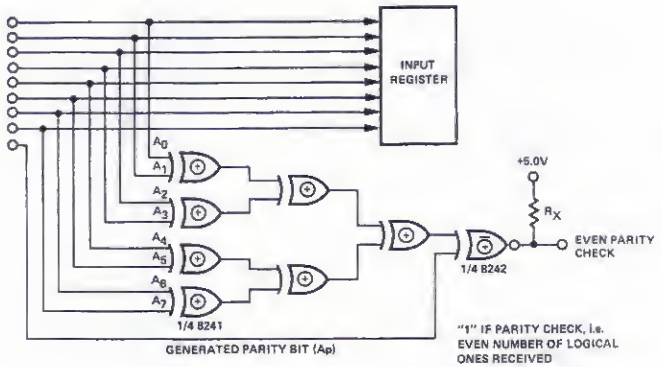


FIGURE 9

The ODD PARITY CHECKER provides a "1" output when the total number of logical ones received (data plus parity bit) is odd and produces a "0" when the total number of logical ones received is even. Figure 10 shows an example of an odd parity checker.

ODD PARITY CHECKER USED WITH 8-BIT WORD

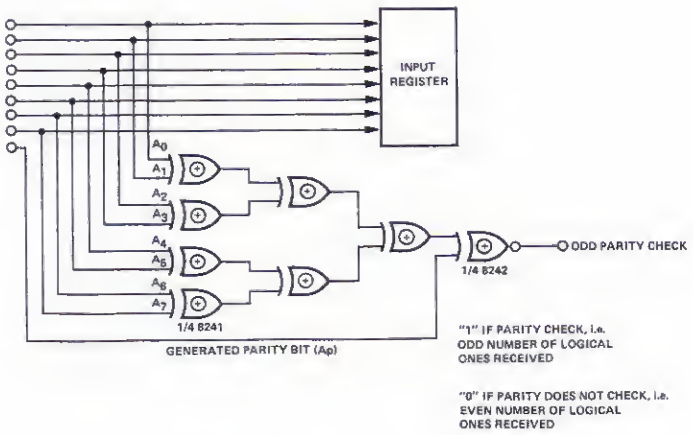


FIGURE 10

Parity generators and checkers find wide application in I/O (input-output) equipment such as magnetic tape writers and readers. In addition parity generators and checkers may be used anywhere within a system where there is concern about "dropping" bits due to the nature of the equipment used to send and/or receive information. A parity system may also be incorporated in equipment where high ambient noise is of concern when recording or transmitting data.

BINARY ADDERS

The Exclusive-OR is the heart of an adder system. Figure 11 shows 4-bits of a binary adder with ripple carry.

BINARY ADDER WITH RIPPLE CARRY (4-Bits)

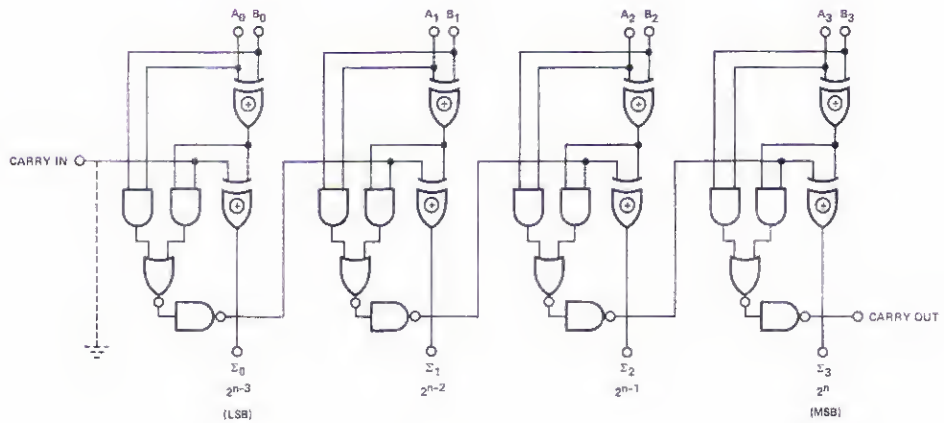


FIGURE 11

Each 2-wide 2-input AND-OR-INVERT gates shown in Figure 13 is 1/2 of a 7451 and each inverters 1/6 of 7404.

The binary adder shown in Figure 11 may be expanded to arbitrary length by simply continuing the pattern of interconnection shown. The CARRY IN term of the least significant bit (LSB) is grounded in actual implementation.

BCD ADDERS

Figure 12 shows the construction of a BCD adder. A second decade of addition would be constructed exactly as shown in Figure 12. The CARRY IN term of the least significant decade is grounded in actual implementation. MSI implementations, the 82S82 and 82S83 BCD arithmetic unit and the 82S82 and 82S83 BCD Adder are also available from Signetics.

BCD ADDER WITH RIPPLE CARRY (ONE DECADE)

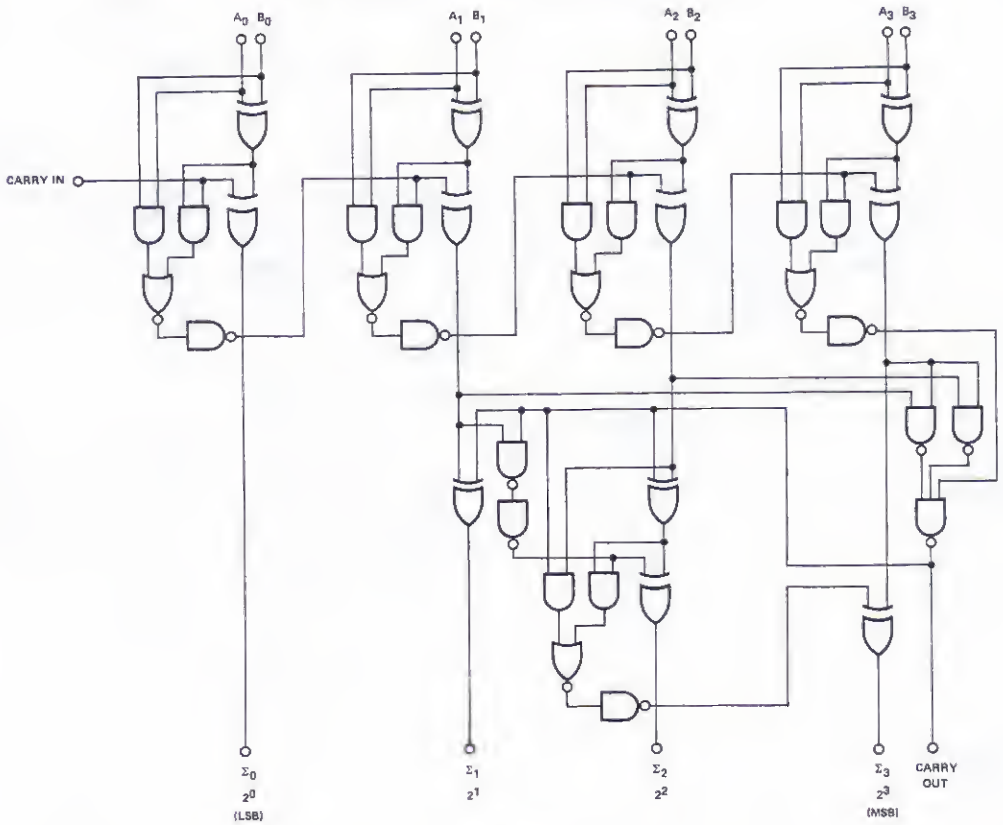


FIGURE 12

Each 2-wide, 2-input AND-OR-INVERT gate shown in Figure 12 may be 1/2 7451. Each inverter shown is 1/6 7404. Each 2-input NAND may be 1/4 7400. The 3-input NAND may be 1/3 7410.

CONDITIONAL COMPLEMENTORS

ADD-SUBTRACT subsystems require the ability to present information to the inputs of the adder in its TRUE form for addition and in its COMPLEMENT form for subtraction.

The Exclusive-OR may be used to implement a 4-bit conditional complementor as shown in Figure 13.

The Conditional Complementor may be expanded by connecting the COMPLEMENT inputs together. The designer should consider the additional fan-out required to drive the COMPLEMENT input on expanded Conditional Complementors designed with 8241's. The gate driving the COMPLEMENT input of Figure 15 must sink 12.8mA at V_{OUT} = "0" and source 200μA at V_{OUT} = "1".

4-BIT CONDITIONAL COMPLEMENTOR

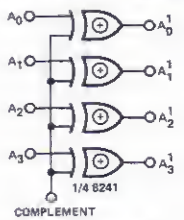


FIGURE 13

TRUTH TABLE

INPUTS		OUTPUT
Complement	A_i	A_i
0	0	A_i
0	1	A_i
1	0	$\overline{A_i}$
1	1	$\overline{A_i}$

EIGHT-BIT POSITION SCALER

INTRODUCTION

The 8243 Eight-Bit Position Scaler is an MSI array of approximately 70 gate complexity designed with TTL techniques. Its primary function is to scale (asynchronously shift) data a given number of positions determined by a 3-bit binary selector code. For system flexibility and easy array expansion INHIBIT and ENABLE inputs are provided.

The 8243's principal advantages over conventional shift registers are higher speed of operation and lower complexity of peripheral logic to perform a scale function. Any scaling operation performed with the 8243 is determined by fixed gate delays whereas the speed of shift registers for an equivalent operation is a function of the necessary clock pulses as well as propagation delays.

GENERAL DESCRIPTION

The 8243 Scaler may be used wherever any shift function is required without the need for internal storage. There are eight data inputs (I_0 through I_7) which are related to the eight outputs (O_0 through O_7) by the binary value on the select lines (S_0, S_1, S_2). A 3-bit binary address scales the data the desired number of positions in accordance with the truth table, TABLE 1.

At scale select of binary zero (000), or zero shift, all 8 data bits are transferred and inverted to their respective outputs (I_0 to O_0, I_1 to O_1, ..., I_n to O_n). At scale select of binary one (001) each input bit, I_n will appear shifted and inverted at the next lower order output O_{n-1}. However, input I_0 is lost and output O_7 is forced to a logical "1". This process continues up to the highest address, binary seven (111)

LOGIC DIAGRAM

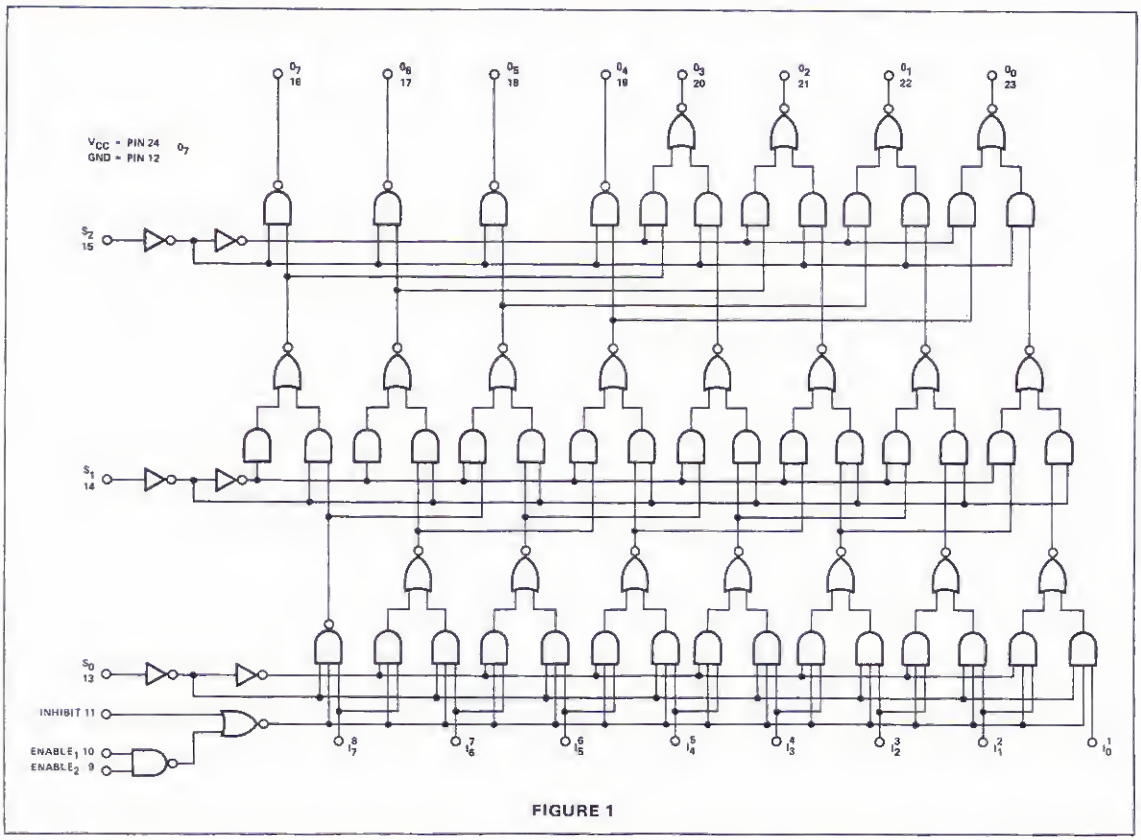


FIGURE 1

TRUTH TABLE OF 8243 SCALER

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
		0	0	0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
0	1	1	0	0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I
0	1	0	1	0	I_2	I_3	I_4	I_5	I_6	I_7	I	I
0	1	1	1	0	I_3	I_4	I_5	I_6	I_7	I	I	I
0	1	0	0	1	I_4	I_5	I_6	I_7	I	I	I	I
0	1	1	0	1	I_5	I_6	I_7	I	I	I	I	I
0	1	0	1	1	I_6	I_7	I	I	I	I	I	I
0	1	1	1	1	I_7	I	I	I	I	I	I	I
1	X	X	X	X	I	I	I	I	I	I	I	I
X	0	X	X	X	I	I	I	I	I	I	I	I

X indicates either Logic "1" or Logic "0" may be present.

TABLE 1

where input I_7 is inverted and connected to output O_0 while the remaining outputs (O_1 through O_7) are forced to a logical "1".

It may be noted from Table 1 that the scaler can be used to scale data left or right since assignment of a weighting factor to the data bits is arbitrary. Thus, the scaling action as shown in Table 1 suggests an asynchronous shift left action if I_7 is the rightmost bit. But if a different topographical arrangement of the Truth Table is chosen, where I_7 is the leftmost bit, scaling of the data bits will be a shift right process.

Output O_0 is never forced to a logical "1" by a binary address on the scale select lines and as such it can be used as the output of an 8-bit multiplexer. Similarly, input I_7 is always connected to some output and can therefore be used as an input of an 8-bit demultiplexer.

The 8243 has open collector outputs to facilitate expansion to larger scaling arrays. By means of the INHIBIT and ENABLE lines all outputs can be forced to a logical "1" state, effectively disabling the unit. (Disabled=INH + $\overline{EN}_1$ + $\overline{EN}_2$). When the 8243 is disabled, the data input "0" loading is reduced to less than −100μA. Therefore, large scaler arrays may be implemented without encountering the usual current sink capability limitations of the driver.

BASIC SCALER ARRAY EXPANSION

Any number of bits may be shifted over as many positions as desired by simply making a large enough array using only 8243 8-bit position scalers. (However buffer gates may be necessary for very large arrays). It is important to note that no matter how large the array becomes, the delay for any bit shift (scaling) operation is always the same. Figure 2 shows the basic step in array expansion. Input bits, A_i, are made available at outputs B_0 through B_{15} as determined by the scaling address. The results are shown in the truth table (Table 2) indicating that eight bits of input data appears inverted at the outputs and can be shifted a maximum of seven positions. This idea is used in all expansions for shift left or shift right scaling arrays. Since the outputs are open collector they may be bussed together in larger arrays or circular shift implementations as it will be shown in the following discussion.

BIDIRECTIONAL 7-POSITION SCALER AND SEQUENCE GENERATOR

To illustrate the bidirectional shift capability of the scaler, two 8243's are interconnected as shown in Figure 3a. By means of two control lines data may be scaled right or scaled left. Since data can be scaled around in both directions, a circular sequence can be generated in accordance with the truth table in Table 2.

Scaling to the right is done by Unit B while Unit A is effectively disabled. Similarly, for scaling data to the left Unit A is enabled while Unit B is inhibited. To effect the circular sequence generation or scale around action both 8243's are enabled. The exclusive-OR circuits act as conditional complementers for all operations.

ARRAY EXPANSION

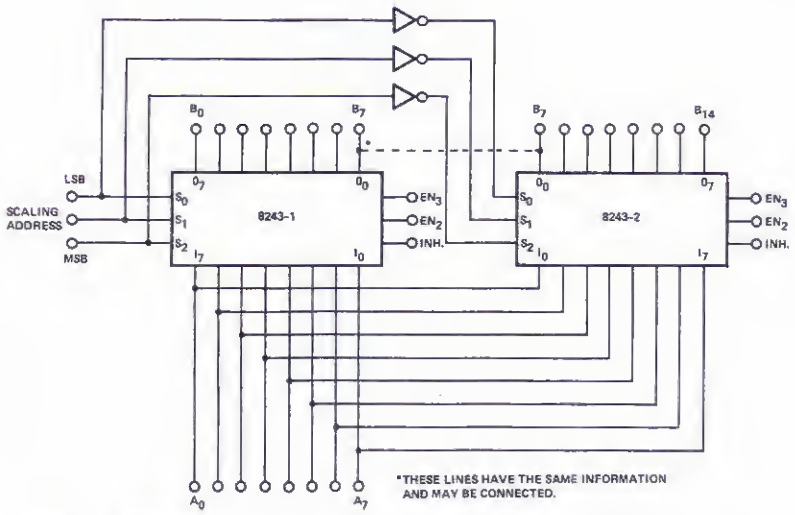


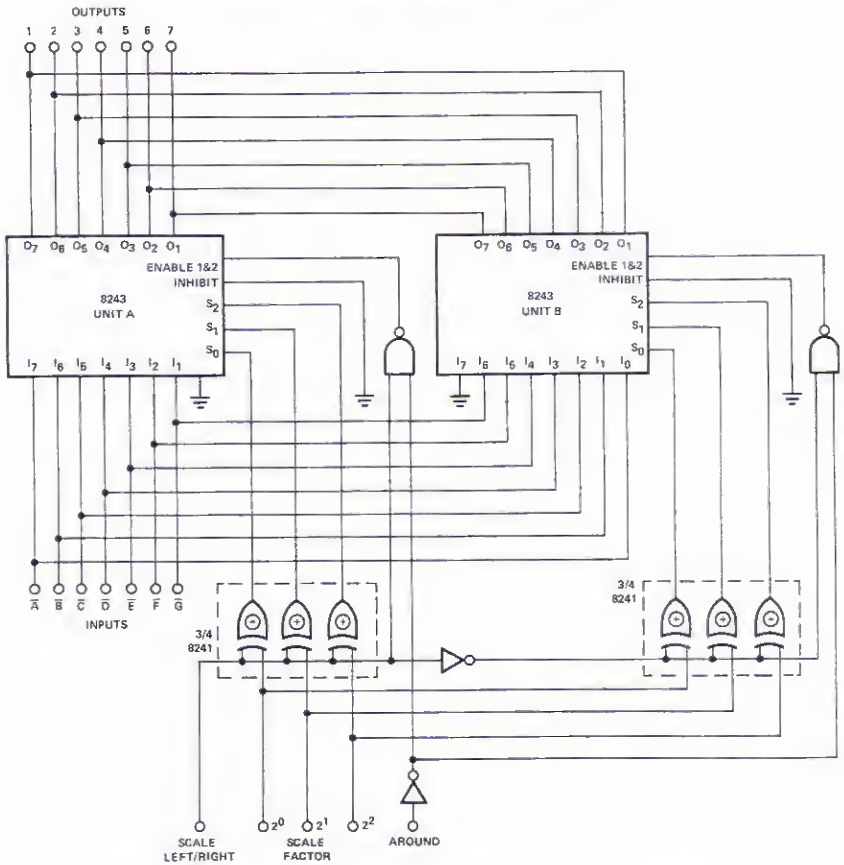
FIGURE 2

TRUTH TABLE FOR ARRAY EXPANSION

SCALE ADDRESS			8243-1								8243-2							
MSB		LSB	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}
0	0	0	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_7$	1	1	1	1	1	1	1
0	0	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_6$	$\overline{A}_7$	1	1	1	1	1	1
0	1	0	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1	1	1	1
0	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1	1	1
1	0	0	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1	1
1	0	1	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1
1	1	0	1	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1
1	1	1	1	1	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$

TABLE 2

BIDIRECTIONAL 7-POSITION SHIFTER



a.

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	C	E	F	G	
1	1	A	B	C	D	E	F	SCALE
2	1	1	A	B	C	D	E	RIGHT
3	1	1	1	A	B	C	D	
4	1	1	1	1	A	B	C	Scale = 0
5	1	1	1	1	1	A	B	Around = 0
6	1	1	1	1	1	1	A	
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	
1	B	C	D	E	F	G	1	SCALE
2	C	D	E	F	G	1	1	LEFT
3	D	E	F	G	1	1	1	
4	E	F	G	1	1	1	1	Scale = 1
5	F	G	1	1	1	1	1	Around = 0
6	G	1	1	1	1	1	1	
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	
1	G	A	B	C	D	E	F	SCALE
2	F	G	A	B	C	D	E	RIGHT &
3	E	F	G	A	B	C	D	AROUND
4	D	E	F	G	A	B	C	
5	C	D	E	F	G	A	B	Scale = 0
6	B	C	D	E	F	G	A	Around = 1
7	A	B	C	D	E	F	G	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	
1	B	C	D	E	F	G	A	SCALE
2	C	D	E	F	G	A	B	LEFT &
3	D	E	F	G	A	B	C	AROUND
4	E	F	G	A	B	C	D	
5	F	G	A	B	C	D	E	Scale = 1
6	G	A	B	C	D	E	F	Around = 1
7	A	B	C	D	E	F	G	

b.

FIGURE 3

FOUR-BIT BINARY CODE FOR 16 POSITIONS SCALE RIGHT

SCALE SELECT	FOUR BIT BINARY CODE				POSITION OF 1st EIGHT BITS							
	S_3	S_2	S_1	S_0	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A7}$
0	0	0	0	0	B0	B1	B2	B3	B4	B5	B6	B7
1	0	0	0	1	B1	B2	B3	B4	B5	B6	B7	B8
2	0	0	1	0	B2	B3	B4	B5	B6	B7	B8	B9
3	0	0	1	1	B3	B4	B5	B6	B7	B8	B9	B10
4	0	1	0	0	B4	B5	B6	B7	B8	B9	B10	B11
5	0	1	0	1	B5	B6	B7	B8	B9	B10	B11	B12
6	0	1	1	0	B6	B7	B8	B9	B10	B11	B12	B13
7	0	1	1	1	B7	B8	B9	B10	B11	B12	B13	B14
8	1	0	0	0	B8	B9	B10	B11	B12	B13	B14	B15
9	1	0	0	1	B9	B10	B11	B12	B13	B14	B15	B16
10	1	0	1	0	B10	B11	B12	B13	B14	B15	B16	B17
11	1	0	1	1	B11	B12	B13	B14	B15	B16	B17	B18
12	1	1	0	0	B12	B 13	B14	B15	B16	B17	B18	B19
13	1	1	0	1	B13	B14	B15	B16	B17	B18	B19	B10
14	1	1	1	0	B14	B15	B16	B17	B18	B19	B20	B21
15	1	1	1	1	B15	B16	B17	B18	B19	B20	B21	B22

TABLE 3

LARGE SCALING ARRAYS

24 BIT 16 POSITION SHIFT RIGHT ARRAY SCALING

The 8243 scaler may be expanded in both bits and positions in accordance with Figure 3. A Shift Right Scaling Array for 24 bits and 16 positions is shown in Figure 4. The data word is inverted and scaled (shifted) according to Table 2.

If bit S_3 of the binary selector code is connected to one of the ENABLE inputs or S_3 is connected to the INHIBIT of the upper row of 8243's in Figure 4, they will be disabled during the first eight scale addresses and activated for the second eight scale addresses. If at the same time S_3 is connected to the INHIBIT or S_3 is connected to one of the ENABLE inputs of the lower 8243's, they will be enabled during the first eight scale addresses and disabled for the second eight scale addresses.

Both connections of the selector bit S_3 result in the lower 8243's scaling the first eight scale positions and the upper 8243's scaling the second eight positions.

24-BIT 8-POSITION SHIFT RIGHT/LEFT SCALING ARRAY

The 8243 may be connected as a Shift Right/shift Left Scaler. An Array for 24 bits and 8 positions in each direction is shown in Figure 5.

If S_3 is connected to the INHIBIT of the upper 8243's, they will be disabled during the first eight scale addresses and activated for the second eight scale addresses. If at the same time S_3 is connected to the INHIBIT of the lower 8243's, they will be enabled during the first eight scale addresses and disabled for the second eight scale addresses.

As a result, the lower 8243's perform a "scale-left" function when any one of the first eight scale addresses is selected. Alternately, the upper 8243's perform a "scale-right" function when any one of the last eight scale addresses is selected. The word is scaled (shifted) in accordance with Table 4.

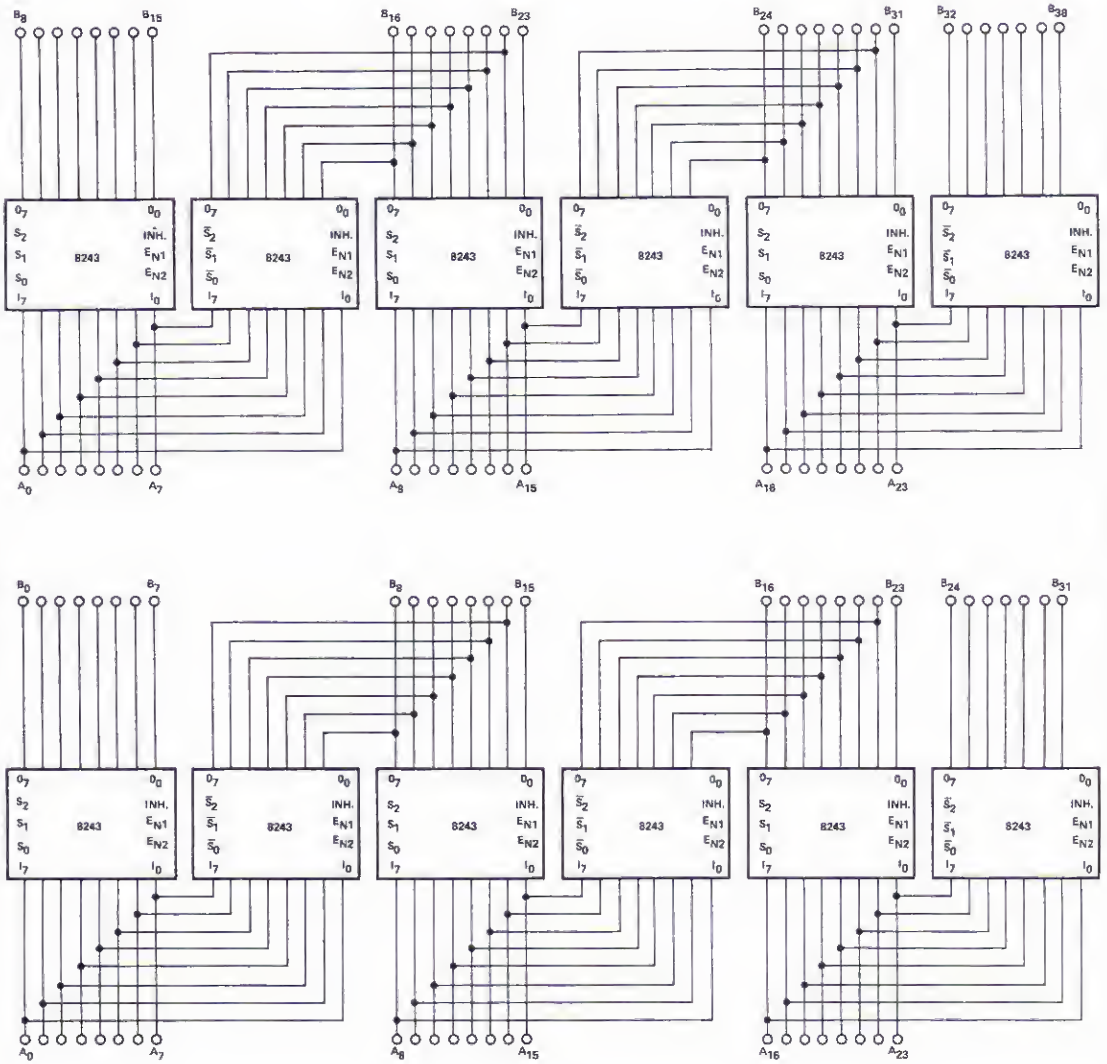
24-BIT 16-POSITION SHIFT LEFT SCALING ARRAY

The 8243 may be connected as a Shift Left Scaler. For 24 bits and 16 positions the connections are shown in Figure 6.

If S_3 is connected to the INHIBIT of the upper 8243's, they will be enabled during the first eight scale addresses and disabled during the second eight scale addresses. If at the same time $\overline{S_3}$ is connected to the INHIBIT of the lower 8243's they will be disabled during the first eight scale addresses and enabled during the second eight scale addresses.

As a result, the upper 8243's are scaling the first eight positions and the lower 8243's are scaling the second eight positions. The word is scaled (shifted) as shown in Table 5.

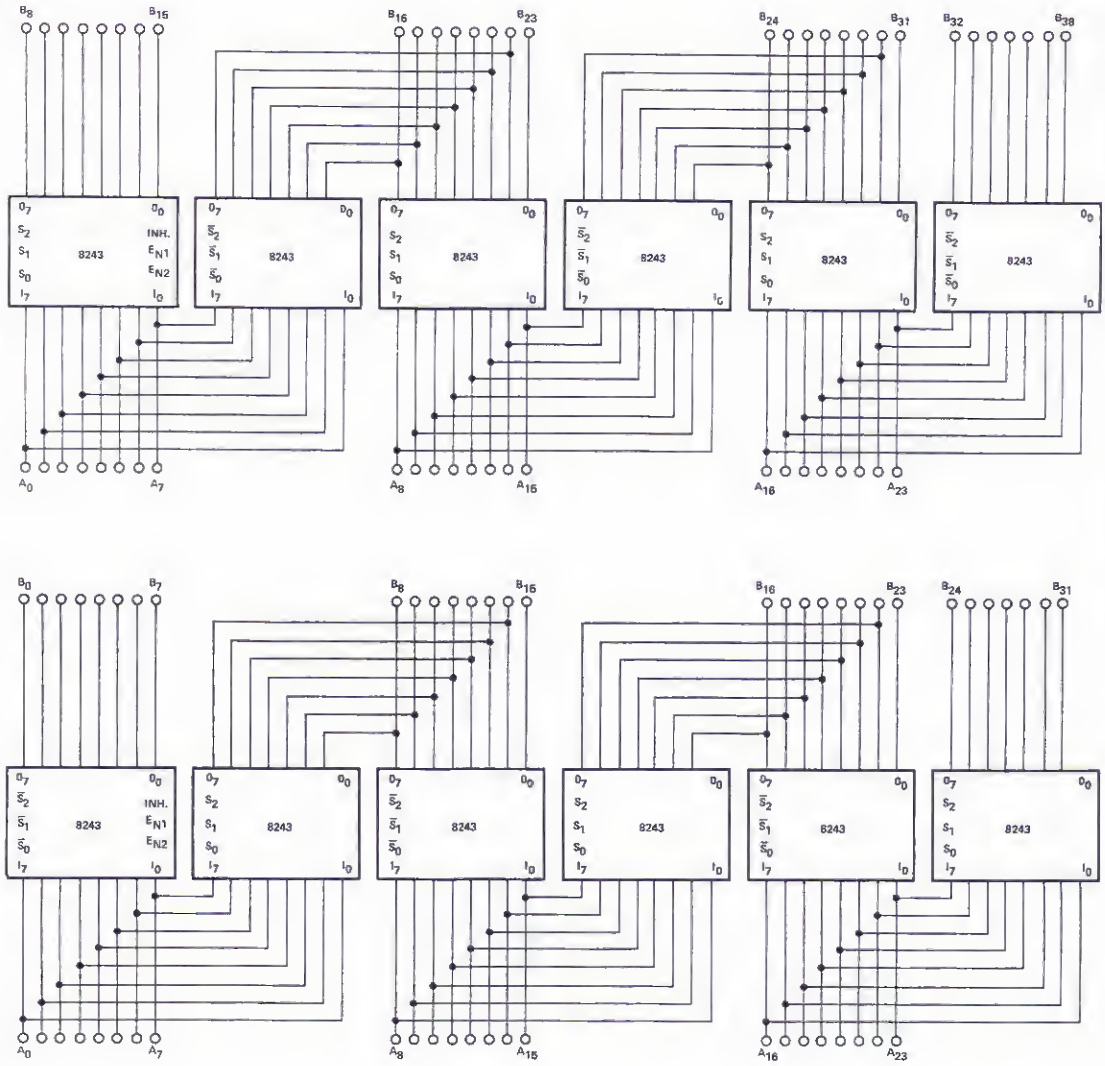
24-BIT 16 POSITION SHIFT RIGHT SCALING ARRAY



ENABLE GATES

FIGURE 4

24-BIT 8 POSITION SHIFT RIGHT/LEFT SCALING ARRAY



ENABLE GATES

FIGURE 5

FOUR-BIT BINARY CODE FOR SCALE RIGHT/LEFT

SHIFT LEFT / SHIFT RIGHT	SCALE SELECT	FOUR BIT BINARY CODE				POSITION OF 1ST EIGHT BITS							
		S_3	S_2	S_1	S_0	$\bar{A}_0$	$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$
SHIFT LEFT	0	0	0	0	0	B7	B8	B9	B10	B11	B12	B13	B14
	1	0	0	0	1	B6	B7	B8	B9	B10	B11	B12	B13
	2	0	0	1	0	B5	B6	B7	B8	B9	B10	B11	B12
	3	0	0	1	1	B4	B5	B6	B7	B8	B9	B10	B11
	4	0	1	0	0	B3	B4	B5	B6	B7	B8	B9	B10
	5	0	1	0	1	B2	B3	B4	B5	B6	B7	B8	B9
	6	0	1	1	0	B1	B2	B3	B4	B5	B6	B7	B8
	7	0	1	1	1	B0	B1	B2	B3	B4	B5	B6	B7
SHIFT RIGHT	8	1	0	0	0	B8	B9	B10	B11	B12	B13	B14	B15
	9	1	0	0	1	B9	B10	B11	B12	B13	B14	B15	B16
	10	1	0	1	0	B10	B11	B12	B13	B14	B15	B16	B17
	11	1	0	1	1	B11	B12	B13	B14	B15	B16	B17	B18
	12	1	1	0	0	B12	B13	B14	B15	B16	B17	B18	B19
	13	1	1	0	1	B13	B14	B15	B16	B17	B18	B19	B20
	14	1	1	1	0	B14	B15	B16	B17	B18	B19	B20	B21
	15	1	1	1	1	B15	B16	B17	B18	B19	B20	B21	B22

TABLE 4

FOUR-BIT BINARY CODE FOR 16-POSITION SCALE LEFT

SCALE SELECT	FOUR BIT BINARY CODE				POSITION OF 1ST EIGHT BITS							
	S_3	S_2	S_1	S_0	$\bar{A}_0$	$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$
0	0	0	0	0	B15	B16	B17	B18	B19	B20	B21	B22
1	0	0	0	1	B14	B15	B16	B17	B18	B19	B20	B21
2	0	0	1	0	B13	B14	B15	B16	B17	B18	B19	B20
3	0	0	1	1	B12	B13	B14	B15	B16	B17	B18	B19
4	0	1	0	0	B11	B12	B13	B14	B15	B16	B17	B18
5	0	1	0	1	B10	B11	B12	B13	B14	B15	B16	B17
6	0	1	1	0	B9	B10	B11	B12	B13	B14	B15	B16
7	0	1	1	1	B8	B9	B10	B11	B12	B13	B14	B15
8	1	0	0	0	B7	B8	B9	B10	B11	B12	B13	B14
9	1	0	0	1	B6	B7	B8	B9	B10	B11	B12	B13
10	1	0	1	0	B5	B6	B7	B8	B9	B10	B11	B12
11	1	0	1	1	B4	B5	B6	B7	B8	B9	B10	B11
12	1	1	0	0	B3	B4	B5	B6	B7	B8	B9	B10
13	1	1	0	1	B2	B3	B4	B5	B6	B7	B8	B9
14	1	1	1	0	B1	B2	B3	B4	B5	B6	B7	B8
15	1	1	1	1	B0	B1	B2	B3	B4	B5	B6	B7

TABLE 5

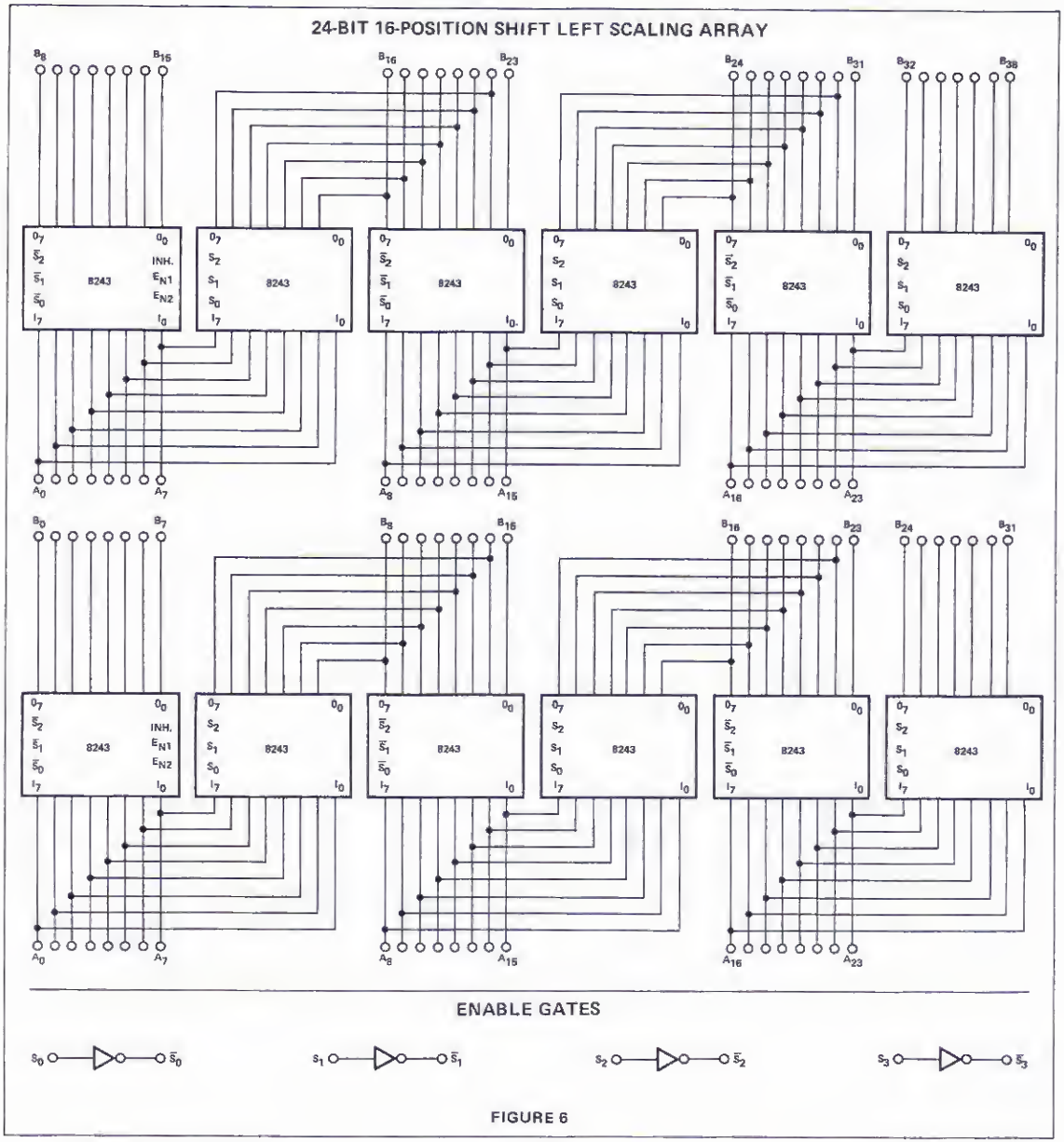


FIGURE 6

DEMULTIPLEXERS

The 8243 is very useful in applications where demultiplexing of digital data is desired. Two examples are shown in Figure 7 and Figure 8.

Figure 7 shows the 8243 used to demultiplex data from one line to as many as eight lines simultaneously. The number of output lines selected is determined by the 3-bit binary code on the SELECT lines as given in Table 6.

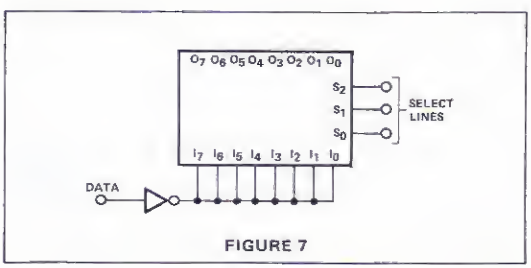


FIGURE 7

DEMULTIPLEX ONE TO EIGHT SIMULTANEOUSLY

SCALE SELECT	THREE BIT BINARY CODE			OUTPUT							
	S_2	S_1	S_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	0	Data	Data	Data	Data	Data	Data	Data	Data
1	0	0	1	Data	Data	Data	Data	Data	Data	Data	1
2	0	1	0	Data	Data	Data	Data	Data	Data	1	1
3	0	1	1	Data	Data	Data	Data	Data	1	1	1
4	1	0	0	Data	Data	Data	Data	1	1	1	1
5	1	0	1	Data	Data	Data	1	1	1	1	1
6	1	1	0	Data	Data	1	1	1	1	1	1
7	1	1	1	Data	1	1	1	1	1	1	1

TABLE 6

DEMULTIPLEX ONE TO ONE OF EIGHT

SCALE SELECT	THREE BIT BINARY CODE			OUTPUT							
	S_2	S_1	S_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	0	1	1	1	1	1	1	1	Data
1	0	0	1	1	1	1	1	1	1	Data	1
2	0	1	0	1	1	1	1	1	Data	1	1
3	0	1	1	1	1	1	1	Data	1	1	1
4	1	0	0	1	1	1	Data	1	1	1	1
5	1	0	1	1	1	Data	1	1	1	1	1
6	1	1	0	1	Data	1	1	1	1	1	1
7	1	1	1	Data	1	1	1	1	1	1	1

TABLE 7

Another demultiplexer application which may be considered a serial to parallel converter can be implemented using an 8243 as shown in Figure 8. The Truth Table is given in Table 7.

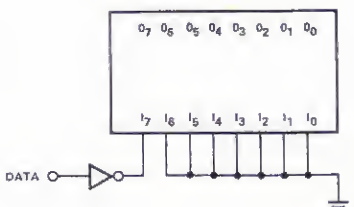


FIGURE 8

R_L MIN/MAX CALCULATIONS FOR BARE COLLECTOR DEVICES

In choosing the proper load resistor, consideration must be given to the number of inputs as well as the number of outputs tied together. For a selected "1" level the maximum load resistor becomes:

$$R_L \text{ max} = \frac{V_{CC} \text{ min} - V_{\text{"1" min}}}{\text{Total Leakage Current}}$$

If N is the total number of open collectors to be tied together and M is the total number of inputs to be driven, the total leakage becomes:

$$I_L \text{ total} = M\ (I_{\text{"1" in}}) + N\ (I_{\text{"1" out}})$$

and the maximum load resistor becomes:

$$R_L \text{ max} = \frac{V_{CC} \text{ min} - V_{\text{"1" min}}}{M_{(I_{\text{"1" in}})} + {}^{N}(I_{\text{"1" out}})}$$

The minimum load resistor becomes:

$$R_L \text{ min} = \frac{V_{CC} \text{ max} - V_{\text{"0" out}}}{I \text{ sink} - M\ (I_{\text{"0" in}})}$$

The input capacitance of the driven devices plus the output caacitance of the driving devices plus the interconnect wiring capacitance in conjunction with R_L will be determined by the speed power tradeoff of the system.

Example:

If 8243 outputs are paralleled as shown in Figure 9 to perform collector logic, the pullup resistor R_L is found as follows:

From the Electrical Specifications
V_{CC} = 5.0V ±5%
8243 Scaler
I "1" out = 150μA
V "0" out = 0.4V at I_{sink} = 12.8 mA
N = 3; number of collectors to be tied together
8800 NAND Gate
I "1" in = 25μA
I "0" in = 1.6 mA
M = 4; number of inputs tied together
Select Min "1" output level = 2.6V

$$R_L \text{ max} = \frac{(4.75 - 2.6)V}{4(25\mu A) + 3(150\mu A)} = \frac{2.15V}{550\mu A} = 3.91K \text{ max}$$

$$R_L \text{ min} = \frac{(5.25 - 0.4)V}{12.8mA - 4(1.6mA)} = \frac{4.85V}{6.4mA} = 760\Omega \text{ min}$$

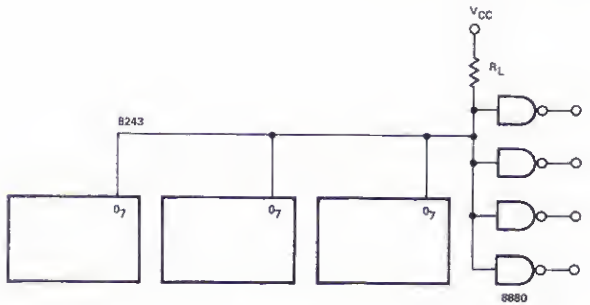


FIGURE 9

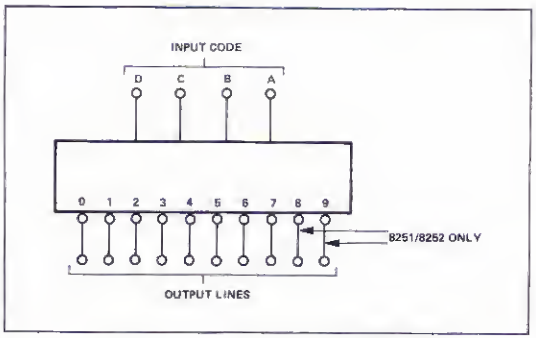
INTRODUCTION

The Decade Decoders, 8251/52, accept a four bit input code and activates one of the ten mutually exclusive outputs.

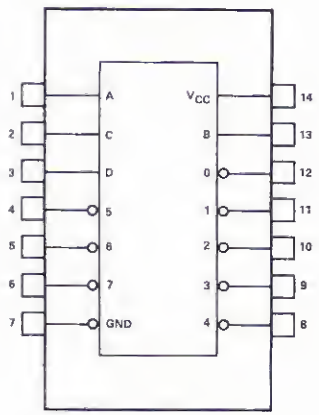
The Octal Decoder, 8250, decodes an octal number (3 bit), applied to the input pins and one of the eight outputs will be activated, representing the decoded number.

The Octal/Decade Decoders are very flexible devices for decoding and logic conversion applications.

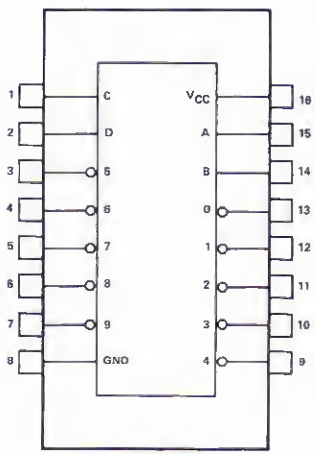
The 8252 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs.



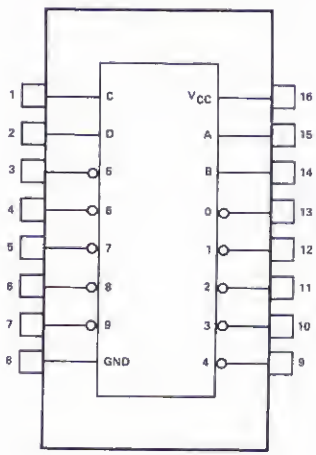
8250A



8251B

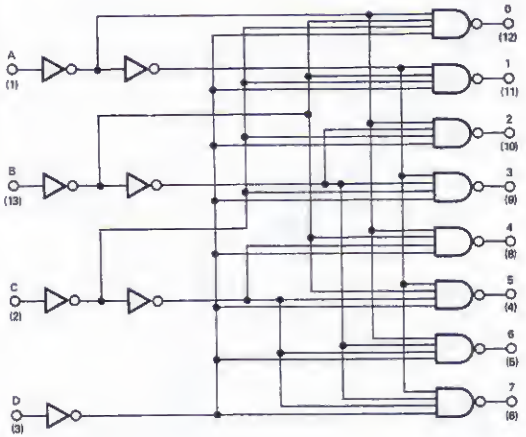


8252B



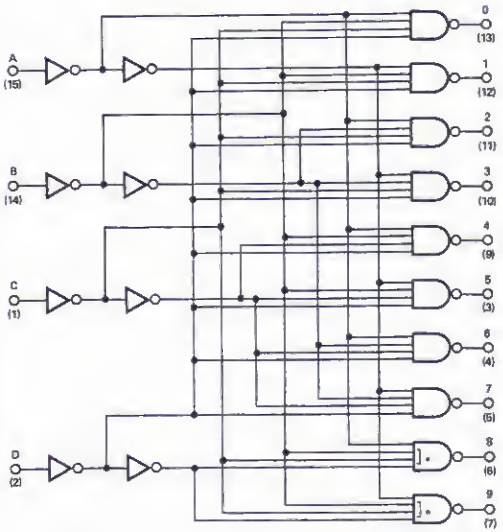
LOGIC DIAGRAMS

8250



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for
14 Pin Dual-in-Line Package

8251/8252



V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers for
16 Pin Dual-in-Line Package

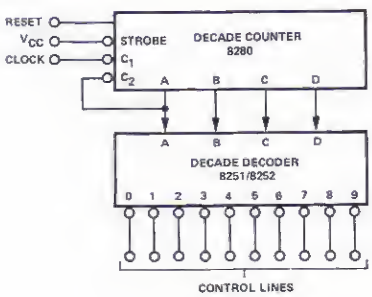
*Connections made on 8252 only

TRUTH TABLE

				OUTPUT STATE										
INPUT STATE				8250								8251		8252	
A	B	C	D	0	1	2	3	4	5	6	7	8	9	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1

DECODER APPLICATIONS

The Decade Decoder (8251, 8252) may be used conveniently in conjunction with the Decade Counter (8280). The change of the different states is controlled by the clock-signal.



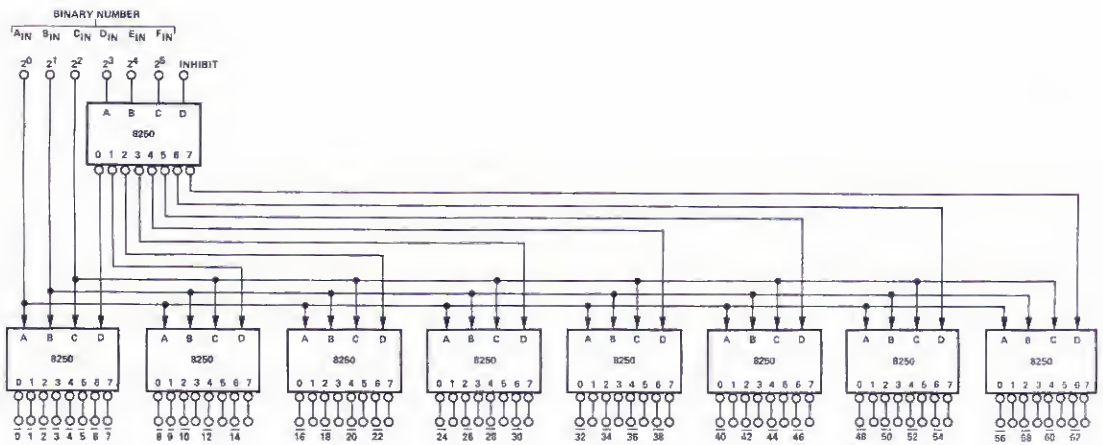
OCTAL DECODER (8250)

The Octal Decoder decodes the binary numbers 0 to 7 which are applied to the pins (CBA). The D-input provides gating of the input. When D is high, decoding is inhibited — when D is low, decoding occurs. This is indicated in the truth table.

The Octal Decoder can be expanded to layer arrays. The next example shows a "One-of-64 Decoding."

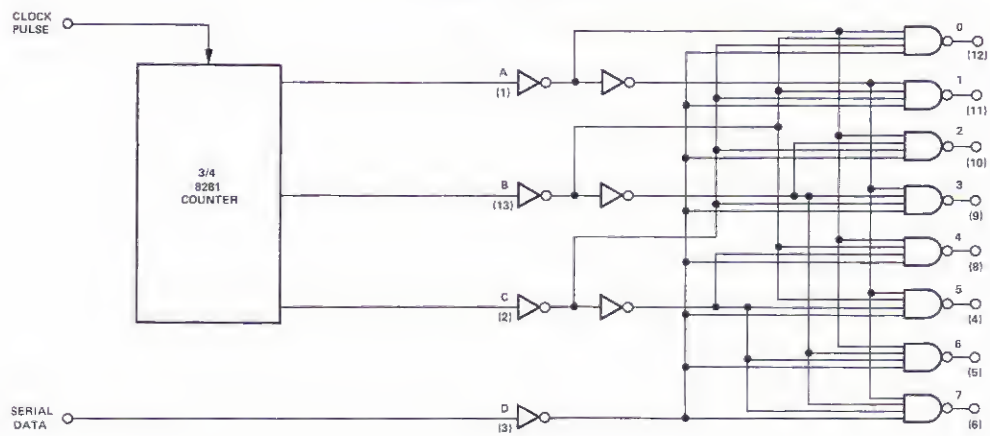
Note that the decoder device with inputs D_{in}, E_{in}, F_{in} controls the other eight octal decoders by the D-inputs. The decoding process may be stopped by the Inhibit line.

ONE-OF-64 DECODING



The 8250 Octal Decoder can also be used to demultiplex bits of information from a serial data stream. Used with an 8281 counter, the input data is routed to outputs "0" through "7" sequentially.

DEMULTIPLEXER



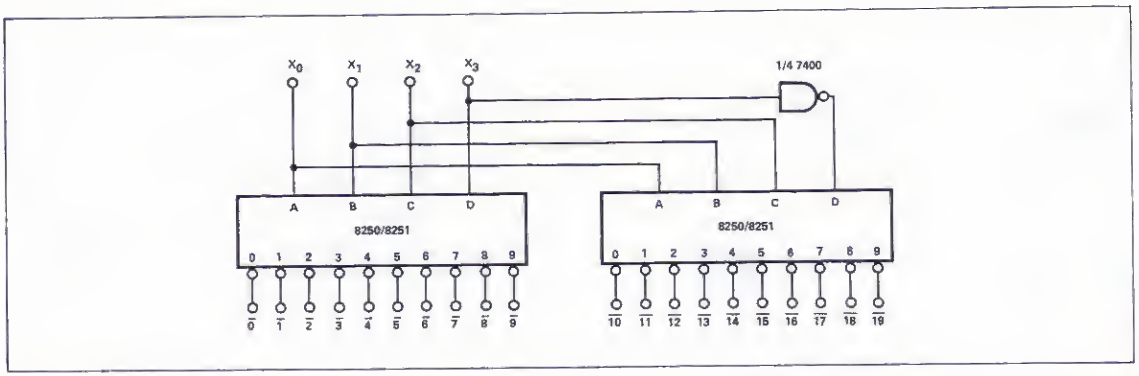
V_{CC} = (14)
GND = (7)
( ) = DENOTES PIN NUMBERS FOR 14 PIN DUAL-IN-LINE PACKAGE

8250

ARBITRARY 4-BIT DECODING

Using two Decoders every 4-bit code may be decoded.

As an example we apply the excess–3 code to the pins (X_3, X_2, X_1, X_0) and examine the generated outputs.



DECIMAL QUANTITY	EXCESS -3 CODE X_3 X_2 X_1 X_0	ACTIVATED OUTPUTS (NOT TRUE LEVELS)	USEFUL OUTPUTS (NOT TRUE LEVELS)
0	0 0 1 1	3 19	3 -
1	0 1 0 0	4 18	4 -
2	0 1 0 1	5 19	5 -
3	0 1 1 0	6 18	6 -
4	0 1 1 1	7 19	7 -
5	1 0 0 0	8 10	- 10
6	1 0 0 1	9 11	- 11
7	1 0 1 0	8 12	- 12
8	1 0 1 1	9 13	- 13
9	1 1 0 0	8 14	- 14

The well-defined outputs are listed at the right most column.

In the next table other codes will be shown with their corresponding outputs.

DECIMAL QUANTITY	WELL-DEFINED OUTPUTS (Not true levels) BINARY CODED DECIMAL	AIKEN CODE 2*4 2 1	4 2* 2 1
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	5
4	4	4	6
5	5	13	11
6	6	14	12
7	7	15	15
8	8 10	16	16
9	9 11	17	17

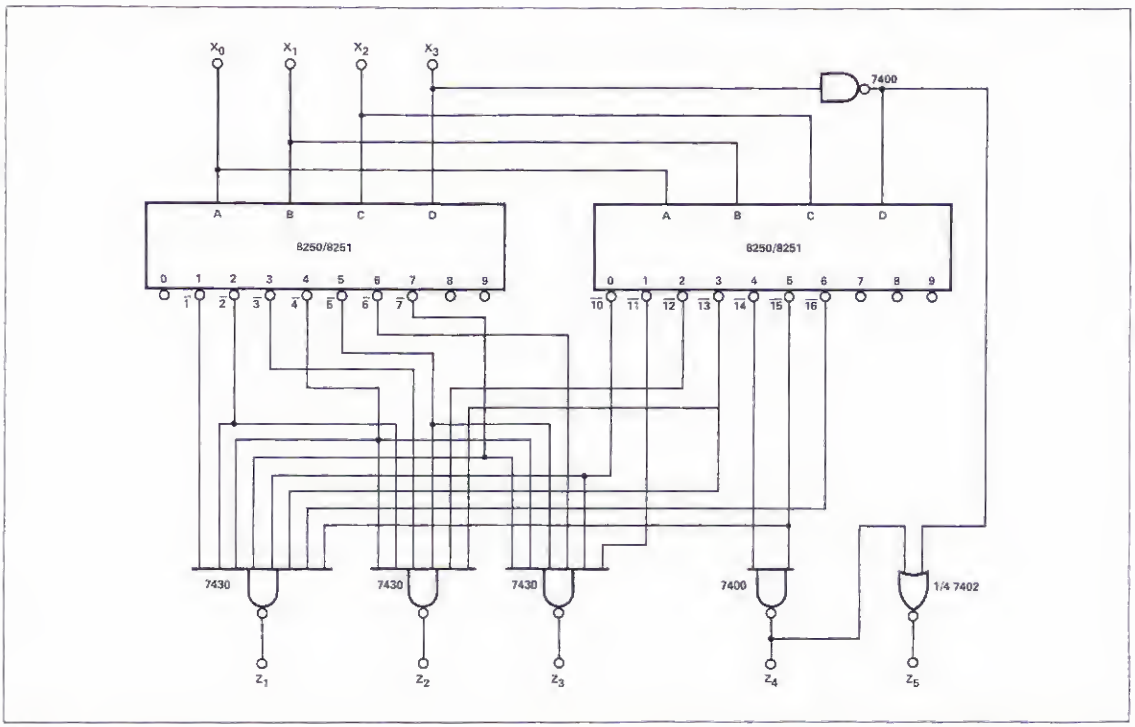
CODE CONVERSION

The Decade Decoders are also useful in code conversion applications. As an example let us convert the Gray Code into the BCD Code. First we apply the Gray Code to the pins of two Decade Decoders. The activated outputs are listed in the following table.

Now the Decoder outputs will be used to form the BCD Code.

$$Z_4 = 14 + 15$$
$$Z_3 = 6 + 7 + 5 + 4 + 11 + 10$$
$$Z_2 = 3 + 2 + 5 + 4 + 12 + 13$$
$$Z_1 = 1 + 2 + 7 + 4 + 15 + 16 + 13 + 10$$
$$Z_5 = \overline{X_3 + Z_4}$$

DECIMAL QUANTITY	GRAY REFLECTED CODE X_3	X_2	X_1	X_0	DECODER OUTPUTS	2 DECADES BINARY CODED DECIMAL (BCD) Z_5	Z_4	Z_3	Z_2	Z_1
0	0	0	0	0	$\overline{0}$	0 0 0 0	0	0	0	0
1	0	0	0	1	$\overline{1}$	0 0 0 0	0	0	0	1
2	0	0	1	1	$\overline{3}$	0 0 0 0	0	0	1	0
3	0	0	1	0	$\overline{2}$	0 0 0 0	0	0	1	1
4	0	1	1	0	$\overline{6}$	0 0 0 0	0	1	0	0
5	0	1	1	1	$\overline{7}$	0 0 0 0	0	1	0	1
6	0	1	0	1	$\overline{5}$	0 0 0 0	0	1	1	0
7	0	1	0	0	$\overline{4}$	0 0 0 0	0	1	1	1
8	1	1	0	0	$\overline{14}$	0 0 0 0	1	0	0	0
9	1	1	0	1	$\overline{15}$	0 0 0 0	1	0	0	1
10	1	1	1	1	$\overline{17}$	0 0 0 1	0	0	0	0
11	1	1	1	0	$\overline{16}$	0 0 0 1	0	0	0	1
12	1	0	1	0	$\overline{12}$	0 0 0 1	0	0	1	0
13	1	0	1	1	$\overline{13}$	0 0 0 1	0	0	1	1
14	1	0	0	1	$\overline{11}$	0 0 0 1	0	1	0	0
15	1	0	0	0	$\overline{10}$	0 0 0 1	0	1	0	1



This configuration provides significant package count savings as shown in the table below.

PACKAGE COUNT WITH DECODERS		PACKAGE COUNT WITH STANDARD GATES	
8250	2	7420	4
7430	3	7430	1
7400	1/2	7400	2 - 3/4
7402	1/4	7410	2/3
		8875	1/3
Total	5 -3/4	Total	8 - 3/4

8250	Octal Decoder
7430	Single 8 input NAND
7420	Dual 4 input NAND
7410	Triple 3 input NAND
8875	Triple 3 input NOR
7400	Quad 2 input NAND
7402	Quad 2 input NOR

INTRODUCTION

The 8260 Arithmetic Logic Element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. As a four-bit adder, the 8260 permits parallel addition of four sets of data with the sum output being available in 20ns (typical). High speed operation of this device is achieved through the use of TTL circuitry providing low propagation delays and high noise immunity.

The 8260 series can be used in the ripple carry mode between adders, in systems where package count must be minimized with some sacrifice in speed. For anticipated carry beyond 4 stages, FAST CARRY EXTENDER (8261) packages are used. For example, using 8260 and 8261 elements, a 64-stage adder system, capable of adding two 64-bit numbers in less than 100ns, can be built with only 23 packages. Faster systems can be built by taking full advantage of look-ahead carry configurations. The 8260 may also be used as four mutually independent EQUIVALENCE or AND gates by proper addressing of the inhibit lines.

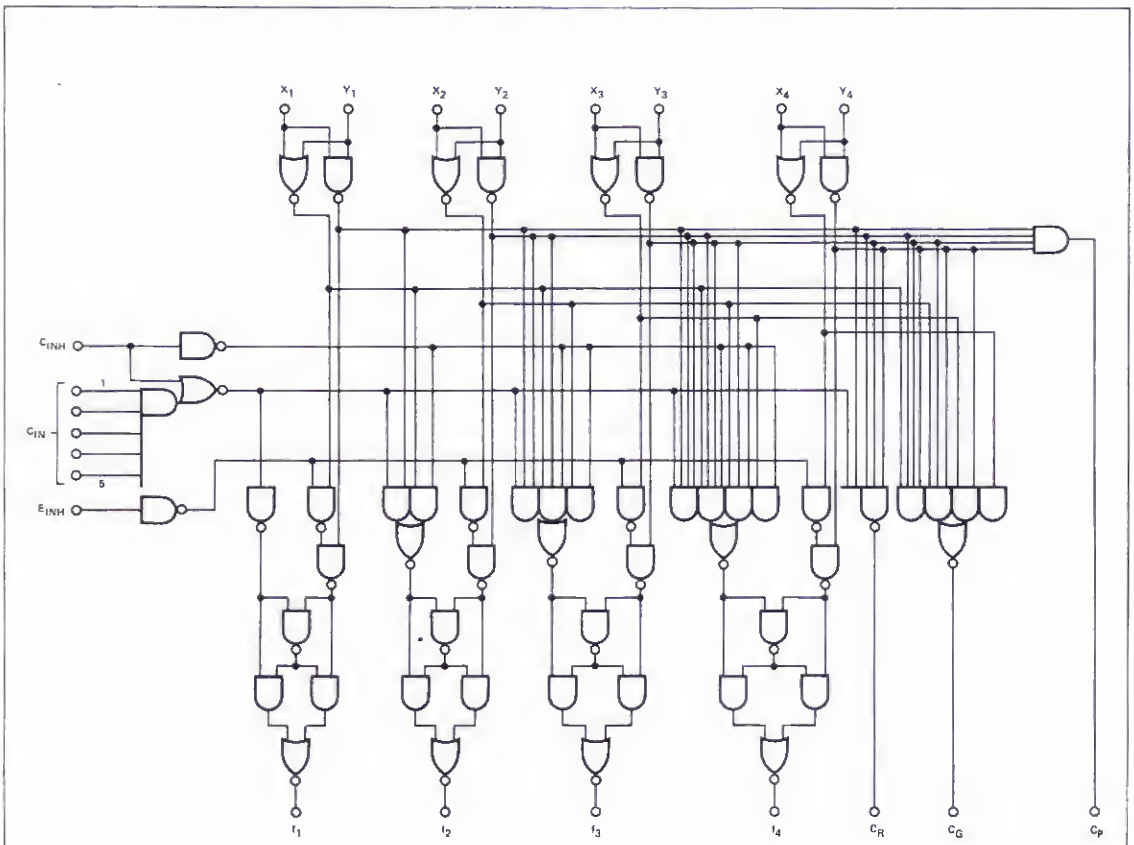


FIGURE 1

DESCRIPTION OF THE LOOK-AHEAD (or anticipated) CARRY PRINCIPLE

A standard parallel adder utilizing the ripple-through carry principle is shown in FIGURE 2.

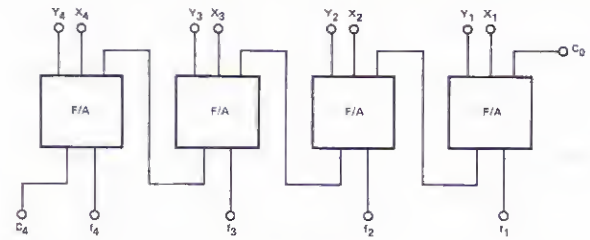


FIGURE 2

The correct sum is not available until the carry has propagated through the entire series of full adders. When adding long numbers, say 32 bits, this ripple time generally becomes the limiting factor on system speed.

One way of increasing system speed is by using the "look-ahead carry" technique. Additional logic circuitry is employed to look at the inputs to all preceding bit positions and determine what the carry input for each package will be without waiting for the information to propagate through all preceding positions.

The carry output of any n package is given by:

$$C_n = X_n Y_n + (X_n + Y_n) C_{n-1}$$

But then $C_n - 1$ can be similarly expressed such that all carries are written as functions of only the input bits and the carry into the least significant bit position. For the four stage adder example above:

$$C_1 = X_1Y_1 + (X_1 + Y_1) C_0$$

$$C_2 = Y_2Y_2 + (X_2 + Y_2) C_1 = X_2Y_2 + (X_2 + Y_2) [X_1Y_1 + (X_1 + Y_1) C_0]$$

$$C_3 = X_3Y_3 + (X_3 + Y_3) C_2 = X_3Y_3 + (X_3 + Y_3) [X_2Y_2 + (X_2 + Y_2) \quad X_1Y_1 + (X_1 + Y_1) C_0 \quad]$$

$$C_4 = X_4Y_4 + (X_4 + Y_4) C_3 = X_4Y_4 + (X_4 + Y_4) \quad X_3Y3 + (X_3 + Y_3) [X_2Y_2 + (X_2 + Y_2) \quad X_1Y_1 + (X_1 + Y_1) C_0 \quad]$$

The circuit shown in Figure 3 indicates how this logic can be utilized to provide the necessary carry information to each full adder.

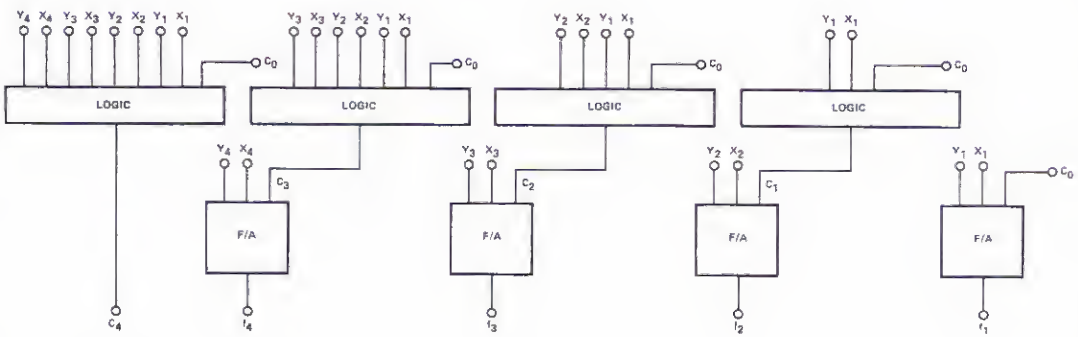


FIGURE 3

Referring to the simplified logic diagram of the 8260 (Figure 4), the anticipated carry is generated using two-level logic (shown shaded). That is, the carry information to any stage will be available within two gate propagation delays.

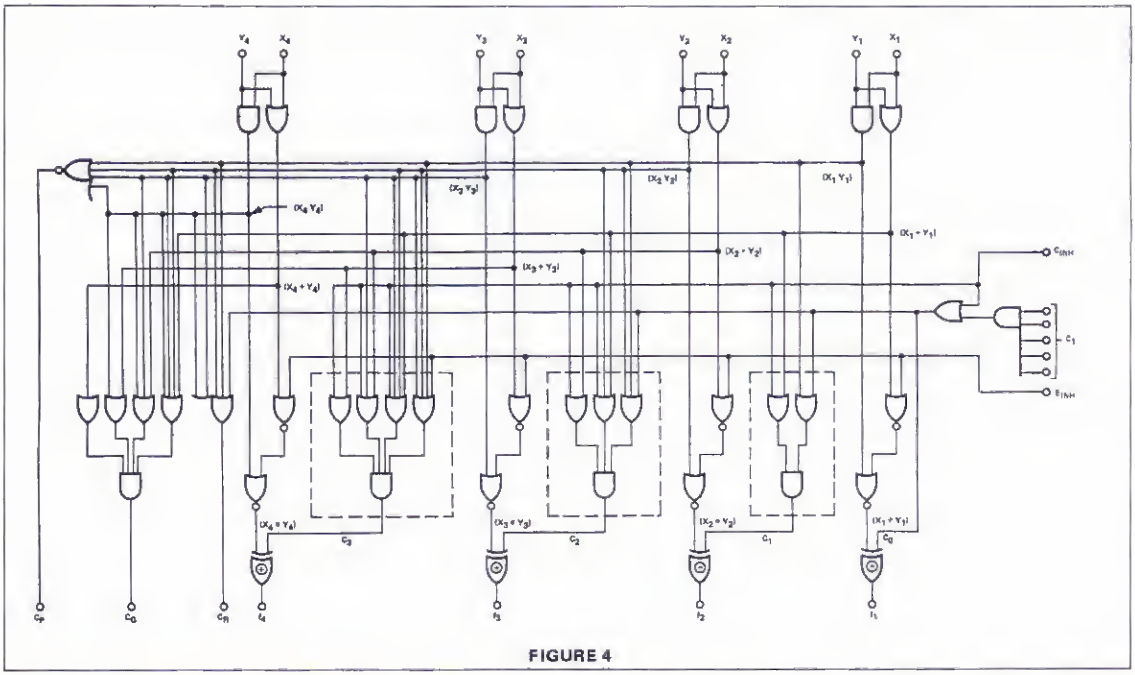


FIGURE 4

CARRY TERMS C_R, C_G, AND C_P

The additional carry outputs are necessary for high speed adders employing word lengths greater than 4 bits. The logic equations for these outputs are given below:

$$C_R = C_O + X_1Y_1 + X_2Y_2 + X_3Y_3 + X_4Y_4$$

$$C_G = (X_4 + Y_4)\,[X_4Y_4 + (X_3 + Y_3)]\,[X_4Y_4 + X_3Y_3 + (X_2 + Y_2)]\,[X_4Y_4 + X_3Y_3 + X_2Y_2 + (X_1 + Y_1)]$$

$$C_P = X_1Y_1 + X_2Y_2 + X_3Y_3 + X_4Y_4$$

C_R — is used in the ripple carry mode to help determine whether a carry can ripple through the 8260.

C_G — indicates whether a carry will be generated internally, or if the inputs are such that an incoming carry will propagate to the output.

C_P — is used as an input to the 8261 FAST CARRY EXTENDER package to provide anticipated carry information for adder systems greater than 12 bits in length.

These carry terms are used, in specific combinations, as inputs to the more significant adder packages. The C_{IN} inputs are effectively ANDed together to form C_O, the lower order carry.

$$C_O = (C_{IN1} \cdot C_{IN2} \cdot C_{IN3} \cdot C_{IN4} \cdot C_{IN5}) + C_{INH}$$

None of the above terms (C_R, C_G and C_P) are ever used alone. For example, when opera ting in the ripple mode, C_G and C_R are fed into the next most significant 8260. Therefore, C_O for that particular device would be $C_G\,C_R$.

Besides the normal adder applications, the 8260 acts as multi-purpose logic element. The control input CARRY INHIBIT (C_{INH}) provides the capability of inhibiting the bit-to-bit carries. In this case the device will operate as four independent Exclusive NOR gates. The devices also has an EXCLUSIVE NOR INHIBIT (E_{INH}) to permit a single logical AND combination of the input bits pairs ($X_i \cdot Y_i$).

We assume that we apply true values to the inputs. In this case, the pins f_i have the values shown in top half of Table 1.

On the other hand, we may assume that we apply not true values to the inputs. Depending on the values of C_{INH} and E_{INH} the resultant functions of the pins f_i are listed in the lower half of Table 2.

TABLE I

INPUTS	Least Significant C_{in} Inputs to be:	CONTROL		f_i	FUNCTION
		C_{inh}	E_{inh}		
X_i, Y_i (TRUE INPUTS)	0	0	0	Σ_i	Add
	0	0	1	—	not used
	0	1	0	$\overline{X}_i \overline{Y}_i + X_i Y_i$	Equivalence *
	0	1	1	$X_i Y_i$	AND
$\overline{X}_i$ $\overline{Y}_i$ (NOT-TRUE) INPUTS	1	0	0	$\overline{\Sigma}_i$	Add
	1	0	1	—	not used
	1	1	0	$X_i Y_i + \overline{X}_i \overline{Y}_i$	Equivalence * Coincidence
	1	1	1	$\overline{X}_i \overline{Y}_i$	AND

* (EXCLUSIVE NOR)

FAST CARRY EXTENDER

If we do not extend the internal look-ahead technique beyond one adder, the carry out term $C_G \cdot C_R$ will ripple between 8260 units. The 8260 adder is inherrently a high speed device and look-ahead carry techniques between adders are not necessary for addtions up to 12 bits.

To avoid the RIPPLE CARRY addition time, for larger adder systems, the 8261 Fast Carry Extender shown in Figure 5 is used. We replace C_R by the logically equivalent CARRY EXTENDER term C_E: Every term C_{Ei} is generated for the i-th package simultaneously and replaces the slower RIPPLE CARRY signal. The FAST CARRY EXTENDER, 8261, will form the C_{Ei} - terms.

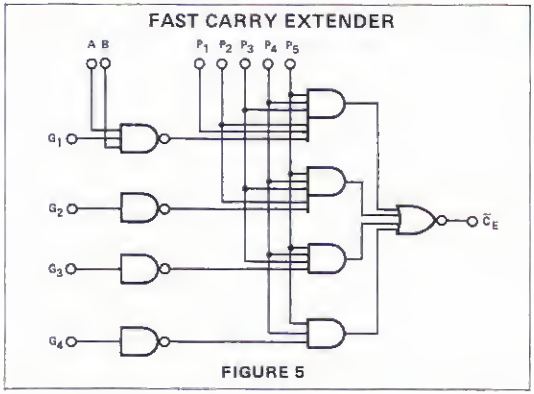


FIGURE 5

ADDER SUBTRACTOR USING TWO'S COMPLEMENT

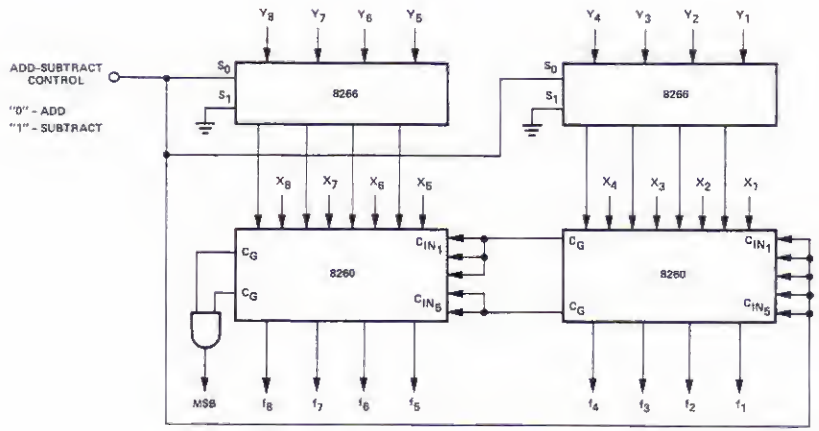


FIGURE 6

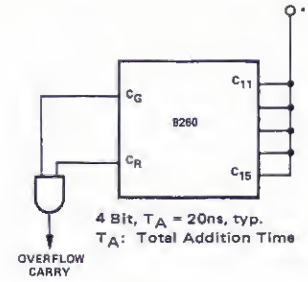
Figure 6 shows an 8-bit add/subtract system using the Signetics 8266 to complement the Y inputs of the 8260 when a subtract command is received.

The above circuitry assumes that in the SUBTRACT mode (X - Y), $Y_{(Y1, Y2, \ldots . Y8)}$ is always the smaller of the two binary numbers. If Y is not the smaller of the two numbers, correction may be made by detecting the presence of a CARRY term at the most significant bit (MSB) and taking the two's complement of the result.

ADDER SYSTEMS

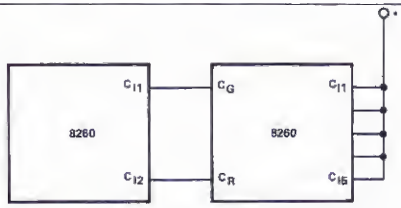
Figures 7-17 show the implementation of various adder systems. If the carry-out term is needed out of the most significant adder stage it can be obtained by combining the C_g and C_r terms with an AND gate as shown in Figure 7. The Fast Carry Extender, 8261, becomes useful for adder systems with more than 12 bits as previously explained. Figures 10 through 17 show various uses of the Fast Carry Extender.

The Fast Adder Systems provide complete carry look-ahead addition for any words length. For longer efficient adders, a combination of anticipated carry techniques (Fast Adder System) and ripple carry techniques are used. These Optimum Adder Systems represent the most economical solutions.



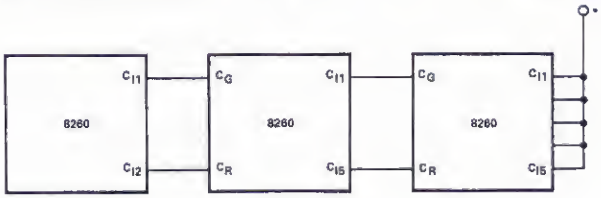
4 Bit, T_A = 20ns, typ.
T_A: Total Addition Time

FIGURE 7



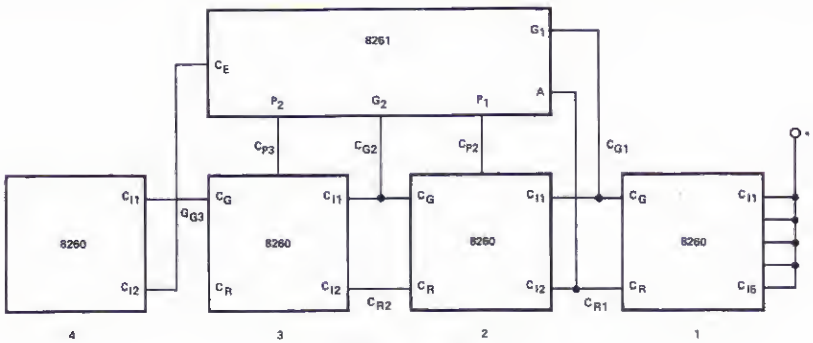
8 Bit, T_A = 30ns, typ.
(Ripple Adder)

FIGURE 8



12 Bit, T_A = 42ns, typ.
(Ripple Adder)

FIGURE 9

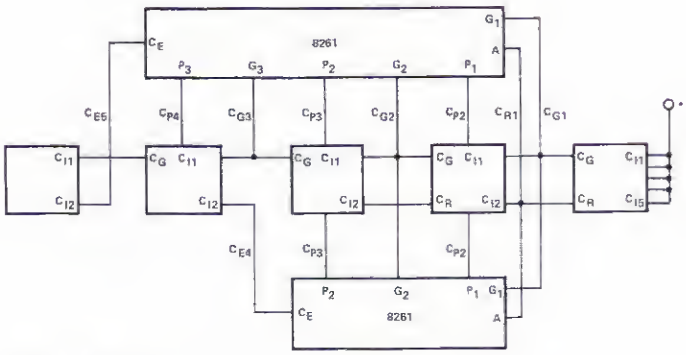


16 Bit, T_A = 42ns, typ.
Fast Adder System

*Tied to V_{CC} if not-true inputs are used, otherwise to ground
Unused 8261 pins should be tied to V_{CC}.

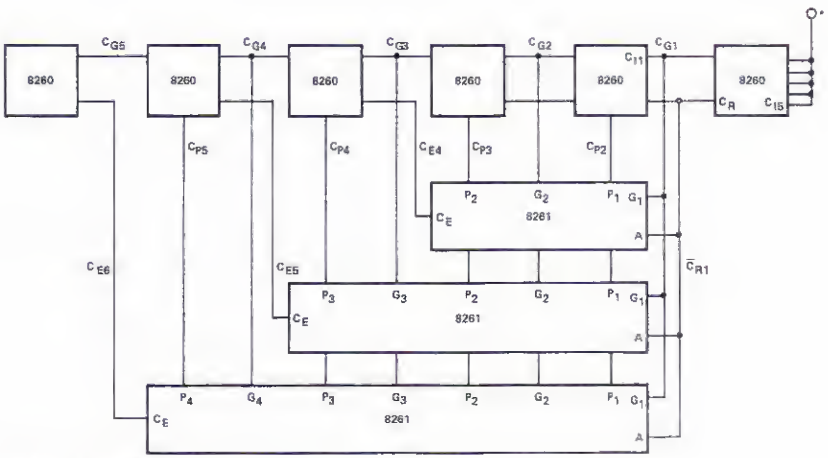
FIGURE 10

ADDER SYSTEMS (CONT'D)



20 Bit, T_A = 42ns, typ.
Fast Adder System

FIGURE 11

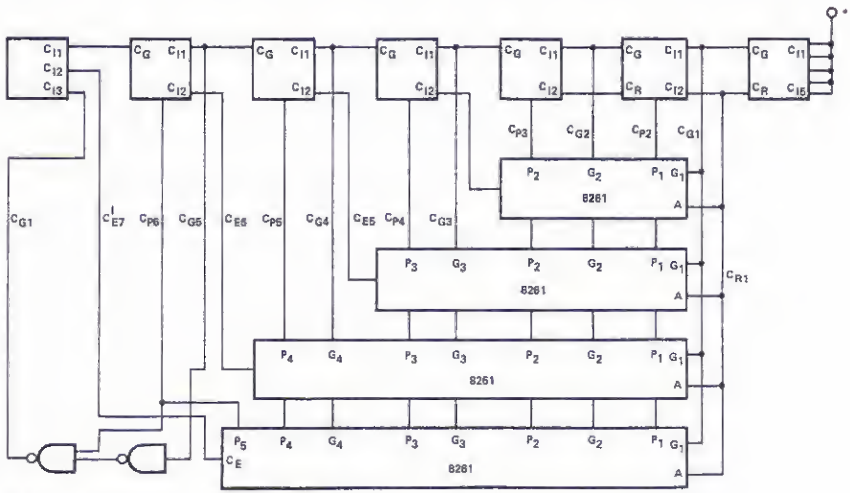


24 Bit, T_A = 42ns, typ.
Fast Adder System

*Tied to V_{CC} if not-true inputs are used, otherwise to ground.

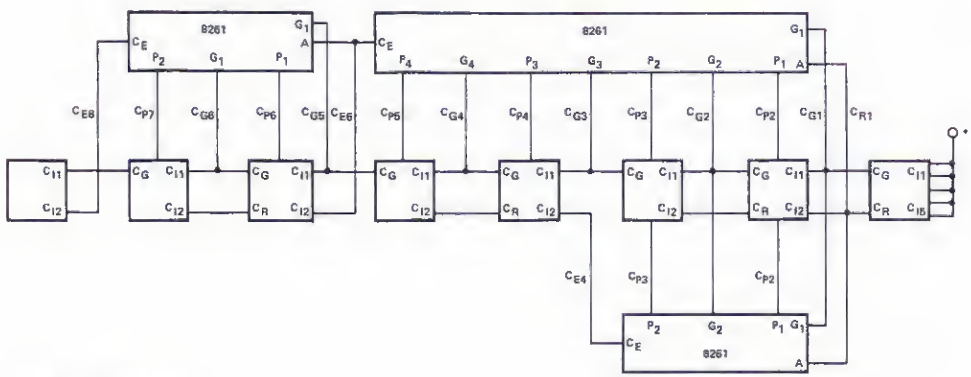
FIGURE 12

ADDER SYSTEMS (CONT'D)



28 Bit, T_A = 42ns, typ.
Fast Adder System

FIGURE 13

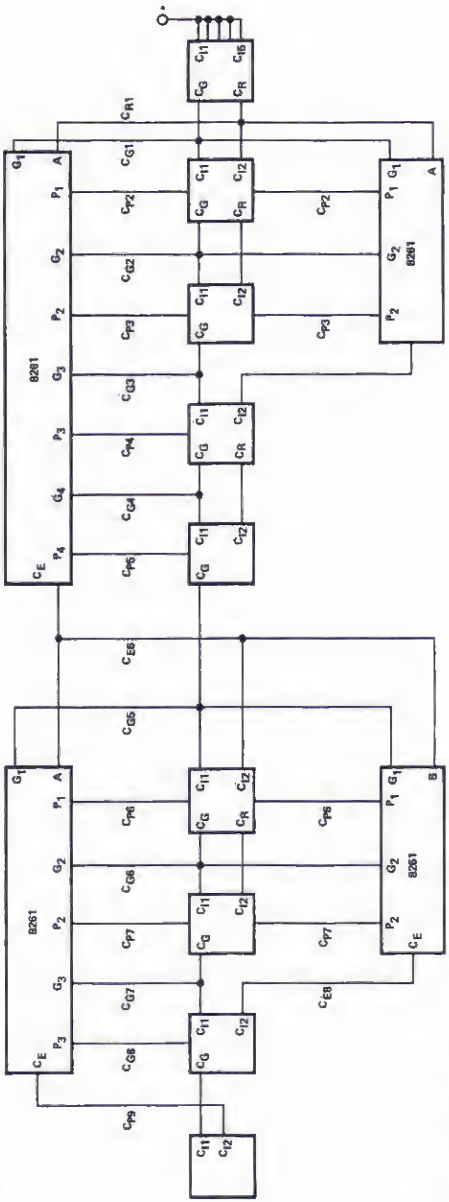


32 Bit, T_A = 54ns, typ.
Optimum Adder

*Tied to V_{CC} if not-true inputs are used, otherwise to ground.

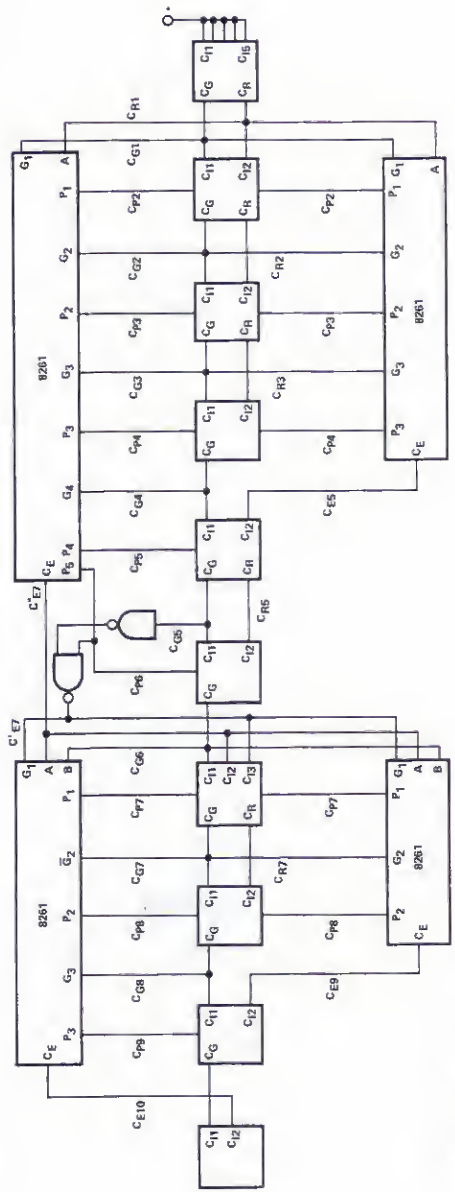
FIGURE 14

ADDER SYSTEMS (Cont'd)



36 Bit, T_A = 54ns, typ.

FIGURE 15

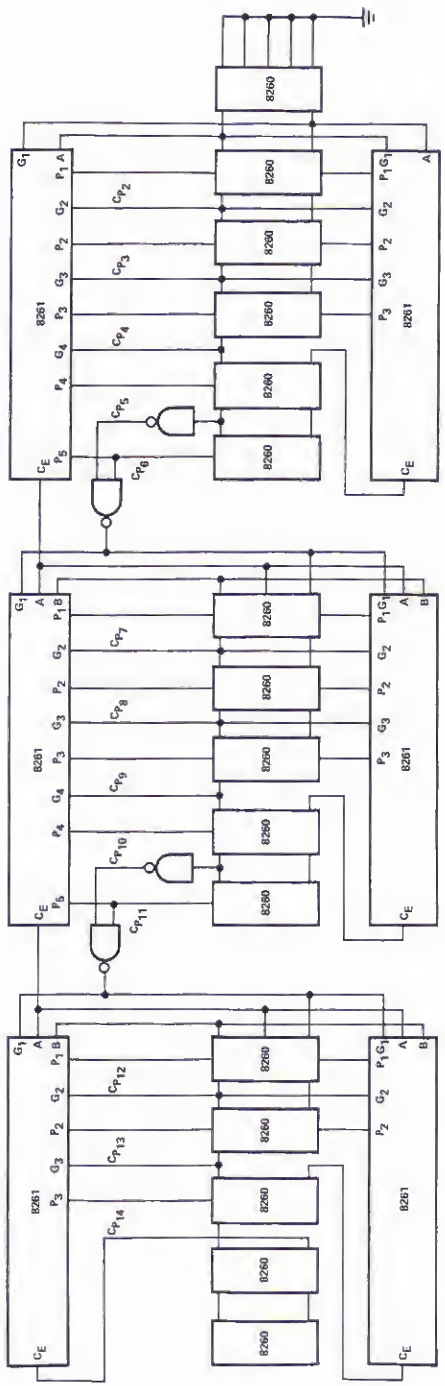


40 Bit, T_A = 54ns, typ
Optimum Adder with 2-Bridge Structure

*Tied to V_{CC} if not-true inputs are used, otherwise to ground.

FIGURE 16

ADDER SYSTEMS (Cont'd)



64-Bit, T_A = 78ns, typical (Optimum Adder)

FIGURE 17

ALSO AVAILABLE IN SCHOTTKY (82S62)

9-BIT PARITY GENERATOR AND CHECKER

INTRODUCTION

The 8262 Parity Generator/Parity Checker is a versatile MSI device generally used for the verification of transmitted data. Two outputs are provided for versatility in parity generation and checking.

As shown, the "odd" output of the 8262 responds to an odd number of "1" 's with a logical "1", whereas the "even" output responds to the same input conditions with a logical "0". When the inputs see an even number of "1" 's the "odd" output responds with a logical "0" while the even output is in the logical "1" state.

The inhibit input may be used to disable the 8262. A logic "1" forces both outputs to a logic "0". This proves especially useful when driving J-K binaries or shift register inputs.

LOGIC DIAGRAM

8262

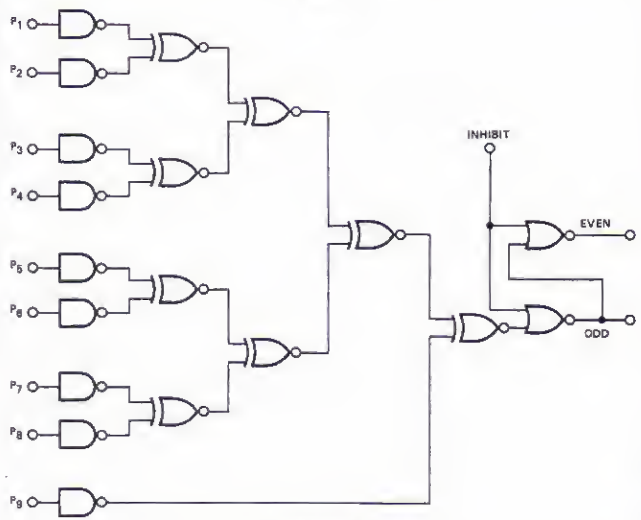


FIGURE 1

LOGIC EQUATIONS

$$\text{EVEN} = \overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$$

$$\text{ODD} = P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

NOTE

Unused inputs of the 8262 must be held at "0" since grounding does not affect the number of "1" 's seen by the remaining inputs.

APPLICATIONS

To verify if a data word has been transmitted correctly, the number of "1" 's at the sender may be checked as well as the number of "1" 's at the receiver. If they are the same, it may be assumed that no single bit reversal or error has occurred in the transmission.*

A PARITY GENERATOR checks the data word and its output supplies a parity bit which is transmitted together with the data word. The PARITY CHECKER then responds to the total word transmitted and its output signals if the transmission was correct or in error.

* More elaborate schemes for double error detection and correction are possible but are not discussed here.

EVEN PARITY is defined such that the total word transmitted, which is the data word plus the parity bit, always has an even number of ones. Conversely, ODD PARITY means that the total word transmitted always consists of an odd number of "1" 's.

PARITY GENERATOR

When using the 8262 as a PARITY GENERATOR several options exist. It may be advantageous to use the "P_9" input as a control line, particularly if propagation delays in the system are critical. The logic diagram (Fig. 1) shows clearly that an additional gate delay is encountered when going to the "even" instead of the "odd" output.

Examples of Parity Generator connections are shown in Fig. 2 with a logic "1" or a logic "0" respectively at the "P_9" input used as a control line. With the "P_9" input at V_{CC} (logic "1") the outputs generate parity signals as shown. If the "P_9" input is grounded (logic "0") the device generates parity. Thus the shortest propagation delay can be obtained for an even as well as an odd parity generator by an appropriate input condition on the control line.

Furthermore, the complement of the parity bit generated is always available. This feature is especially useful when driving J-K binaries or for general line driver applications.

PARITY GENERATORS

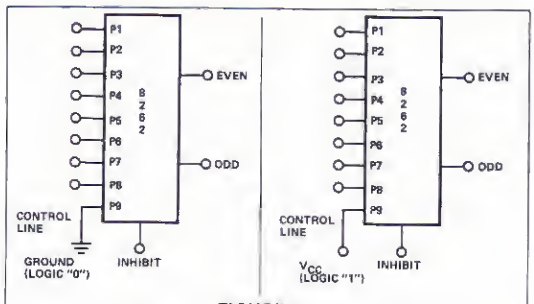


FIGURE 2

EVEN PARITY GENERATOR
OUTPUT = "1" IF ODD NO. OF "1" 's AT INPUTS $P_1 - P_8$

ODD PARITY GENERATOR
OUTPUT = "1" IF EVEN NO. OF "1" 's AT INPUTS $P_1 - P_8$

ODD PARITY GENERATOR
OUTPUT = "1" IF EVEN NO. OF "1" 's AT INPUTS $P_1 - P_8$

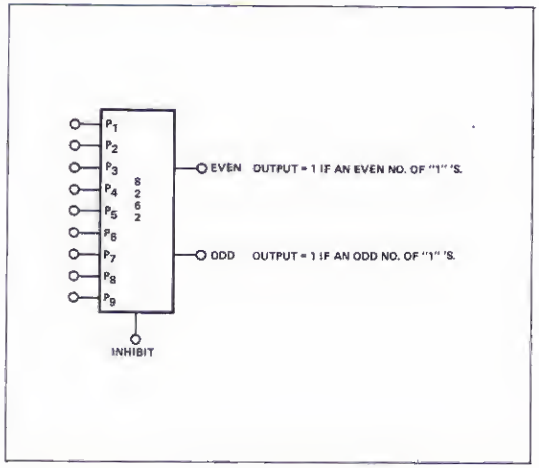
EVEN PARITY GENERATOR
OUTPUT = "1" IF EVEN NO. OF "1" 's AT INPUTS $P_1 - P_8$

PARITY CHECKER

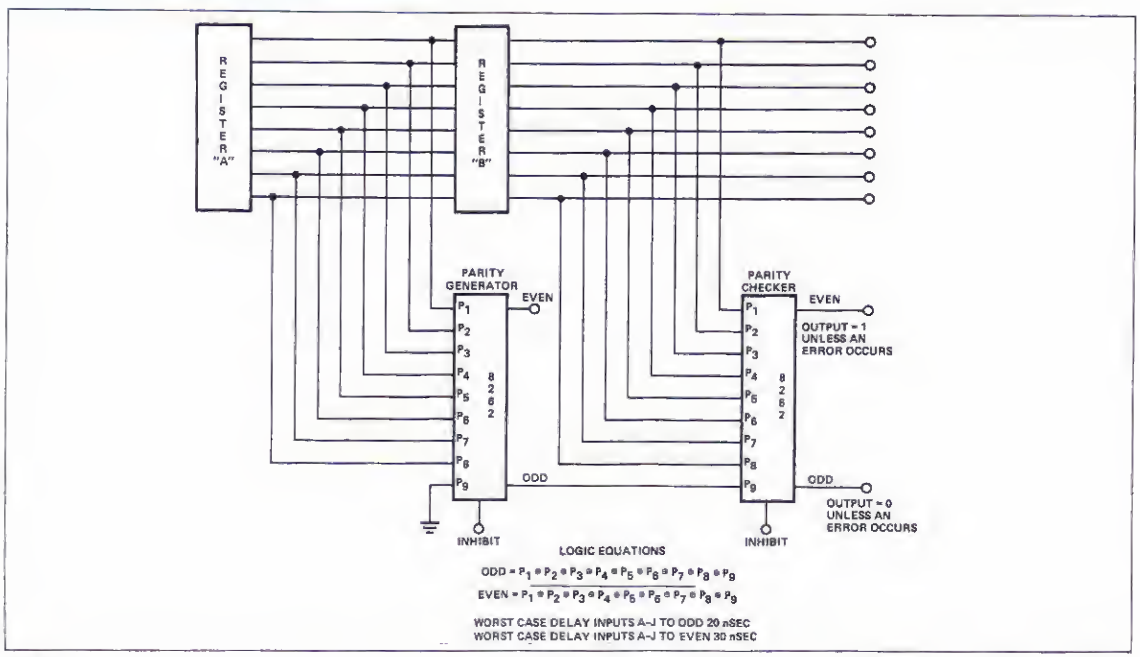
The **PARITY CHECKER** receives a 9-bit word consisting of the 8-bit data word and the parity bit. If data transmission was correct, the output indicates this. We have the option of letting it be shown by a "1" or a "0" since complementary outputs are available.

In the following drawings several possibilities of a parity generator checker system are shown.

PARITY CHECKER



EVEN PARITY GENERATOR/CHECKER

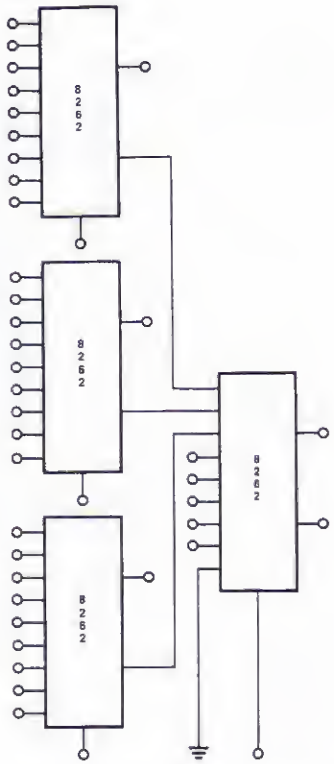


WORD EXPANSION

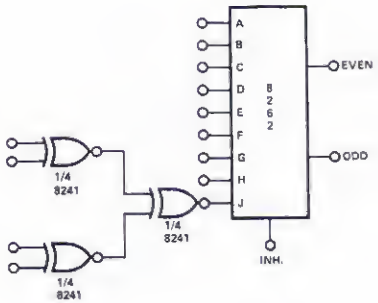
The 8262 can be easily expanded to any desired word length. An example using only 8262 is shown below.

Other expansion schemes are possible using only gates or the 8241 Quad Exclusive-OR package. This method is particularly attractive if the word length has to be expanded by only a few bits. Two examples are shown.

27-BIT EXPANSION



12-BIT EXPANSION



3-INPUT, 4 BIT MULTIPLEXES

INTRODUCTION

The 8263/64 Multiplexers have been designed to select one out of three 4-bit inputs. In addition, provision has been included for selecting the true or complement of the inputs. A 2-bit code determines which input is to be active.

The 8263 has an active output structure to minimize propogation delay. The 8264 features open collector outputs for device expansion and three Output Enable pins for device selection.

Figures 1 and 2 show the logic diagrams for the 8263 and 8264. Table 1 shows the Data Outputs associated with each selection code.

Figures 3 and 4 show how the 8263 and 8264 may be expanded to accomodate six 4-bit inputs.

8263 (ACTIVE PULL-UP)

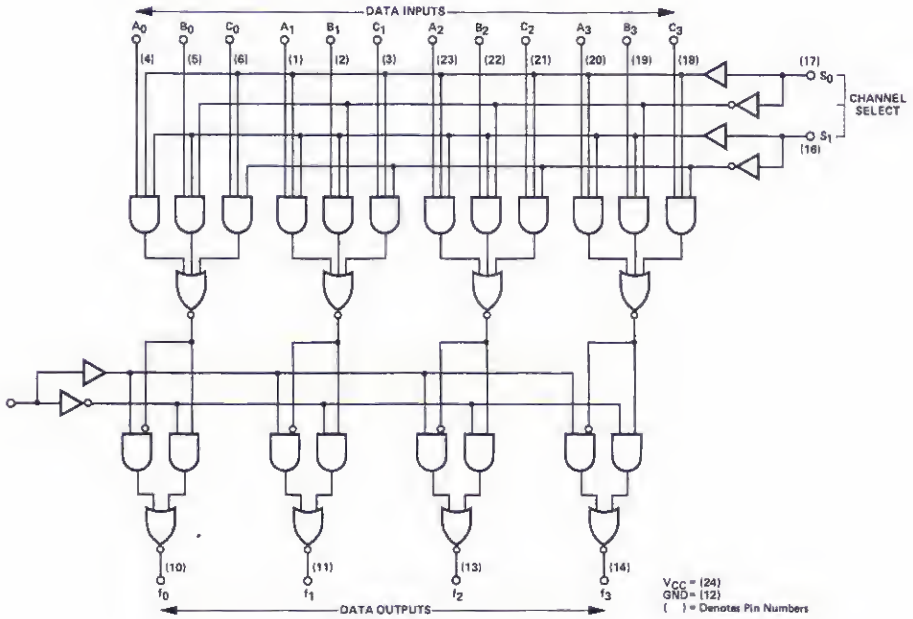


FIGURE 1

8264 (OPEN COLLECTOR)

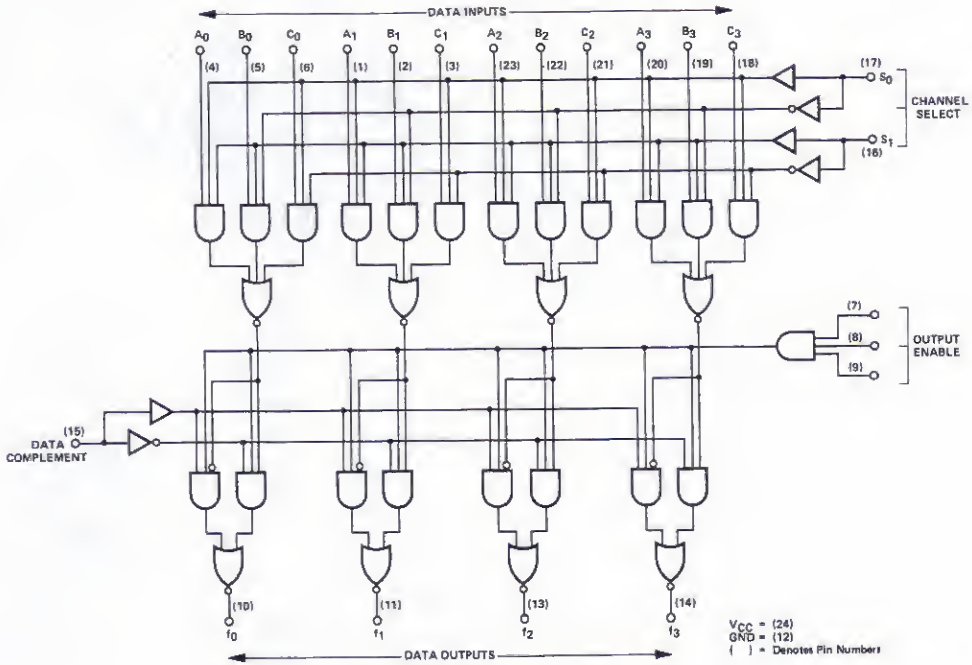


FIGURE 2

TRUTH TABLE

Data Input A_n B_n C_n	Channel Select S_0 S_1	Data Complement	Output Enable (8264)	Data Outputs
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	$\overline{A}_n$
x B_n x	0 1	1	1	$\overline{B}_n$
x x C_n	1 0	1	1	$\overline{C}_n$
x x x	0 0	1	1	1
x x x	x x	x	0	1

X = Either State

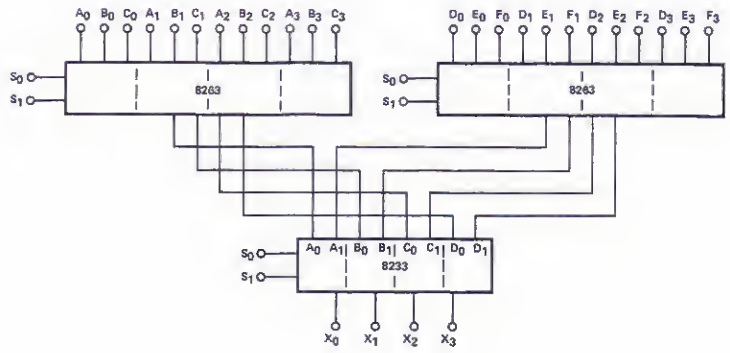


FIGURE 3

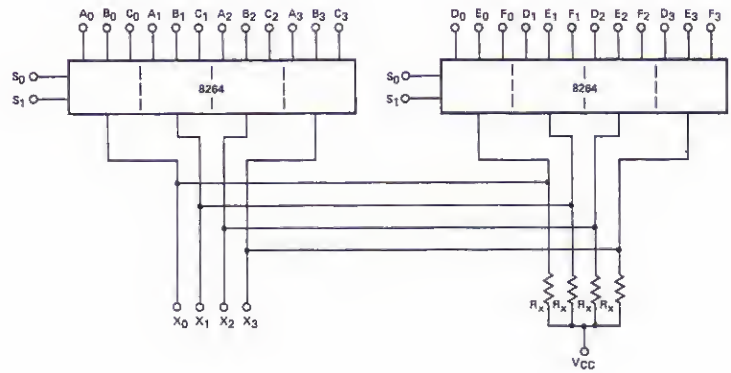


FIGURE 4

INTRODUCTION

The 8268 is a binary Full Adder with gated complementary inputs sum and sum outputs and inverted Carry Out ($\overline{\text{Carry Out}}$). The MSI circuit is designed with TTL techniques, completely compatible with other DTL and TTL devices.

The Full Adder is designed especially for serial and Ripple Carry parallel ADD/SUB arithmetic units. The array has single-ended inputs and outputs, so that only the true or complement information is necessary. The logic diagram for the 8268 is shown in Figure 1.

8268 GATED FULL ADDER

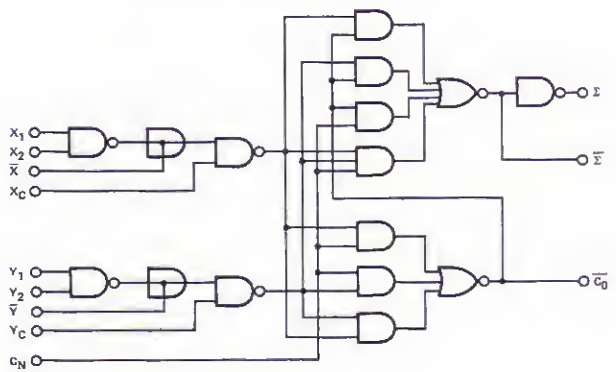


FIGURE 1

TRUTH TABLE (SEE NOTES 1, 2 and 3)

C_N	Y	X	$\overline{C_0}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES:

1. $\overline{X} = X \cdot X_c$; $\overline{Y} = Y \cdot Y_c$

   where $\overline{X} = \overline{X_1 \cdot X_2}$; $\overline{Y} = \overline{Y_1 \cdot Y_2}$

2. When $\overline{X}$ or $\overline{Y}$ are used as inputs, X_1 and X_2 or Y_1 and Y_2 respectively must be tied to GND.

3. When X_1 and X_2 or Y_1 and Y_2 are used as inputs, $\overline{X}$ or $\overline{Y}$ respectively must be left open or used to perform the dot-AND function.

APPLICATIONS

N-BIT PARALLEL ADDER

The factor which determines the maximum operating frequency for an N-bit parallel adder with ripple carry is the total propagation of the ripple carry term, or N x $\text{CARRY}_{\text{DELAY}}$. To avoid the delay of an additional inversion required to provide $\text{CARRY}_{\text{OUT}}$ (C_0), the 8268 provides $\overline{\text{CARRY}_{\text{OUT}}}$ ($\overline{C_0}$). When the $\overline{C_0}$ term is used with the appropriate gated inputs ($\overline{X}$ and $\overline{Y}$) at the next significant bit, the desired result is available at the $\overline{\text{SUM}}$ ($\overline{\Sigma}$) output. This arrangement is used in every even numbered bit in an N-bit parallel adder as shown in Bit 2 and Bit 4 of Figure 2. For each even numbered bit, input control is accomplished through gated inputs X_C and Y_C. With INPUT CONTROL $(X_C \cdot Y_C) = 0$, the adder bit is disabled and all output terms are "0". This use of input control is twofold in purpose.

First, with the adder disabled, data in the input registers may be shifted without activating the adder subsystem. Second, with all output terms at "0" the outputs can be used to clear the output storage register by parallel loading the output register with all "0"s.

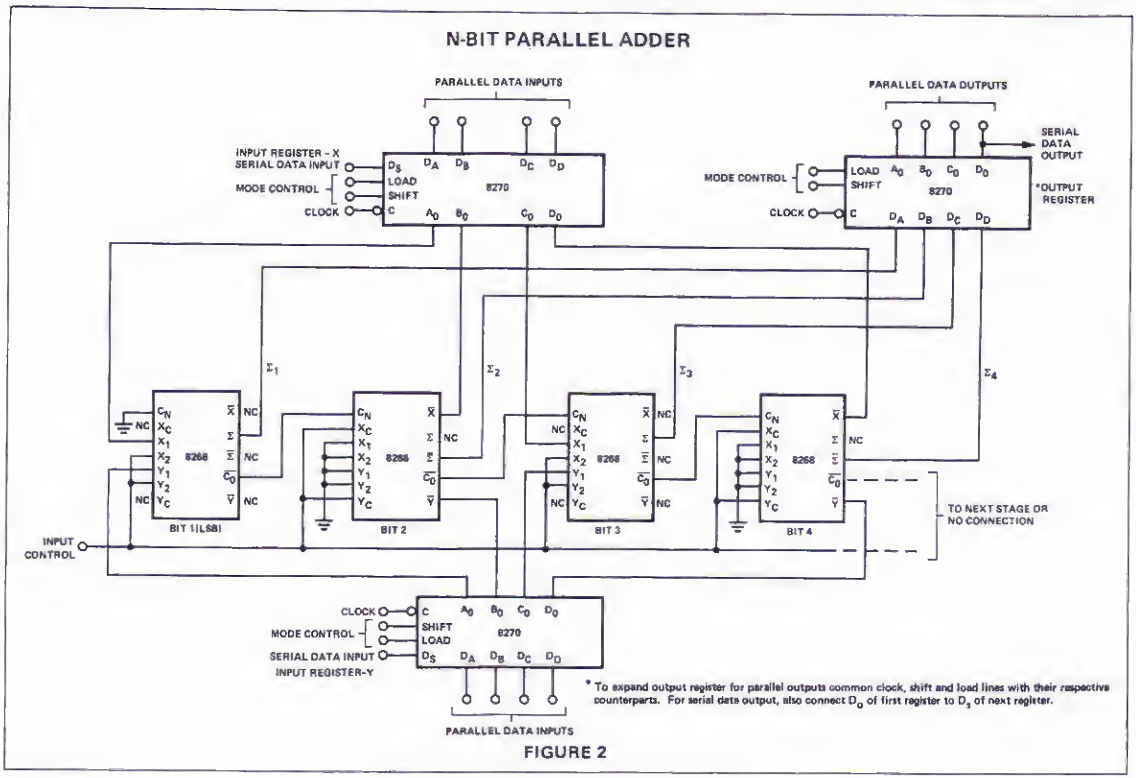


FIGURE 2

NOTE

1. To expand storage register for serial/parallel operation, connect D_0 to D_S of next stage and common the mode control lines and the clock line of the first stage to their respective second stage equivalents.

Notice that the $\overline{C_0}$ of the second, fourth, etc. (all even numbered bits) constitutes a TRUE carry output. Therefore, to arrive at the TRUE sum at the output of all odd numbered bits $\overline{C_0}$ is used in conjunction with the TRUE data inputs X_1 and Y_1. The desired output result for all odd numbered bits is available at the Σ terminal.

INPUT CONTROL is accomplished in the odd number bits of an N-bit adder by inhibiting or enabling the gated inputs $X_2 \cdot Y_2$. From the logic diagram of Figure 1, it is apparent that a "0" at X_2 and Y_2 will inhibit the transfer of the bits to be added (X_1 and Y_1). When INPUT CONTROL = "1", the information at X_1 and Y_1 will be enabled and addition will occur. Since the data inputs used are the TRUE inputs, the desired result will be available at the SUM output (Σ_i). This operating mode is shown in Bit 1 and Bit 3 of Figure 2.

Note that the CARRY$_{IN}$ (C_n) term of the least significant bit of the binary adder in Figure 2 is tied to GND, since C_n is a TRUE term (activiates on "1") and there is no carry term into the least significant bit.

N-BIT BINARY SUBTRACTOR

To construct an N-bit binary subtractor (Figure 3), the logic input of the subtrahend (register Y) is inverted on a by bit basis from the input arrangement for the binary adder.

In addition, the input used for the Y register input control is effectively inverted (compared to the adder). Thus:

for all odd numbered bits (1, 3, etc.)
INPUT CONTROL = $X_2 \cdot Y_C$

for all even numbered bits (2, 4, etc.)
INPUT CONTROL = $X_C \cdot Y_2$

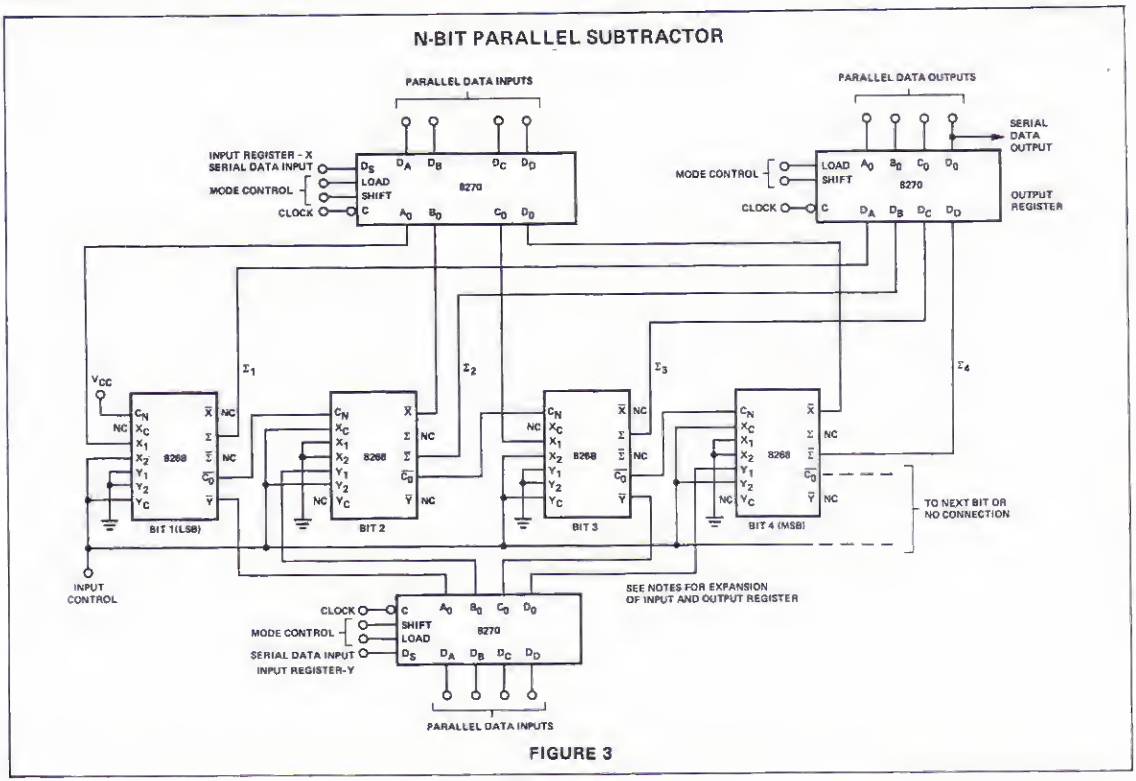


FIGURE 3

The input control connection pattern results from the inversion of the Y-register logic inputs.

Note that to provide the SUBTRACT function, the C_n input of the least significant bit must be connected to a logical 1 level.

SERIAL BINARY ADD-SUBTRACT

Figure 4 illustrates a 4-bit serial ADD/SUB arithmetic unit. The unit will add X + Y or subtract X - Y upon command. The interconnect scheme is implemented as follows:

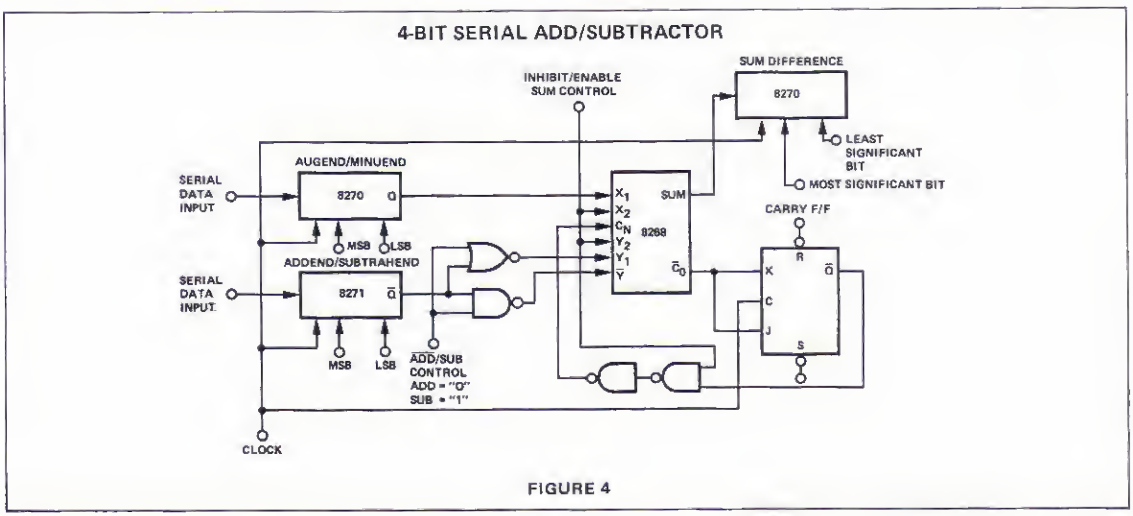


FIGURE 4

Assume the two binary numbers to be added/subtracted are present in the Augend/Minuend and Addend/Subtrahend Registers. For *addition*, set control line to logic "0". Also, initially set Carry F/F ($\overline{Q}$ = 0). This allows the data in the Addend/Subtrahend register to be entered into the sum/difference register and the Carry Flip-Flop has been conditioned for the addition of the next two binary bits. The sum is formed Least Significant Bit first. This process continues until 4 clock pulses have occurred. At the end of the 4th clock pulse, the result is in the sum/difference register (i.e. LSB appears at D_0; MSB appears at A_0). For *subtraction*, the ADD/SUB control is set to a logic "1". Also, the Carry Flip-Flop should be reset (i.e., $\overline{Q}$ = 1). Now the subsystem is ready to perform subtraction (i.e. one's complement addition). Once again, after 4 clock pulses have occurred, the result is in the sum/difference register.

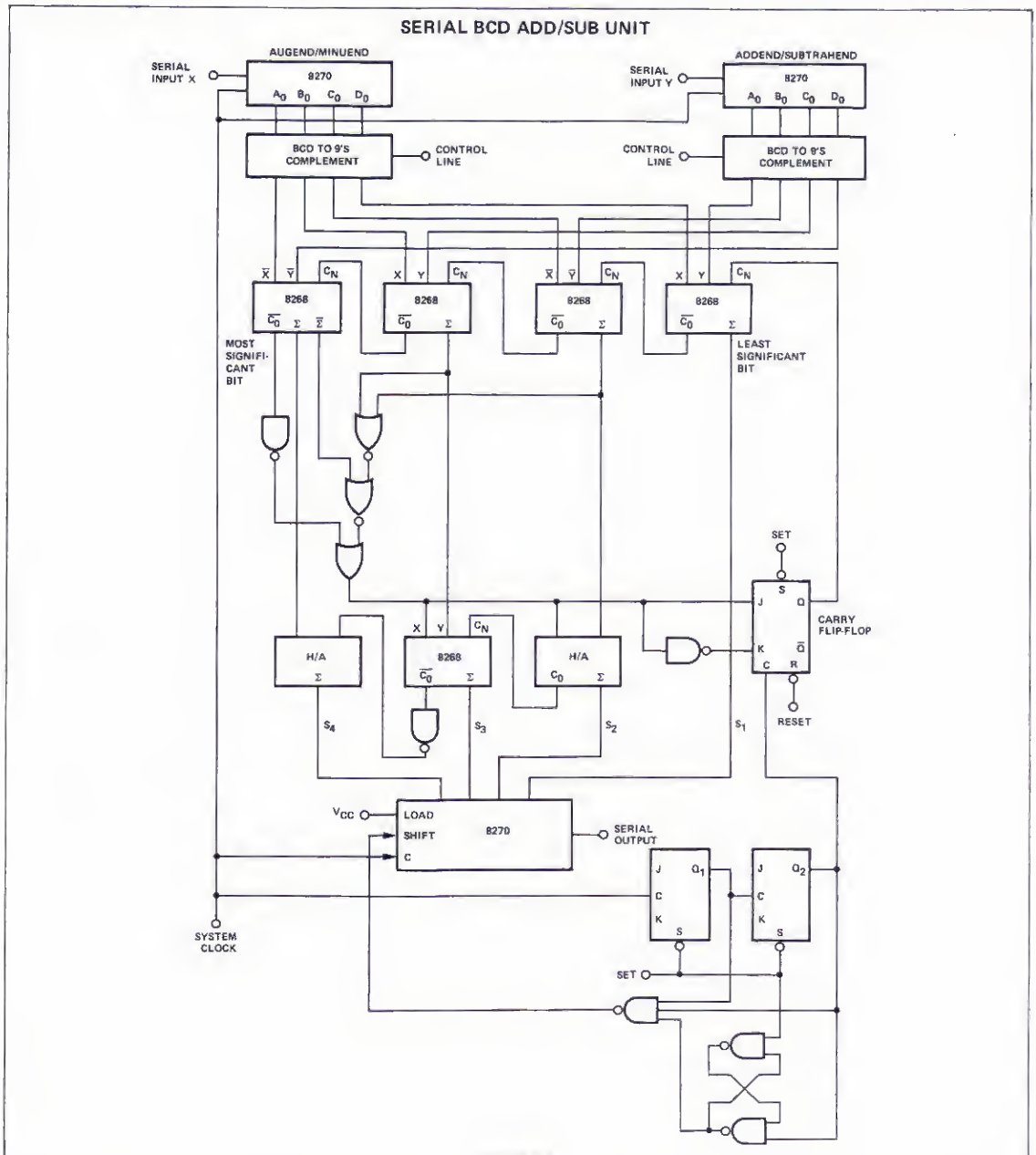


FIGURE 5

As an option, the inhibit/enable sum control may be used to force the sum output to logic "0" in between shift pulses or as a "jam" function. The X_2 and Y_2 inputs force the sum to "0" when $X_2 = Y_2 =$ "0".

SERIAL BCD ADD/SUBTRACT *

Figure 5 shows a BCD ADD/SUBTRACT serial subsystem. This subsystem uses nine's complement addition to perform subtraction. One should be aware that the nine's complement of the smaller (absolute value) number must be formed in order to get the correct result.

OPERATION

The Augend and Addend are shifted into the 8270 (4 bit shift registers). The divide by four counter is initially set to $Q_1 = 1$ and $Q_2 = 1$. The subsystem is now ready to perform Addition or Subtraction. If it is desired to perform addition, then the control lines on the nine's complement converters are at logic "1" and Carry Flip-Flop is initially reset (i.e., Q = "0").

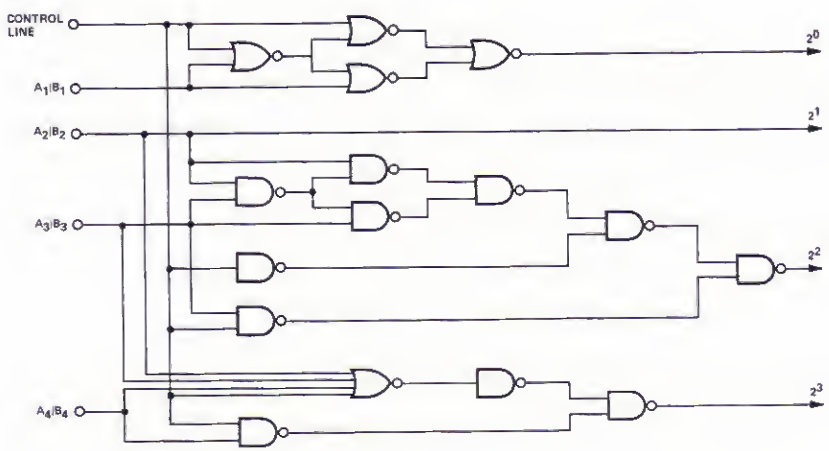
To perform subtraction, the control line associated with the smaller of the two numbers (absolute value) is at logic "0", the other control line at logic "1" and the Carry Flip-Flop is initially set (i.e., Q = "1").

The Carry Flip-Flop is clocked at one-fourth the system rate due to the fact that a BCD code is 4 binary bits long.

The sum outputs of the Adder are allowed to enter the sum/difference register in parallel on every 4th clock. Thus, no information is entered into the sum/difference register while shifting takes place.

*A 4-Bit BCD arithmetic unit, 82S82 and a 4-bit BCD adder 82S83 are also available from Signetics.

CONDITIONAL BCD TO 9's COMPLEMENT †



† Can be programmed into the 8223 256 Bit P-ROM.

FIGURE 6

INTRODUCTION TO ASYNCHRONOUS COUNTERS

Signetics offers a variety of asynchronous MSI counters/storage elements. These counters have two things in common: 1) the output of one flip-flop is connected to the Clock input of the following flip-flop in "ripple" fashion, and 2) each flip-flop is clocked on the negative-going edge of the output transition of the preceding flip-flop or the clock inputs. Thus, the N_{th} flip-flop is activated on the falling edge of the output transition of the N-1 flip-flop as illustrated in Figure 1.

BINARY RIPPLE COUNTER

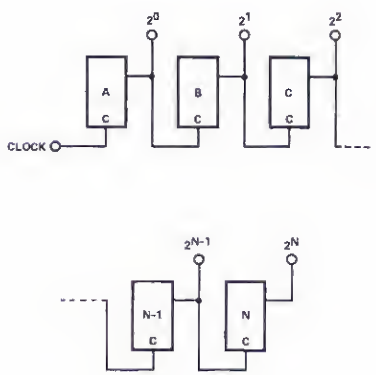


FIGURE 1

Asynchronous counters have two distinct advantages over other counter configurations. Power consumption can be optimized, utilizing the fact that each flip-flop does not have to be operated at the incoming frequency. In a binary ripple counter, each flip-flop operates at one-half the frequency of the preceding flip-flop. Complexity and power consumption are reduced compared to synchronous counters since little or no gating is required between flip-flops.

Asynchronous counters traverse intermediate output codes during single clock intervals. This characteristic is demonstrated for the 8281, 4-Bit Binary Ripple Counter in Figure 2. The traversed state(s) can last from 10 to 80ns depending on the next code in the output sequence.

OUTPUT TRANSITIONS OF A BINARY RIPPLY COUNTER (8281)

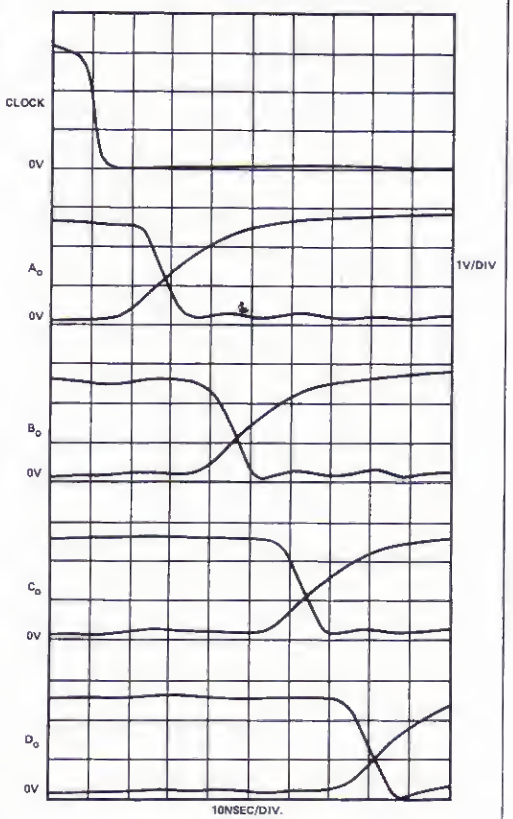


FIGURE 2

In most applications of frequency division, intermediate codes are of no concern. Each output is considered separately, in terms of the number of activating (negative-going) pulses it produces in relation to the number of clock pulses observed at the clock input of the counter.

When decoding the outputs, in counting applications, care may have to be taken to ensure that the decoder is activated after the interval when intermediate codes may exist. An example of this decoding technique is shown in Figure 3.

STROBING THE OUTPUTS OF THE 8281

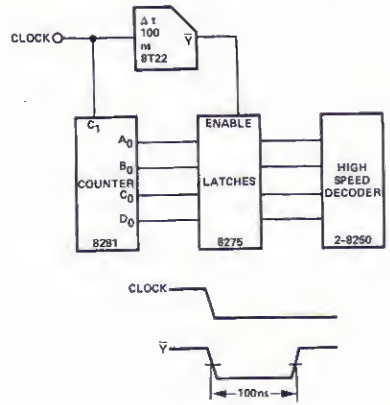


FIGURE 3

8200 SERIES RIPPLE COUNTERS/STORAGE ELEMENTS

To provide the user with a maximum choice of speed/power trade-off and counter moduli; the 8200 series asynchronous MSI counters shown in Table 1 are all pin-for-pin compatible. Thus, a user who wants to upgrade his system at a later time can do so without penalty.

8280/81/88 COUNTERS/STORAGE ELEMENTS

The logic diagram of the 8281 4-Bit Binary (16 State) Ripple Counter is shown in Figure 4. Figure 5 is the logic diagram of a modified ripple configuration, the 8280 BCD Decade Counter, whereas Figure 6 shows the 8288 divide-by-twelve counter. These counter/storage elements consist of four presettable clocked J-K flip-flop elements of the design shown in Figure 7.

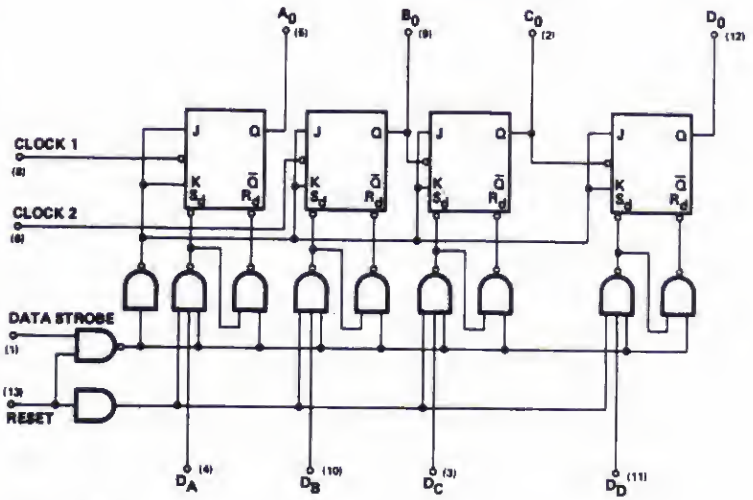
8200 SERIES PRESETTABLE ASYNCHRONOUS MSI COUNTERS

DEVICE TYPE	NUMBER OF OUTPUT STATES	GUARANTEED CLOCK INPUT FREQUENCY	TYPICAL POWER CONSUMPTION PER COUNTER	REQUIRED STROBE HOLD TIME	REQUIRED STROBE RELEASE TIME	REQUIRED RESET HOLD TIME	REQUIRED RESET RELEASE TIME
8280	10	20 MHz	184 mW	35 ns	40 ns	35 ns	75 ns
8281	16	20 MHz	184 mW	35 ns	40 ns	35 ns	75 ns
8288	12	25 MHz	184 mW	35 ns	40 ns	35 ns	75 ns
8290	10	40 MHz	190 mW	25 ns	20 ns	30 ns	20 ns
8291	16	40 MHz	190 mW	25 ns	20 ns	30 ns	20 ns
8292	10	5 MHz	52 mW	75 ns	20 ns	60 ns	100 ns
8293	16	5 MHz	52 mW	75 ns	100 ns	60 ns	100 ns
82S90	10	85 MHz	308 mW	5 ns typ	10 ns typ	7 ns typ	10 ns typ
82S91	16	85 MHz	308 mW	5 ns typ	10 ns typ	7 ns typ	10 ns typ

TABLE 1

The first flip-flop is separated from the other three to provide applications flexibility. For example, the 8280 may be arranged as a BCD decade counter or as a Bi-Quinary (10-state) counter. The specifics of application flexibility will be discussed later.

8281



TRUTH TABLE*

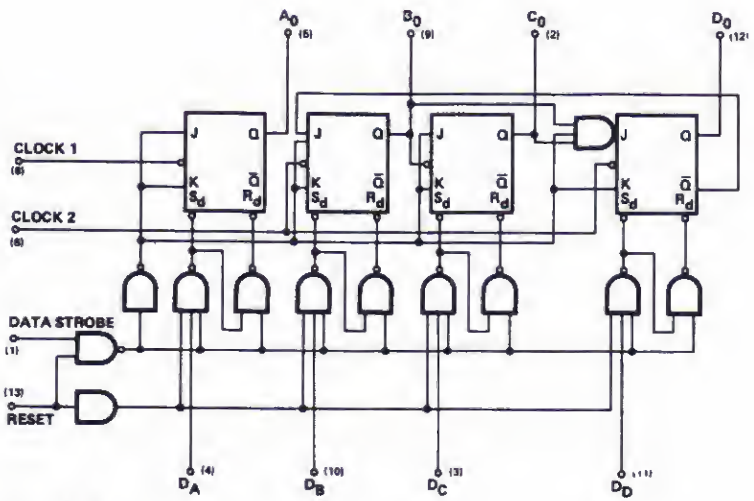
Binary Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

*Connected for divide-by-16 operation (output A connected to C_{P2})

FIGURE 4

8280



TRUTH TABLE*

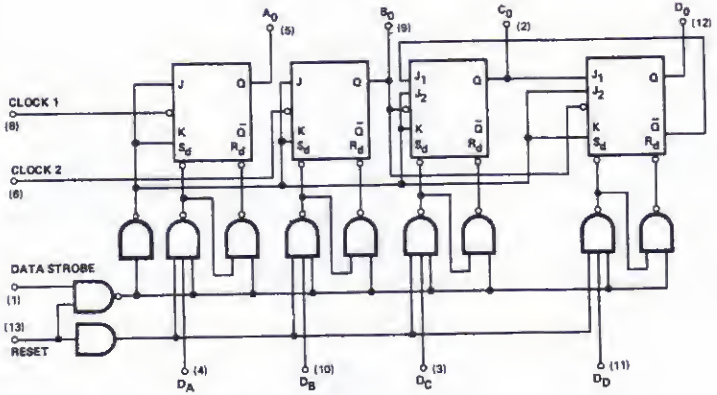
Decade (BCD) Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-In-Line Package

*Connected for BCD divide-by-ten operation (A connected to C_{P2})

FIGURE 5

8288



V_{CC} = (14)
GND = (7) A, F PACKAGES
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

TRUTH TABLE*

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

* Connected for divide-by-12 operation (output A connected to C_{P2})

FIGURE 6

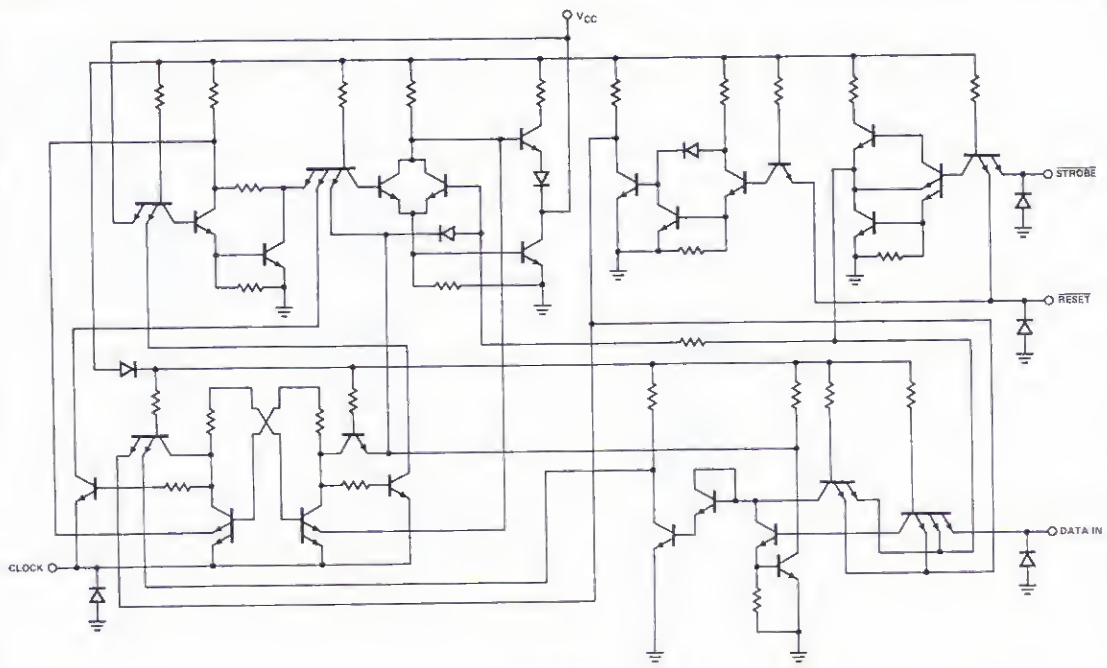


FIGURE 7

SIGNAL PROCESSING/CLOCK INPUT REQUIREMENTS FOR 8280/81/88

ENTERING PARALLEL DATA

While the STROBE line is activated (logic level "0") the Master section of each J-K flip-flop is disabled such that signal transitions at the clock inputs will have no effect.

The parallel preset inputs (D_A, D_B, D_C D_D) are enabled by a "0" on the STROBE input, affecting a parallel data transfer to the respective counter outputs. The STROBE input is buffered to reduce its input load to 1.6mA. This asynchronous parallel entry system is direct coupled, and therefore, is sensitive to DC input voltage levels only. The preset capability allows either counter to be utilized as event counters, fixed quantity totalizers, arbitrary length frequency dividers, and as storage registers.

The minimum strobe hold time ("0" level pulse width) is typically 20ns.

DIRECT RESET

The 8280 and 8281 can also be reset or cleared to zero (all outputs go to "0"), asynchronously. The direct coupled RESET input activates on "0" level. RESET overrides the clock and data strobe inputs. It is also buffered and represents a load of 3.2 mA in the logical "0" state. The minimum reset pulse width is also typically 20ns.

STROBE AND RESET RELEASE TIMES

If it is desired to count after a reset or strobe operation, strobe and reset release times must be considered.

The 8280/81/88 Counters will accept a clocking transition typically 30ns following the entry of parallel data or 50ns following the activation of Reset. These parameters are defined as Data Strobe Release Time and Reset Release Time respectively and are illustrated in Figure 8.

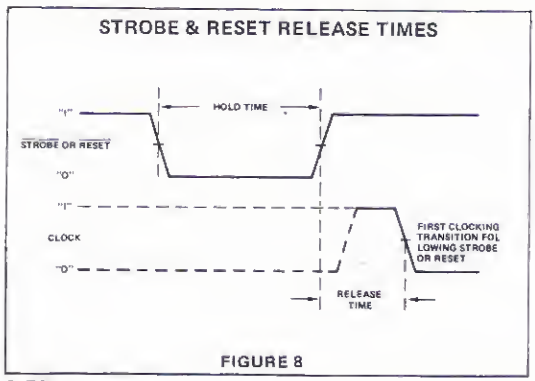


FIGURE 8

CLOCK REQUIREMENTS

The clock pulse amplitude should be 2.4V or greater with minimum pulse width of 15ns at the 1.5V points. Since the clocking mechanism is level-sensitive, the rise and fall times of the clock signal are not critical. However, in line with good TTL design techniques, the transition times should be kept less than 1μs to minimize the effects of noise.

The internal flip-flops are negative edge triggered. When counting, each flip-flop's master is enabled at the rising edge of the clock pulse and data is transferred to the slave (i.e. the output) on the falling edge of the input clock. The first flip-flop of each counter will accept clock (CLOCK 1) input repetition rates in excess of 20 MHz. The CLOCK 2 input will operate reliably at clock frequencies up to 10 MHz.

NEGATIVE EXCURSIONS AT THE CLOCK INPUT

The clock inputs of the 8280/8281 and 8288 have diode clamps to prevent system malfunctions caused by ringing or negative noise voltages which could otherwise cause false triggering. The clamp diodes limit negative excursions to about −1V.

DECOUPLING

Inadequate decoupling from V_{CC} to GROUND can cause system malfunctions. The 8280 and 8281 contain four outputs and one internal totem pole structure which current spike. A 0.01μF capacitor is required to achieve adequate decoupling. The ceramic disc capacitor should be placed as close as possible to the counter package.

AC CHARACTERISTICS OF THE 8280 AND 8281

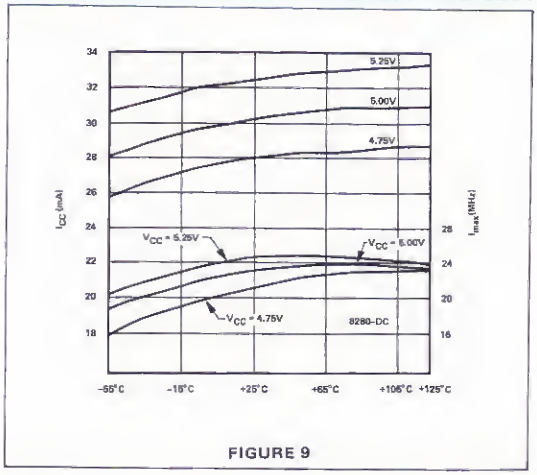


FIGURE 9

Some of the AC characteristics of the 8280 and 8281 are illustrated in Figure 9. The curve shows ONLY typical parameters and must not be construed as being guaranteed characteristics; however, assuming a possible deviation of up to ±25%, these curves demonstrate the rationale behind the guaranteed parameters.

This curve is a composite of two interdependent characteristics: max. freq. and I_{CC} vs. temperature. This composite shows the variation with temperature of I_{CC} at the maximum frequency of operation with all outputs fully DC loaded and for three values of V_{CC}.

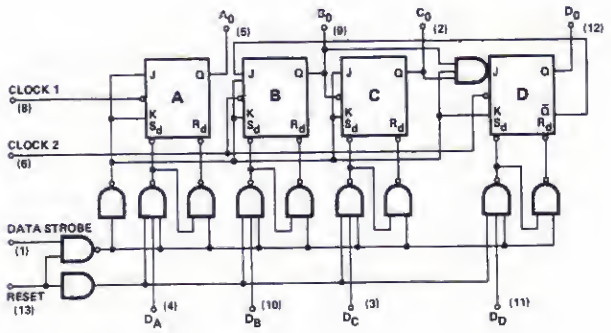
Although this data was taken only from the 8280 all general parameters are also characteristic of the 8281.

8290/91 AND 8292/93 COUNTER STORAGE ELEMENTS

The 8290 BCD Decade Counter, Figure 10 and the 8291 4-Bit Binary (16-state) Ripple Counter, Figure 11, are pin-for-pin interchangeable with the 8280 and 8281, respectively. The logic diagram for the 8290/91 counters is identical with that of the 8280/81. The 8290/91 counters are guaranteed for 40MHz operation with typical frequency capability in excess of 60MHz.

The data strobe holding time is 25ns maximum, with a typical requirement of 15ns. The reset holding time is 30ns maximum but typically reset can be accomplished within 20ns.

8290/92 LOGIC



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

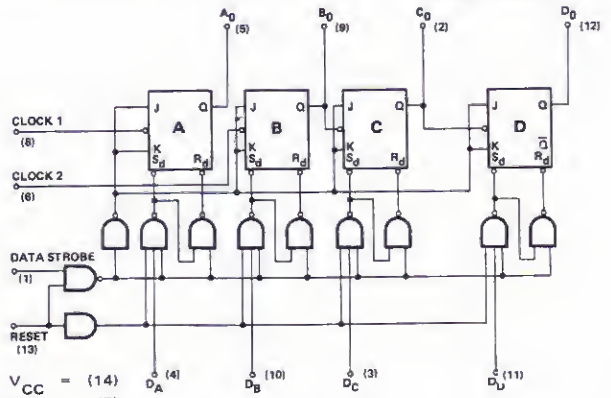
FIGURE 10

TRUTH TABLE*

Decade (BCD)				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

*Connected for BCD divide-by-10 operation A connected to C_{P2}.

8291/93 LOGIC



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

FIGURE 11

TRUTH TABLE*

Binary				
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

*Connected for divide-by-16 operation A connected to C_{P2}.

The 8292 is a low power variation of the 8280 BCD Decade Ripple Counter and is pin-for-pin interchangeable with both the 8290 and 8280. The 8293 is a low power variation of the 8281 4-Bit (16-State) Binary Ripple Counter and is pin-for-pin interchangeable with the 8281 as well as the 8291. Since a majority of counter requirements are at frequencies of less than 5 MHz, significant power saving can be realized by using the 8292 and 8293 for these requirements. Power consumption is typically 52 mW at 5 MHz when operating from a 5.00V supply. Propagation delay from CLOCK to output is typically 35ns for each bit.

8290 AND 8291 BASIC BINARY

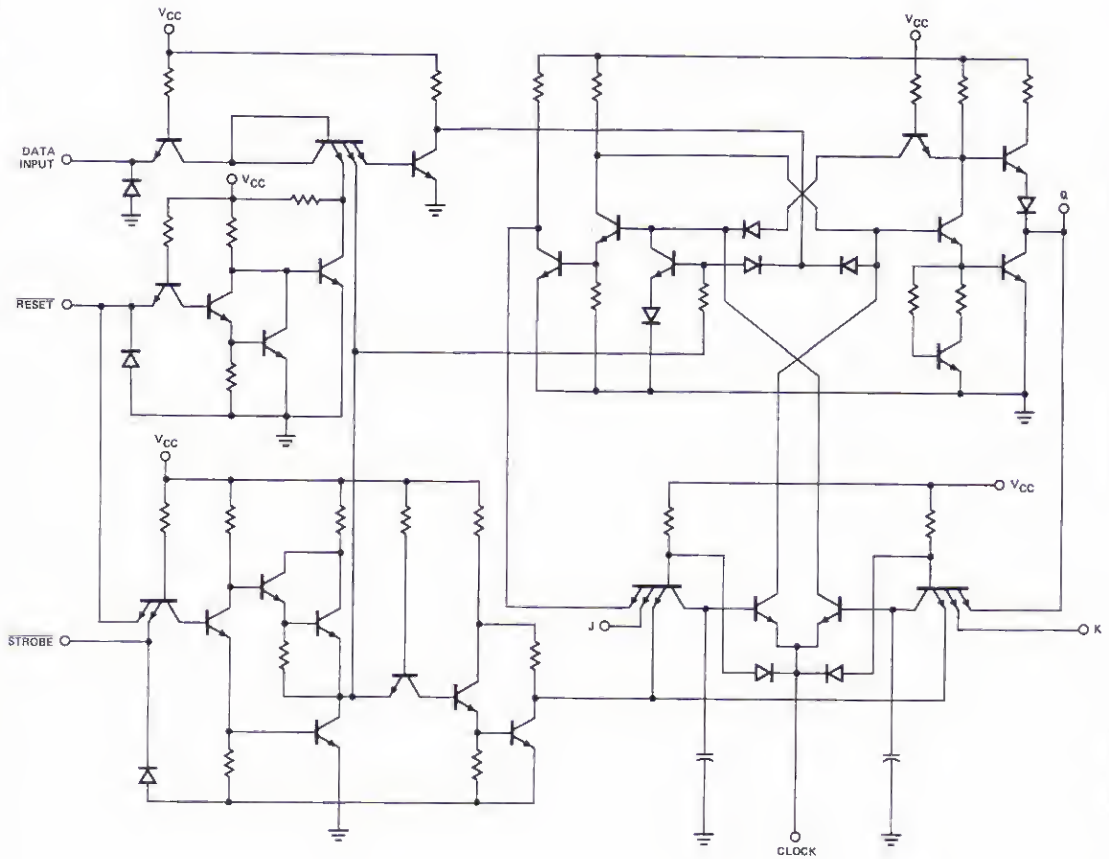


FIGURE 12

8292 AND 8293 BASIC BINARY

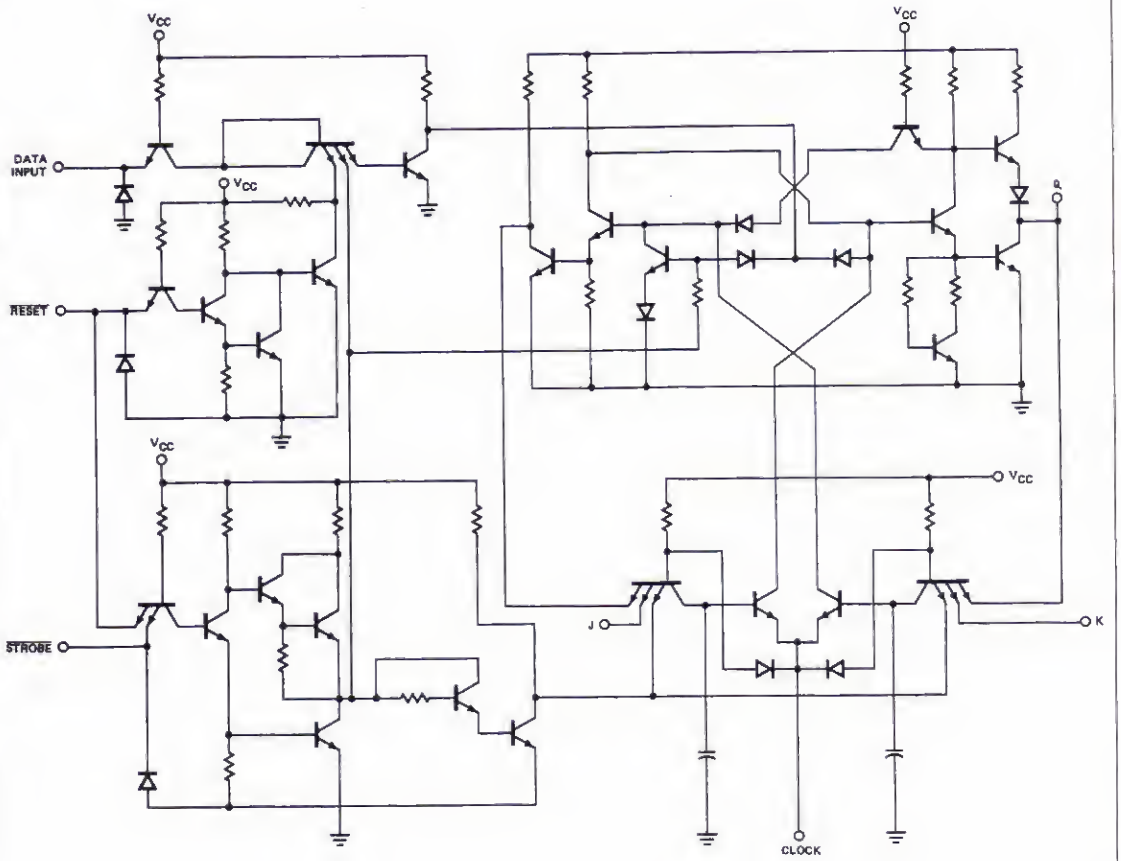


FIGURE 13

The internal flip-flop designs for the 8290/91 and 8292/93 respectively are shown in Figures 12 and 13. By using a stored-charge master in the master-slave storage elements high-speed and low power dissipation can be achieved in the 8290/91 and a low power medium speed counter design resulted in the 8292/93.

The Schottky versions of these counters, the 82S90 (logic as shown in Figure 10) and the 82S91 (logic as shown in Figure 11) have just been introduced. These dc-coupled, master-slave devices are pin compatible with the 8280/90/92 and 8281/91/93 respectively, but they operate at typically 100 MHz.

SIGNAL PROCESSING/INPUT CLOCK REQUIREMENTS FOR 8290/91 AND 8292/93

ENTERING DATA

The entry of any desired output code is achieved by placing that 4-bit code at the data inputs and strobing (STROBE = "0"). STROBE overrides the clock and the typical strobe interval is 15ns for the 8290/91 and 60ns for the 8292/93.

RESET

Total reset may be accomplished in typically 15ns for the 8290/91 and typically 45ns for the 8292/93. The activation of RESET ("0") dominates both CLOCK and STROBE while completely discharging the clocking capacitors, preventing transients at the output and the toggling of any binary.

STROBE AND RESET RELEASE TIMES

If it is desired to count after a reset or strobe operation, strobe and reset release times must be considered.

The 8290/91 Counters will accept a clocking transition typically 20ns following the entry of parallel data or the activation of Reset. The 8290/93 have a typical strobe/reset release time of 80ns. These parameters are defined as Data Strobe Release Time and Reset Release Time respectively and are illustrated in Figure 14.

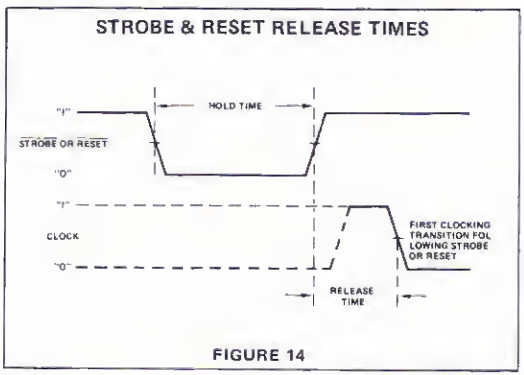


FIGURE 14

CLOCKING

Minimum clock pulse amplitudes of 2.4V with pulse widths 12.5ns for the 8290/91 and 25ns for the 8292/93 counters are recommended for reliable toggling. Fall times, independent of pulse width, should not exceed 75ns to achieve the energy transfer required to reliably activate the stored charge clock steering network. Compatibility with this fall time requirement is met with most TTL and DTL families.

NEGATIVE EXCURSIONS AT THE CLOCK INPUT

Negative ringing at the CLOCK input can cause the 8290 or 8291 to malfunction. If the clock goes to approximately -.6V, both input transistors can turn on and change the state of the output in the same manner as would a normal clock pulse making a "1" to "0" transition. Careful attention must then be paid to board layout to minimize ringing and to prevent noise from being coupled into the clock line.

Since the 8292 and 8293 use a stored-charge clocking mechanism similar to that in the 8290 and 8291, the same precautions should be taken to limit negative overshoot to less than -0.6 volt.

In those applications where negative ringing and noise is a problem, the DC-coupled master-slave designs, 8280/81 and 82S90/91 should be used.

MAXIMUM CAPACITIVE LOADING

The output latch circuit for the 8290 and 8291 is buffered (Figure 12) such that momentary grounding of any output will not cause that particular output to latch in a "0" state after the ground is removed. In addition, the only limitation to capacitive loading is the degradation of ripple propagation time and maintaining the required fall time of less than 75ns.

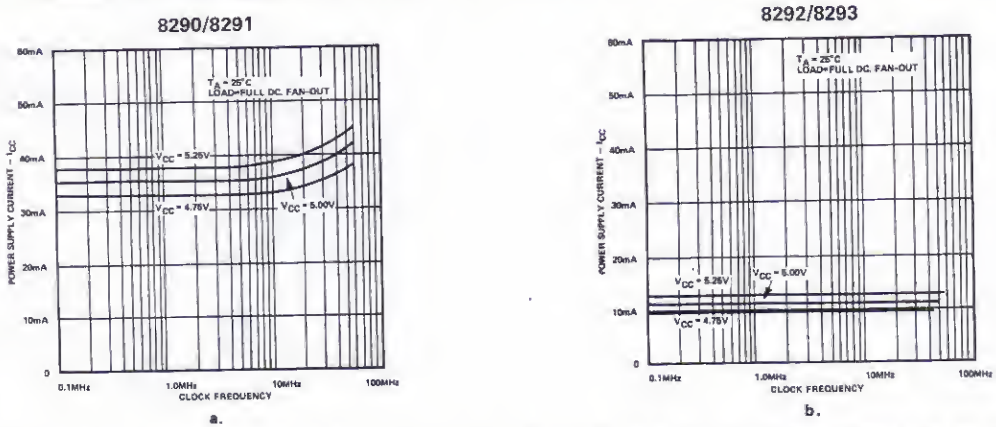
The outputs of the 8292 and 8293 are buffered (Figure 13). Therefore, the only limitation to capacitive loading of these high-speed counters is the degradation of ripple propagation time and maintaining the required fall time of less than 75ns.

DECOUPLING

Although the 8292 and 8293 are low-power counters, they contain the same number of totem pole output structures as the 8280, 8281, 8290 and 8291. As a result, a minimum decoupling capacitance of 0.01μF, non-inductive, is recommended for all counters discussed.

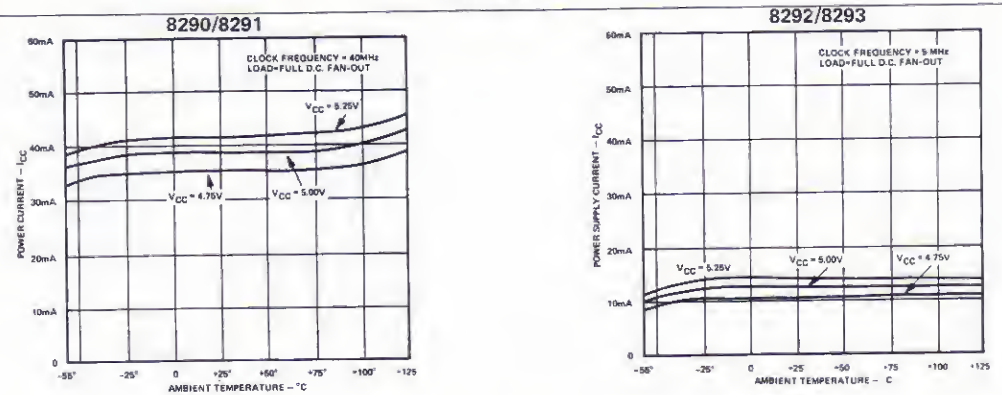
AC CHARACTERISTICS OF THE 8290, 8291, 8292 AND 8293

Shown in Figures 15 through 20 are the AC characteristics of the high-speed 8290 (8291) and low-power 8292 (8293) ripple counters. These curves show ONLY typical parameters and must not be construed as being guaranteed characteristics; however, assuming a possible deviation of up to ±25%, these curves demonstrate the rationale behind the guaranteed parameters. Each curve has two parts: the first curve shows the 8290 and the second curve shows the 8292.



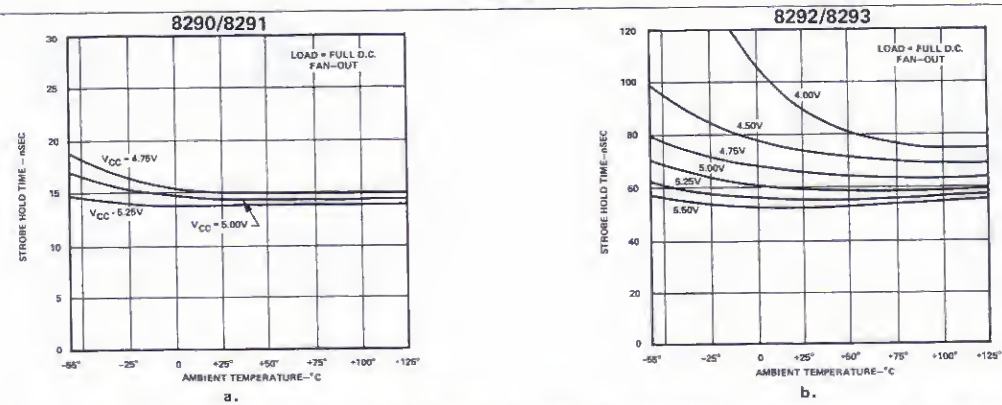
The power supply current vs. clock frequency shown in these curves for three values of V_{CC} (V_{CC} = 5.00V ±5%). All testing was performed at an ambient temperature of 25°C (T_A = 25°C) and with all outputs fully loaded.

FIGURE 15



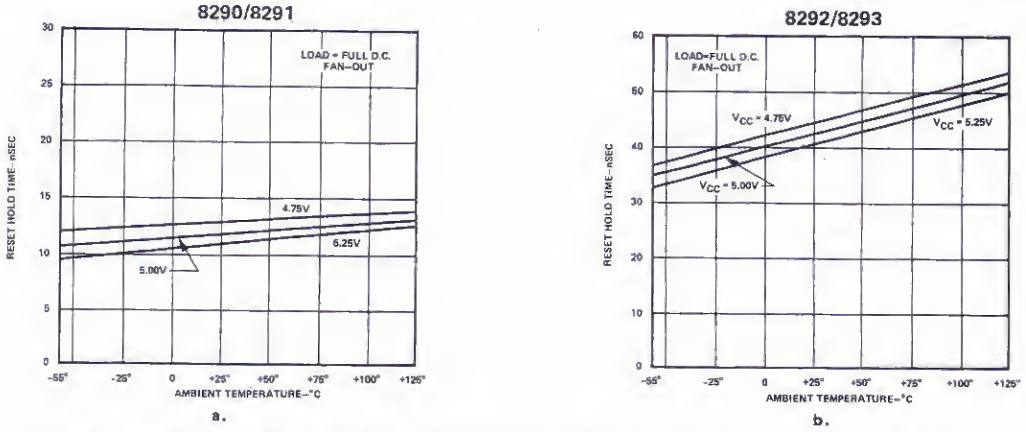
These curves demonstrate the variation of power supply current vs. ambient temperature at the guaranteed operating frequency of these counters under full DC fan-out and at V_{CC} = 5.00V ±5%.

FIGURE 16



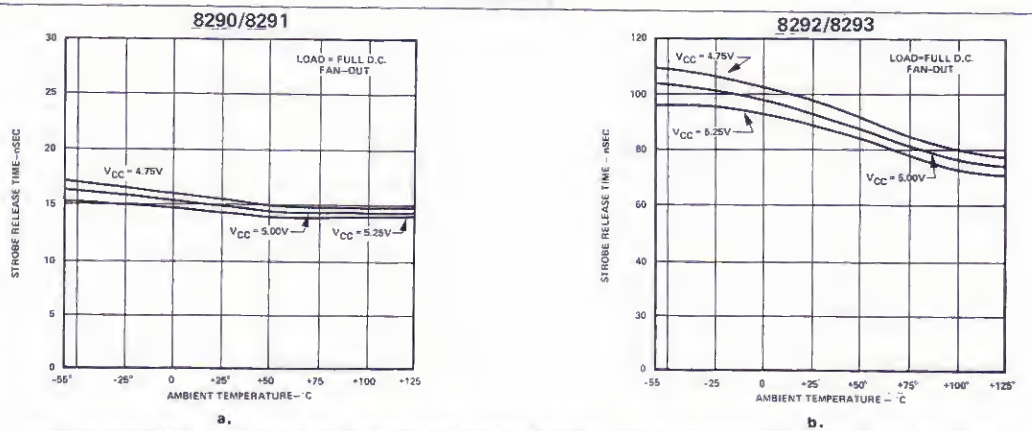
The typical strobe hold time vs. ambient temperature shows the change with temperature of the minimum time the strobe input must be at a "0" level to guarantee that the information present at the parallel data inputs will be stored in each binary element. The strobe hold time was measured for V_{CC} = 5.00V ±5% with all outputs under full DC fan-out.

FIGURE 17



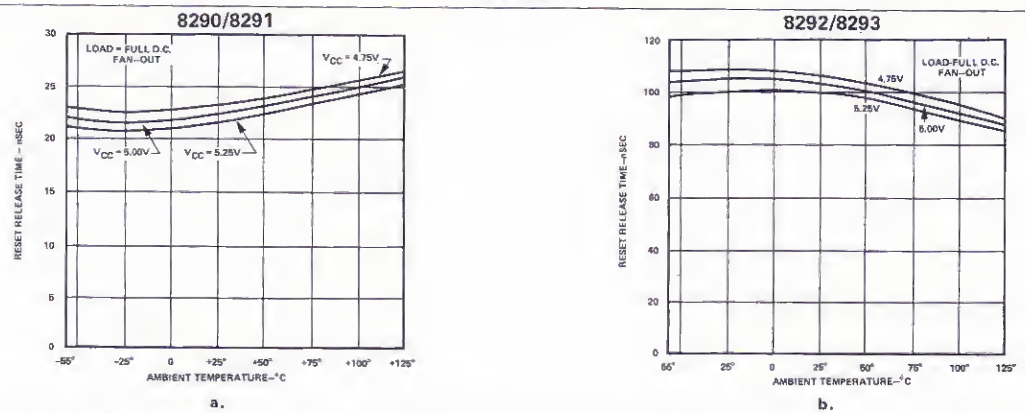
The typical reset hold time vs. ambient temperature shows the change with temperature of the minimum time the reset input must be at a "0" level to guarantee that all outputs are "0". All tests were taken with full DC fan-outs and V_{CC} = 5.00 ±5%.

FIGURE 18



The typical strobe release time vs. ambient temperature illustrates the variation with temperature of the minimum interval of time required before a clocking transition will be recognized by a counter after the strobe input has been disabled ("1").

FIGURE 19



The typical reset release time vs. ambient temperature illustrates the variation with temperature of the minimum interval of time required before a clocking transition will be recognized by a counter after the reset has been disabled ("1").

FIGURE 20

APPLICATIONS

CASCADING ASYNCHRONOUS COUNTERS

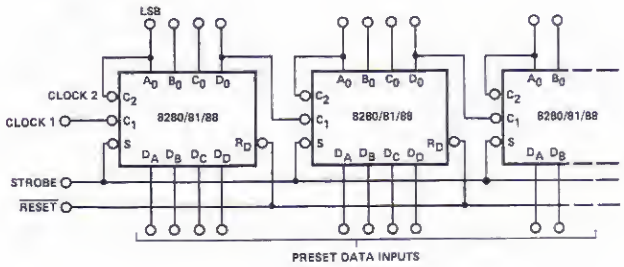


FIGURE 21

CASCADING COUNTERS

Figure 21 illustrates how several 8280/8281, 8288, 8290/8291, 8292/8293 and/or 82S90/82S91 counters may be cascaded in a ripple fashion to count or total any number of counts or events in any one or a combination of BCD decade, divide-by-twelve and/or 4-bit binary (hexadecimal) counting sequences.

The total number of counts before overflow occurs can be reduced by presetting the counter to some initial count. If a clocking signal is not present at the CLOCK 1 input after the STROBE ("0") is released (goes to a "1"), the preset information is stored. However, if a clocking signal is then applied, the counter will eventually overflow to zero at a count equal to the total capacity of the counter minus the preset count.

An example of this function is illustrated in Figure 22. An 8290 40 MHz BCD Decade Counter and two 8292 5 MHz BCD Decade Counters are cascaded producing a 40 MHz divide-by-1000 ripple counter. Notice that the high-speed 8290 was not required in the second and third decade positions due to the frequency division of ten in the first decade (8290). If the high-speed counters are unnecessary, significant power saving can be attained at frequencies below 5 MHz by using the low-power 8292 and 8293.

PRESETTING ASYNCHRONOUS COUNTERS

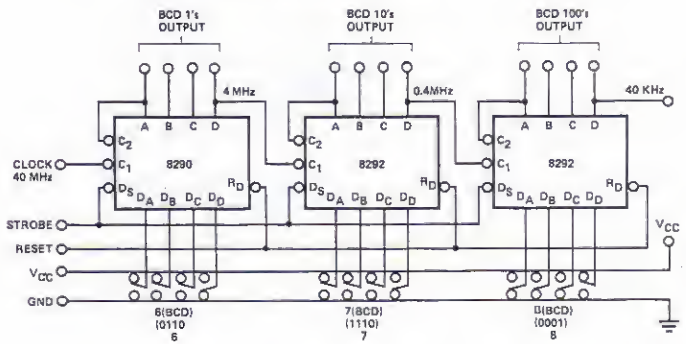


FIGURE 22

In the example (Figure 22), a preset count of 876 is strobed into the counter (STROBE = "0"). When the STROBE is released ("1"), the counter can count 124 events (clock transitions) before overflowing to zero.

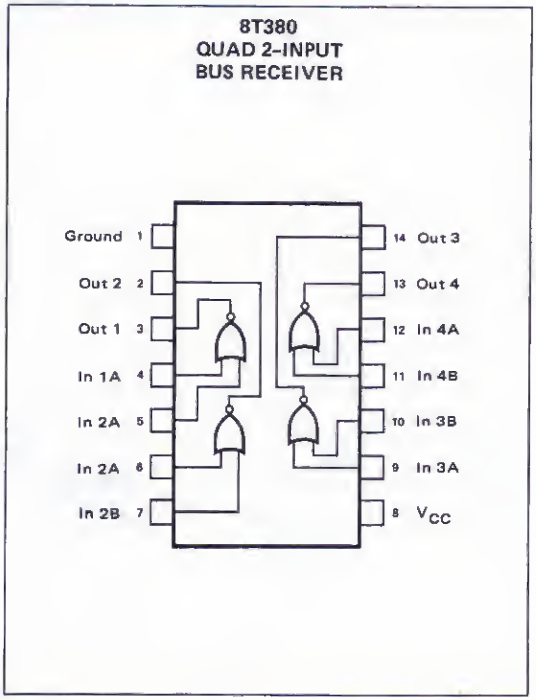
DIGITAL 8000 SERIES TTL/MSI

QUAD BUS RECEIVER WITH HYSTERESIS SCHMITT TRIGGER

DESCRIPTION

The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses that may be terminated in their characteristic impedance of typically 120 ohms. The external termination is intended to be a 180 ohm resistor from the bus to the +5V supply together with a 390 ohm resistor to ground. Built in hysteresis provided maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. Low input current allows several drivers and receivers to communicate over a common bus in "Party Line" fashion. The receiver has been designed to be pin compatible with the Signetics Utilogic II SP380 gate and provides increased noise immunity as well as lower input current. The 8T380 is ideal as a Schmitt-Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. All inputs have clamping diodes to simplify systems design.

PIN CONFIGURATION



FEATURES

- HIGH SPEED (TYP. 18ns)
- LOW INPUT CURRENT (TYP .15μA)
- BUILT IN HYSTERESIS (TYP. 1V)
- HIGH NOISE IMMUNITY (TYP. 1.6V)
- TTL/DTL COMPATIBLE
- INPUT CLAMP DIODES
- SP380/DM7836 PLUG-IN REPLACEMENT

TYPICAL APPLICATIONS BUS INTERFACE

High input impedance and high noise immunity make the 8T380 ideally suited for a bus receiver on a controlled impedance, bi-directional data bus. Controlled impedance data busses feature minimized reflected signals and pulse distortion. The supply voltage on the 8T380 may go to zero without affecting the impedance reflected to the bus. This is important when taking devices "off line" or when devices are attached for "standby" operation with power off.

A generalized "party line" bus interface is shown in Figure 1. Each driver/receiver combination can communicate with any other pair or all. Open collector NAND gates such as the Signetics 8881/7439 have adequate drive capability for the bus terminations as well as 20 driver/receiver pairs. In addition the bussing scheme is non-inverting as shown and bus drivers are activated by a logic "1", whereas bus receivers are activated by a logic "0".

Each terminator consisting of a 180 ohm resistor to V_{CC} and a 390 ohm resistor to ground is a 120 ohm — Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the bus. Using flat ribbon cable, a maximum reasonable length is 50ft. minus the combined length of all taps or stubs.

TYPICAL APPLICATIONS (Cont'd)

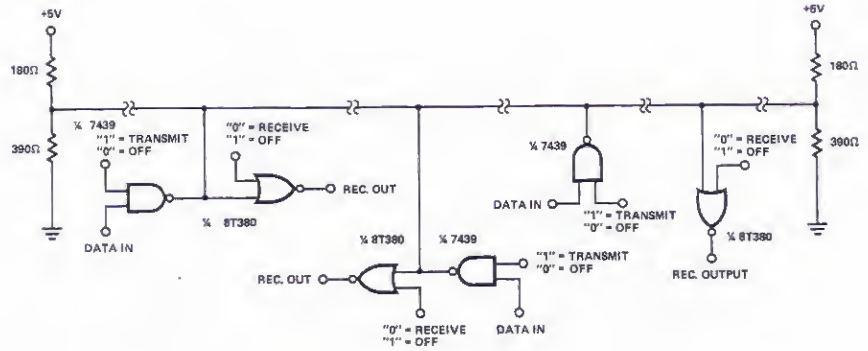


FIGURE 1

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and Wave-shipping applications such as Fig. 2b.

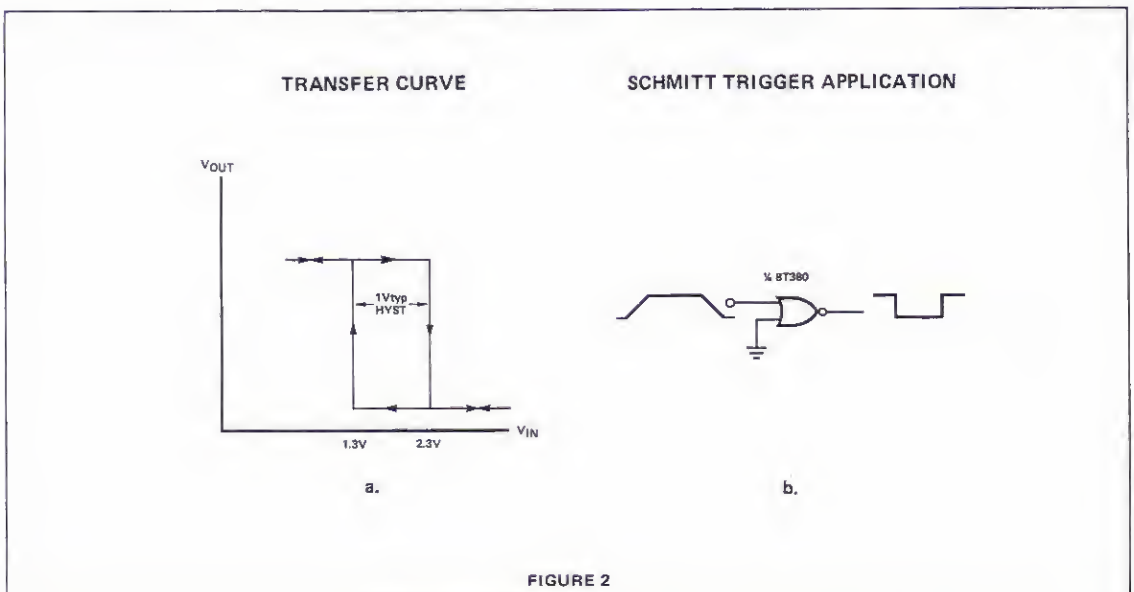
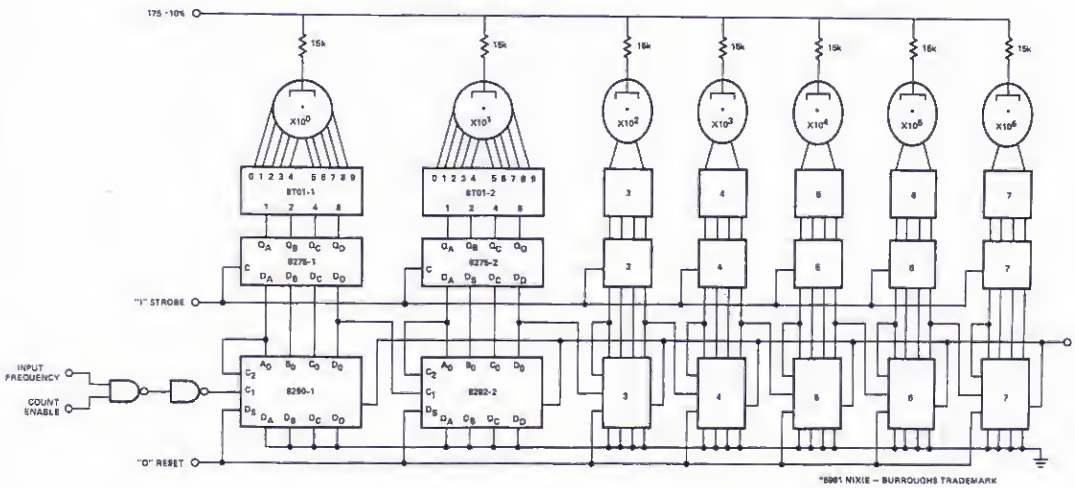


FIGURE 2

FREQUENCY MEASUREMENT

To measure frequency, the input frequency to the counter cascade must be gated by a time standard. The total count after the timing interval is then strobed into a storage/buffer register which could be an 8275 Quad Latch. The counter can be reset and allowed to count again while the stored preceding count is being displayed, as shown in Figure 8. With the 82S90 as the least significant decade, the maximum input frequency is guaranteed to be 85MHz.

FREQUENCY COUNTER



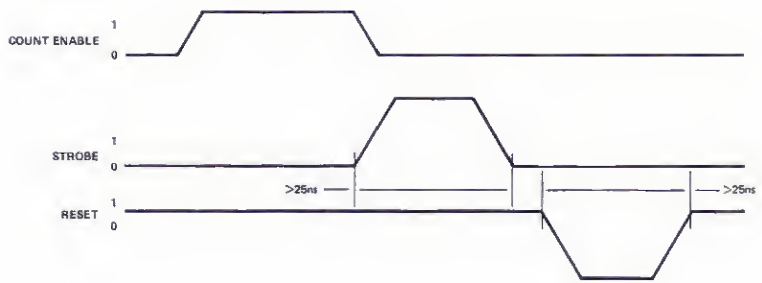


FIGURE 23

FREQUENCY DIVISION WITH SQUARE WAVE OUTPUT

A Bi-Quinary counter for the 8280/8290/8292/82S90 and a square wave divide-by-twelve counter for the 8288 are produced by connecting the D_O output to the A-bit CLOCK input and driving the B-bit CLOCK input with the input frequency. Figures 24 and 25 illustrate these connections. These connections are useful whenever an output square-wave has to be produced by a counter.

BI-QUINARY COUNTER

TRUTH TABLE FOR BI-QUINARY CONNECTION

CLOCK	B	C	D	A	
0	0	0	0	0	÷ 5
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	0	0	0	1	÷ 5
6	1	0	0	1	
7	0	1	0	1	
8	1	1	0	1	
9	0	0	1	1	
10	0	0	0	0	

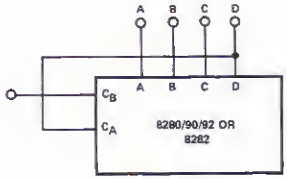


FIGURE 24

TRUTH TABLE FOR ÷12 WITH SQUARE WAVE OUTPUT

CLOCK	B	C	D	A	
0	0	0	0	0	÷ 6
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	1	0	1	0	
6	0	0	0	1	÷ 6
7	1	0	0	1	
8	0	1	0	1	
9	1	1	0	1	
10	0	0	1	1	
11	1	0	1	1	
12	0	0	0	0	

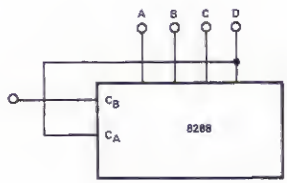


FIGURE 25

DIGITAL CLOCK DESIGN

To illustrate the versatility of Signetics' asynchronous MSI counters a digital clock design is shown in Figure 26. The 60Hz line frequency is fed directly into an 8T14 line receiver that is an excellent Schmitt trigger because of its built-in hysteresis of approximately 0.5V. As a result, TTL compatible rise and fall times are available to drive the 8288-1.

Since the 8288 is partioned into two sections, only the divide-by-six connection is needed. This counter is followed by an 8292 operating in the Bi-Quinary mode which results in a 1Hz square wave at the A output of counter 2.

To count down the seconds and minutes 8292's are used in the BCD mode and 8288's are operating in the divide-by-six mode. The hours are counted on a 12-hour basis as opposed to a 24-hour clock. Thus, in addition to the 8292-7 op-

erating in the BCD mode only a divide-by-two flip-flop is needed. To achieve this inexpensively, advantage has been taken off an unused flip-flop in the 8288-6.

Whenever the thirteenth hour (13:00:00) is detected the appropriate counters (6&7) are strobed such that they are preset to 1:00:00. Since 2/3 (8T14) was not used it is employed as a 3-input NAND gate to give the data strobe command.

For readout purposes seven-segment light emitting diode displays (Monsanto Man-1) are driven by 8T54 constant current LED decoder/drivers. Only one 5V power supply is needed and no current emitting resistors are required for the LED's. For good regulation a 550 Voltage Regulator with an external series pass transistor is employed.

The clock can be easily preset by use of a 2-pole 4-position switch. When setting hours and minutes, the second counters (3&4) remain reset while a 60Hz or 2Hz square wave respectively is applied to the C_{P_1} input of 8292-5.

12 HOUR DIGITAL CLOCK

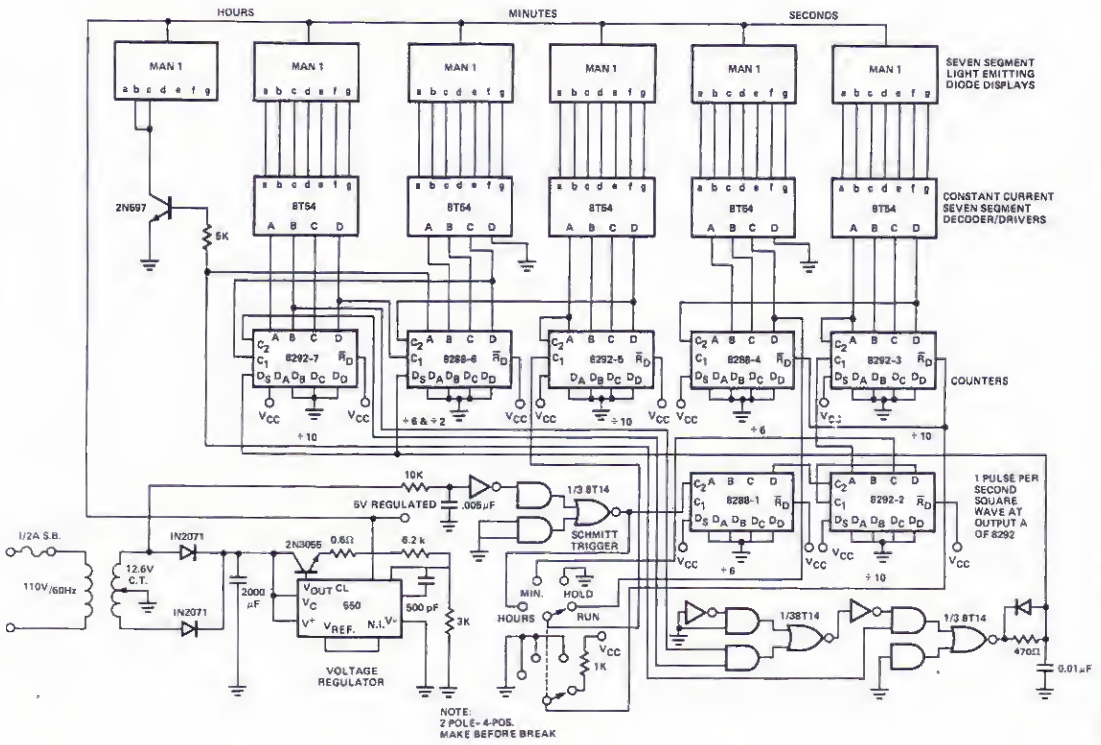


FIGURE 26

VARIABLE MODULUS COUNTERS

A variable modulus counter (VMC) is a programmable divider capable of dividing the input frequency by any desired count. The VMC finds extensive use in precise frequency division applications such as digital timers, sequential control operations and frequency synthesizers. It will be shown in the following discussion how BCD decade counters such as the 8280, 8290, 82S90 or 8292 and/or 4-bit binary counters such as the 8281, 8291, 82S91 and 8293 can be used in variable modulus counter (programmable divider) applications.

Figure 27 shows a generalized application of the variable modulus principle. A decade counter is cascaded with a 4-bit binary counter for a maximum possible modulus of 160 (i.e., a divide by ten counter cascaded with a divide by 16 counter yields 160 distinct output states, 0 to 159). The VMC operation is attained by presetting an initial condition (N_C) such that:

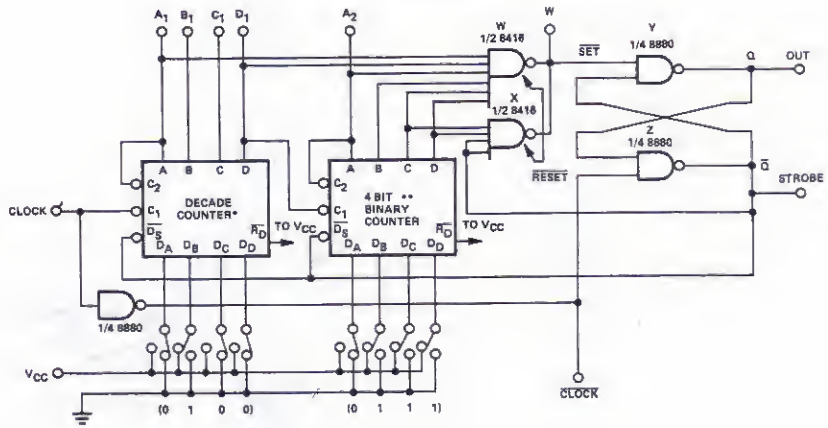
$$N_C = N_{max} - N$$

where: N_C = the preset number
N_{max} = the maximum count (i.e., modulus −1) of the cascaded counters
N = the desired frequency divisor

After N clock pulses, the preset counters in Figure 27 have attained their maximum count which is detected by Nand gates W and X resulting in a set pulse for the strobe latch consisting of cross-coupled gates Y and Z. The $\overline{Q}$ output of the strobe latch is connected to the data strobe inputs (DS) of the counters to parallel load them with the preset information. Since the inverted clock pulse resets the strobe latch, new information from the data inputs will be loaded every N clock pulses.

In the example, Figure 27, a modulus of 17 is desired. Thus, the counters are preset with binary information as shown and the full count on both counters is detected (full count = 1001 for the BCD counter and 1111 for the binary counter) at the point W.

VARIABLE MODULUS COUNTER



TIMING DIAGRAM

*DECADE COUNTERS:

8280	25 MHz TYP
8290	60 MHz TYP
82S90	100 MHz TYP
8293	LOW POWER (10 MHz, 52 mW)

**4-BIT BINARY COUNTERS:

8281	25 MHz TYP
8291	60 MHz TYP
82S91	100 MHz TYP
8293	LOW POWER (10 MHz, 52 mW)

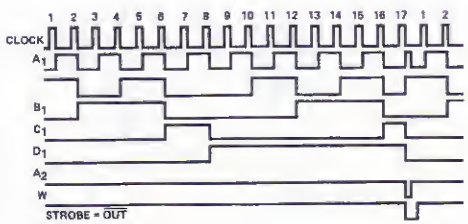


FIGURE 27

As seen in the timing diagram point W falls after 17 clock pulses (falling edges). A logical "0" at W sets the strobe latch and the strobe line stays low for as long as the clock is low, thus presetting the number $N_C = N_{max} - N$. The output frequency at the Q and $\overline{Q}$ outputs of the strobe latch is equal to the clock frequency divided by the desired modulus, 17.

Thus, in general, the presetting of the counter yields:

$$f_{out} = f_{in}/N$$
$$T_{out} = N\ T_{in}$$

HIGH SPEED VARIABLE MODULUS COUNTER

The principal limitation in the design of high-speed programmable counters is the strobe internal required to synchronously preset data into the counters.

The approach shown here will work in the programmable mode to over 40MHz and does not depend on clock-pulse width. The only restriction is that division is not possible for N = 1 or 2. But, all other numbers can be preset such that $f_{out} = f_{in}/N$. N is defined to be any number such that $3 \leqslant N \leqslant$ modulus -1.

THE CIRCUIT OPERATES AS FOLLOWS: One-third 74H11 3-Input AND-gate together with the multiple J-Inputs of the 74H102 decode the BCD number 97 at the falling edge of the clock when A_0 goes to A logical 1. Thus, after a small delay Δ, J' will be a logical 1 and on the fall of the next clock-pulse the flip-flop is triggered. The $\overline{Q}$ output will go low and the counters are strobed for one full clock interval. The fall of the 99th clock pulse toggles the flip-flop back since the J' input is at a logical 0.

HIGH SPEED VARIABLE MODULUS COUNTER

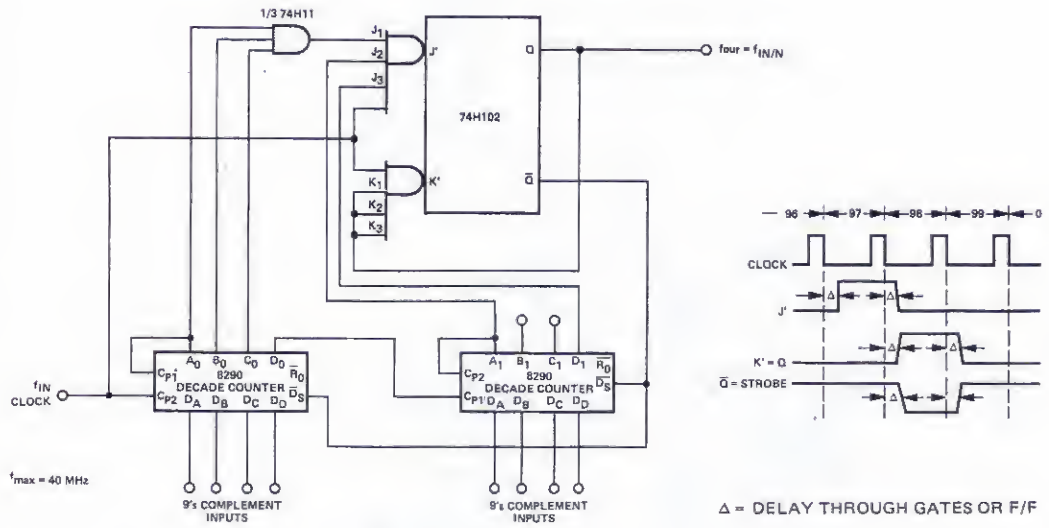


FIGURE 28

INTRODUCTION

The 8284 Hexadecimal (4-bit binary) Synchronous UP/DOWN Counter has sixteen unique 4-bit output codes which occur synchronously. The 8285 is a BCD Decade Synchronous UP/DOWN Counter and has ten unique binary-coded-decimal (8421) synchronous output states. The input/output functions of the 8284 and 8285 permit cascading of ten stages at about the guaranteed operating frequency of 20 MHz.

The operation and applications of these counters are discussed in detail. To help the system designer use the 8284 and 8285 more effectively, a section has been included on design precautions.

One of the major advantages of synchronous counters over ripple or asynchronous counters is that all outputs change at the same time, eliminating false output transition codes.

DEVICE DESCRIPTION

The 8284 and 8285 are synchronous UP/DOWN counters with reset to "0" and set to 15 (8284) or 9 (8285) asynchronous entry clock override (refer to Figure 1). Carry-Out and propagation of data occur synchronously with the falling edge of the clock input. The Q outputs of all four binaries are available, together with $\overline{Q_4}$ and Carry-Out.

The Count-Enable input goes to an AND gate which is tied to the toggle enable input of each binary element. This toggle enable AND gate also has the Carry-In, Set and Reset inputs connected to it. As shown in Figure 1, if one of these inputs is "0", the counter is disabled and will not count.

The Carry-In input, besides being tied to the toggle enable AND gate, also enables the Carry-Out output. The Count-Enable input has no effect on the Carry-Out. Therefore, the carry term can propagate through the counter while counting is inhibited by the Count-Enable ("0"). This input/output configuration makes it possible to cascade up to eleven stages of 8284's or 8285's with completely synchronous operation at high speeds which is not possible with ripple carry terms.

For the 8284 Hexadecimal Counter, a binary coded fifteen ($Q_1 = Q_2 = Q_3 = Q_4 =$ "1") in the count up mode (UP/$\overline{DOWN}$ = "1" level) will generate a Carry-Out (C_o = "1" level) when Carry-In goes high. The 8285 BCD Decade Counter in the count up mode generates a Carry-Out for a binary coded nine ($Q_1 = Q_4 =$ "1", $Q_2 = Q_3 =$ "0") when the Carry-In input goes to a "1" logic level. In the count down mode (UP/$\overline{DOWN}$ = "0" level), both counters generate a Carry-Out when the Carry-In is a logic "1" level and a binary coded zero ($Q_1 = Q_2 = Q_3 = Q_4 =$ "0") is detected. The propagation delay from Carry-In going to a logic "1" level to Carry-Out going to a logic "1" level is typically 15 nsec. The propagation delay from Clock to Carry-Out is typically 30 nsec.

The level sensitive clocking mechanism is buffered to reduce the clock line loading to a single TTL load. The clock input pulse width must be greater than 20 nsec at the 1.5V points of the rising and falling edges with an amplitude of 2.4V or greater.

CASCADING COUNTERS

The manner in which the first two 8284's or 8285's are connected is the key to cascading ten stages at the maximum guaranteed toggle rate of 20 MHz (Figure 2). The least significant counter (1) has the Count-Enable and the Carry-In inputs tied together to optimize speed. These paralleled inputs are used to enable ("1" level) or inhibit ("0" level) the counter. The Carry-Out is connected to the Count-Enable inputs of all succeeding stages. The Carry-In input of the second stage (2) is tied to V_{CC} which generates an "anticipated" Carry-In 16 counts (8284) or 10 counts (8285) before the Count-Enable is activated ("1" level) by the Carry-Out of the first stage (1).

The Set and Reset inputs provide complete clock lock-out when activated ("0" level). Reset and Set are accomplished in typically 20 nsec.

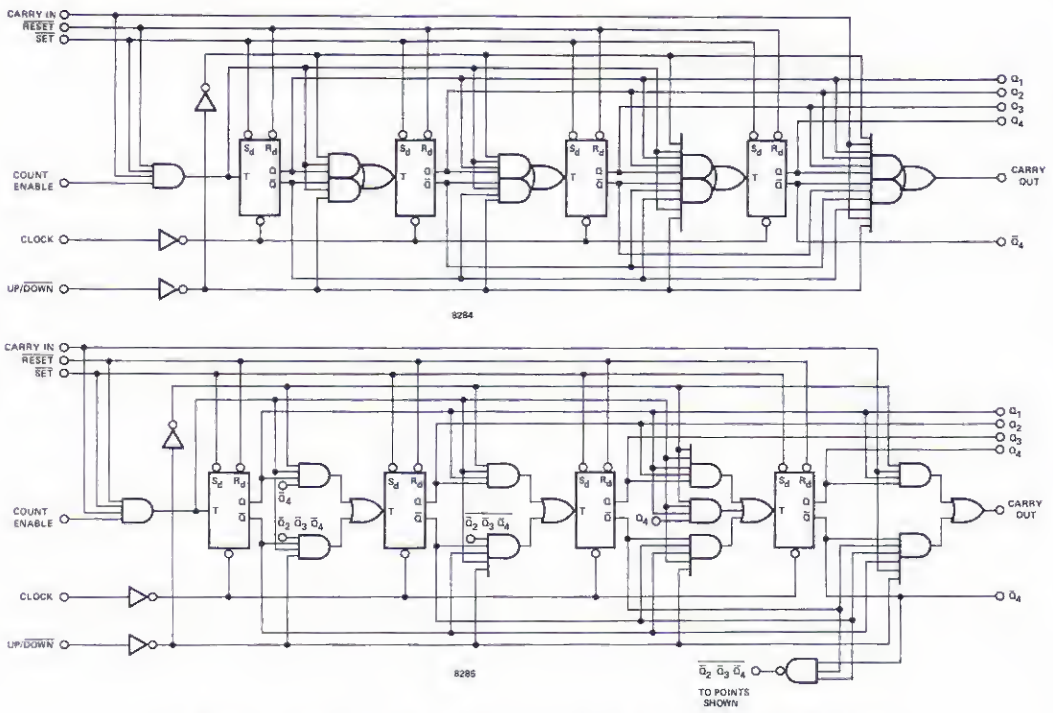
The 2's complement is generated for all negative binary counts of the 8284. The 2's complement $2_{(\overline{A})}$ of a binary word is found in Table 2.

DESIGN PRECAUTIONS

Certain precautions must be taken to ensure optimum system performance of MSI circuit designs using TTL techniques.

High frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include ground planes to minimize DC offsets and provide a low impedance path to reduce transient noise on the printed circuit boards.

LOGIC DIAGRAMS



CARRY OUT

$$\text{Carry Out}_{8284} = \text{Carry In}\,(Q_1\,Q_2\,Q_3\,Q_4\ \text{UP} + \bar{Q}_1\,\bar{Q}_2\,\bar{Q}_3\,\bar{Q}_4\,\overline{\text{DOWN}})$$

$$\text{Carry Out}_{8285} = \text{Carry In}\,(Q_1\,Q_4\ \text{UP} + \bar{Q}_1\,\bar{Q}_2\,\bar{Q}_3\,\bar{Q}_4\,\overline{\text{DOWN}})$$

FIGURE 1

MODE OF OPERATION

	SET	RESET	CARRY IN	COUNT ENABLE	UP/$\overline{\text{DOWN}}$	FUNCTION
A. Asynchronous	1	0	X	X	X	"0" (0000)
8284 Only	0	1	X	X	X	"15" (1111)
8285 Only	0	1	X	X	X	"9" (1001)
B. Synchronous						
	1	1	0	X	X	Hold*
	1	1	X	0	X	Hold*
	1	1	1	1	0	"Down" Count*
	1	1	1	1	1	"Up" Count*

*Function is synchronous with NEGATIVE going transition of the Clock pin.
X = don't care.

TABLE 1

DEFINITION OF 2's COMPLEMENT

2's Complement of A $2_{(\overline{A})} = {}^{1}(\overline{A}) + 2^{\circ}$ where $2_{(\overline{A})}$ = 2's Complement of A

$^{1}(\overline{A})$ = 1's Complement of A

EXAMPLE:

$$2_{(0\,1\,1\,0)} = {}^{1}(0\,1\,1\,0) + 0\,0\,0\,1 = 1\,0\,0\,1 + 0\,0\,0\,1 = 1\,0\,1\,0$$

Count Sequence — UP/DOWN = "0"

0 0 1 1	+3
0 0 1 0	+2
0 0 0 1	+1
0 0 0 0	0
1 1 1 1	−1
1 1 1 0	−2
1 1 0 1	−3

The 1's complement of a word is found by inverting all bits: $^{1}(1\,0\,1\,0) = 0\,1\,0\,1$.

TABLE 2

The current spike produced by the totem-pole output structures during "0" to "1" switching transitions can cause MSI elements to malfunction if V_{CC} is not properly decoupled to GROUND. A ceramic disc capacitance of 2000 pF or more for each totem-pole structure should be connected between V_{CC} and GROUND in close proximity to the MSI device to provide proper bypassing. The six output and two internal totem-pole structures of the 8284 and 8285 require a 0.02μF ceramic disc capacitor V_{CC} bypass.

Electrically open inputs degrade the AC and DC noise immunity as well as the switching speed of an MSI circuit. All inputs must be connected to low impedance sources for optimum noise immunity and switching speed. Unused inputs should be tied to a driving source, V_{CC} or GROUND. Unused inputs may be tied directly to V_{CC} if the power supply voltage never exceeds 5.5V; otherwise, the input should be tied to V_{CC} through a resistor (1KΩ). More than one unused input may be tied to V_{CC} through the same resistor.

For the 8284 and 8285, Reset and Set should be connected to V_{CC} when unused. Count-Enable when unused should be connected to the Carry-In input or to V_{CC}. The Carry-In input for a single counter or the first in a series of cascaded counters can be used to inhibit counting ("0" logic level) by a gate or, when unused, should be tied to V_{CC}.
All rise and fall times (10% to 90%) should be less than 1 μsec for a pulse amplitude of 2.2V or greater (not to exceed 5.5V).

If interconnections between devices are longer than 8 inches, precautions should be taken to minimize line reflections and ringing. All inputs to the 8284 and 8285 counters are internally protected with diode clamps. These diodes will limit negative excursions to −1V or less.

SYSTEM APPLICATIONS

CASCADING COUNTERS

Their unique input and output functions make possible the cascading of up to ten 8284 Hexadecimal and 8285 BCD Decade Counters while operating up to a frequency of 20 MHz. Being able to cascade ten stages permits the designer to count to 2_{40} or 1,099,511,627,776 counts for the 8284 and to 10_{10} or 10,000,000,000 counts for the 8285. These total counts can be achieved in both the up and down count modes with completely synchronous output code transitions. Further cascading past the eleventh stage is possible "if necessary", but the Carry-Out of the first stage (C_{o1}) would have to be buffered.

The following example is intended to clarify the interconnection scheme shown in Figure 2a. The example will show the cascading of ten 8285 BCD Decade Counters. The counters will be connected to take full advantage of the "anticipated-carry" capability.

Decade No. 1 has the Carry-In and Count-Enable inputs tied together. This input is used as the Count-Enable (CE) for the entire ten stage counter. The Carry-In (C_i) to Carry-Out (C_o) propagation delay is typically 15 nsec (as shown in Figure 2b) and the typical propagation delay from the falling edge of the Clock (C_L) to C_o is 30 nsec (as shown in Figure 2c for the ninth and tenth clocking transition).

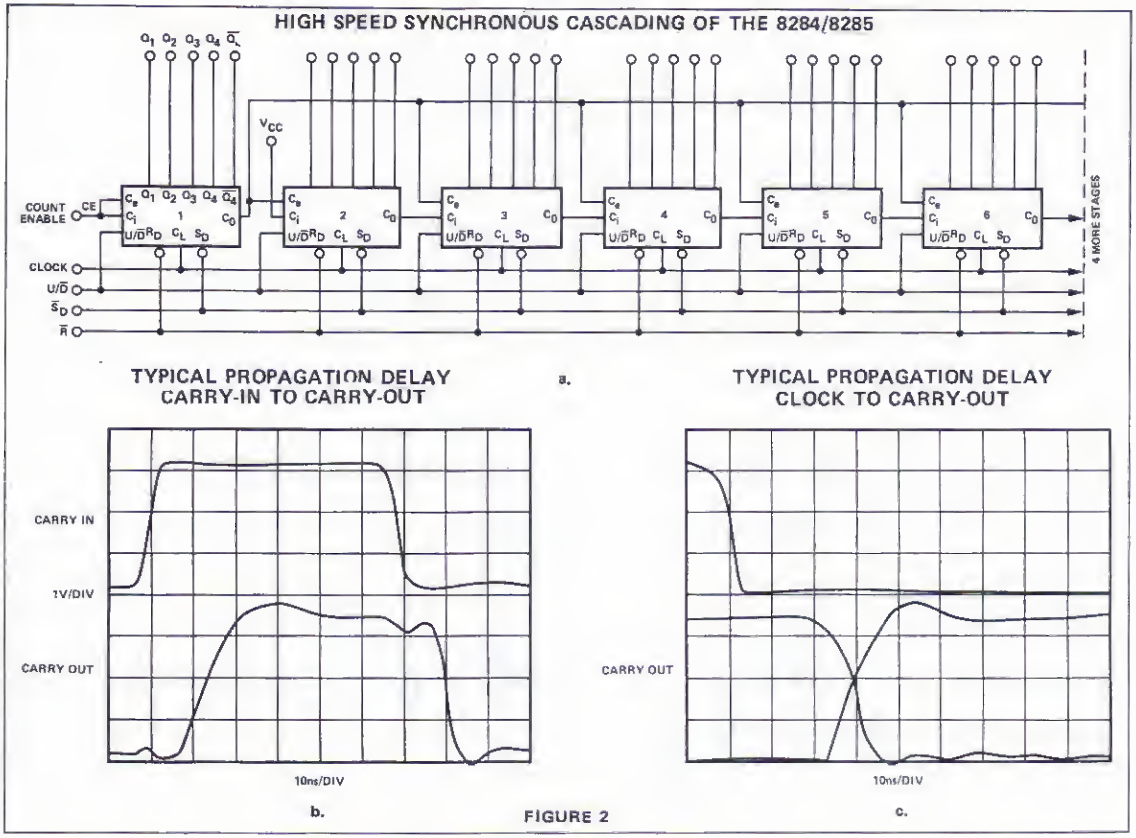


FIGURE 2

The second decade (2) has the C_{i2} tied to V_{CC}. The C_{o2} is therefore always enabled. The C_{o1} of the first decade which is connected to the C_e of the other nine decades enables the second decade to count one count for every ten counts in the first decade. C_{o2} is allowed to ripple through all successive decades. The propagation delays are shown below:

For the

9 9 9 9 9 9 9 9 9 to 9 9 9 9 9 9 9 9 0 transition

C_L to C_{o2} = 30 nsec x 1 decade = 30 nsec

C_{i3} to C_{o3} = 15 nsec x 8 decades = 120 nsec

-150 nsec -150 nsec

10 more counts in the first decade at 20 MHz = +500 nsec

+350 nesc

The 500 nsec between Count-Enables for the second through tenth decade allows three times the delay required for the carry term to propagate through nine decades. If the designer has a requirement for more than ten stages (either BCD Decade or Hexadecimal) of synchronous UP/DOWN counters, it is possible to buffer the C_o of the first stage and drive the C_e inputs of 24 stages at the maximum operating frequency of 20 MHz. A 25 stage Hexadecimal Counter is able to store 2^{100} counts. It would take approximately $2 \cdot 10^{15}$ years at 20 MHz to overflow this counter. A ten stage Hexadecimal will take over fifteen hours to overflow at 20 MHz. Therefore, few requirements ever exceed ten stages.

1'S COMPLEMENT GENERATOR

In the count down mode the 8284 (Hexadecimal) generates the 2's complement (Table 2) of any negative count. The 2's complement permits addition of positive and negative binary numbers without code conversion of the negative number. However, if the 1's complement or the reciprocal of the positive binary number is desired, 2^0 (LSB) must be subtracted from the 2's complement number:

-6 in 2's complement = 1 0 1 0

-2^0 -0 0 0 1

then: -6 in 1's complement = 1 0 0 1

where: $2_{(\overline{A})} - 2^0 = 1_{(\overline{A})}$

To generate the 1's complement automatically in the normal counting sequence of a system using 8284's requires the addition of a single 8H70 (Triple 3-Input NAND Gate). As shown in Figure 3, the combined Carry-Out ($C_e \cdot C_i$) detects all zero crossings. The 1's complement has two states for zero, all 0's and all 1's. All outputs are Set ($\overline{S}_D$ = "0") to "1"s when all "0" are detected in the count "DOWN" ($U/\overline{D}$ = "0") mode. Conversely, all outputs are Reset ($\overline{R}_D$ = "0") to "0"s when all 1's are detected in the count "UP" ($U/\overline{D}$ = "1") mode. An example of the generated "1"s complement counting sequence is shown in Table 3.

GENERATION OF 1's COMPLEMENT NEGATIVE BINARY NUMBERS

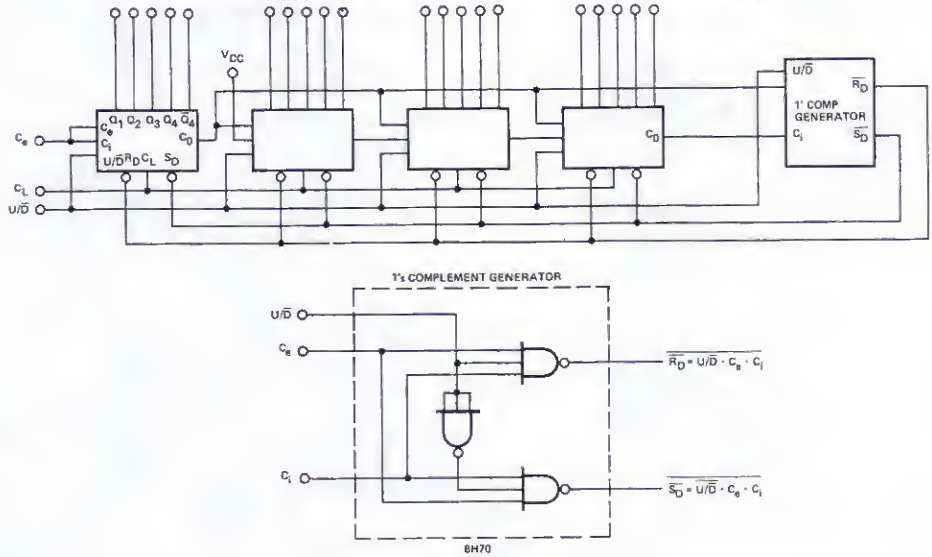


FIGURE 3

TABLE 3

"1"s COMPLEMENT COUNTING SEQUENCE

Clock	Decimal	Binary	$C_e \cdot C_i$	$U/\overline{D}$	S_D	R_D
0	+3	0 0 1 1	0	0	1	1
1	+2	0 0 1 0 ◄ 1's Comp.	0	0	1	1
2	+1	0 0 0 1	0	0	1	1
3	0	0 0 0 0	1	0	0	1
	0	1 1 1 1	0	0	1	1
4	-1	1 1 1 0	0	0	1	1
5	-2	1 1 0 1 ◄	0	0	1	1
6	-1	1 1 1 0	0	1	1	1
7	0	1 1 1 1	1	1	1	0
	0	0 0 0 0	0	1	1	1
8	+1	0 0 0 1	0	1	1	1

MAGNITUDE AND SIGN GENERATOR

The 1's and the 2's complement representations of negative numbers are insufficient for some applications. When decoding the outputs of 8285's for numeric readouts, it is desirable to produce the absolute value of a number and its sign. A decoding system with these features eliminates any further decoding to display negative numbers. The magnitude and sign capability of the configuration shown in Figure 4 simplifies the decoding of negative numbers for both the 8284 and the 8285.

As shown in Figure 4, Gates 1, 2, 3 and 4 form a D-type latch. The U/D input is transferred to point P (Gate 3) when the combined Carry-Out ($C_e \cdot C_i$) goes to a "1" level. The function generated at the output $U/\overline{D}$ is:

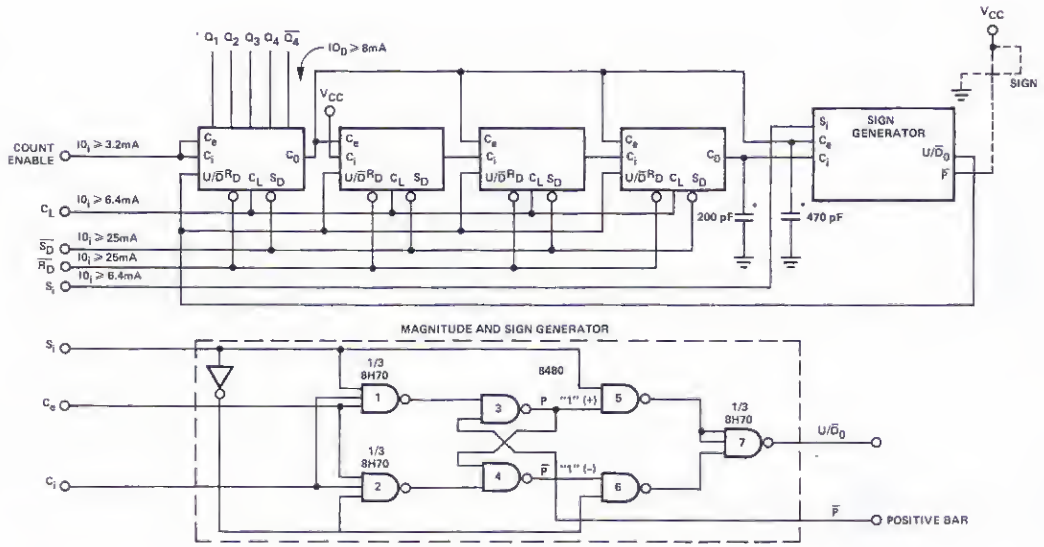
$$U/\overline{D}_o = S \cdot P + \overline{S} \cdot \overline{P}$$

where: P = "1" ($\overline{P}$ = "0") then $N \geq 0$
P = "0" ($\overline{P}$ = "1") then $N \geq 0$
N = Number of counts
S = "1", count positive
S = "0", count negative

The latch (P) is enabled when Carry-In ($C_e \cdot C_i$) goes to "1" which occurs at all zero crossings.

Table 4 shows the count sequences generated for a single 8285 BCD Decade Counter with the magnitude and sign generator connected.

GENERATION OF MAGNITUDE AND SIGN



*CAPACITORS ELIMINATE SPIKES DUE TO UNEQUAL OUTPUT LOADING

FIGURE 4

COUNT SEQUENCE USING THE MAGNITUDE AND SIGN GENERATOR

S*	Carry-Out $C_e \cdot C_i$	P	U/$\overline{D}$	N Clock	Binary	Decimal
0	0	1	0	0	0 0 1 1	+3
0	0	1	0	1	0 0 1 0	+2
0	0	1	0	2	0 0 0 1	+1
0	0	1	0	3	0 0 0 0	0
0	1/0	0	1	4	0 0 0 1	-1
0	0	0	1	5	0 0 1 0	-2
0	0	0	1	6	0 0 1 1	-3
1	0	0	0	7	0 0 1 0	-2
1	0	0	0	8	0 0 0 1	-1
1	0	0	0	9	0 0 0 0	+0
1	1/0	1	1	10	0 0 0 1	+1
1	0	1	1	11	0 0 1 0	+2
0	0	1	0	12	0 0 0 1	+1
0	0	1	0	13	0 0 0 0	0
0	1/0	0	1	14	0 0 0 1	-1

*S = "1" — Count Up S = "0" — Count Down

TABLE 4

SYNCHRONOUS COUNTER DECODING

Synchronous counters such as the 8284 and 8285 have an advantage over ripple or asynchronous counters (8280 and 8281) in high speed decoding applications. The decoding of high-speed memories and general high speed multiplexer applications requiring precise code transitions should be driven by synchronous code changes. The outputs of an asynchronous counter change in a rippling sequence, as seen in Figure 5a. To achieve synchronous code transitions, an 8275 Quad D-Type Latch must be used to strobe the outputs of an asynchronous counter after the ripple interval (see Figure 5c). The 8281 requires a ripple interval of at least 100 nsec before the outputs can be strobed. Due to their low relative power consumption and low cost, the 8280 and 8281 Ripple Counters are excellent for all applications not requiring high speed synchronous output code transitions or UP/DOWN counting capabilities.

All the outputs of an 8284 or 8285 synchronous counter change simultaneously, eliminating the generation of false transition codes. Figure 5b shows the outputs of the 8284 changing 22 nsec* after the falling edge of the input clock. However, as seen in Figure 5a, the 8281 requires typically 80 nsec before the correct code is achieved.

*Propagation delays are measured from the 1.5V points.

1-OUT-OF-N DECODING

A 1-in-16 decoder (4 lines to 16 lines) using an 8284 (Hexadecimal Counter) and two 8250's (Binary to Octal Decoders) is shown in Figure 6a. The necessity of having the $\overline{Q}_4$ output is apparent in this application. If $\overline{Q}_4$ was not available, an inverter would have to be connected to the Q_4 output to generate $\overline{Q}_4$ at some finite delay time after Q_4. This delay could cause possible decoding errors.

Figure 6b shows the use of an 8285 BCD Decade Counter in conjunction with an 8251 BCD to Decimal Decoder (Figure 6c).

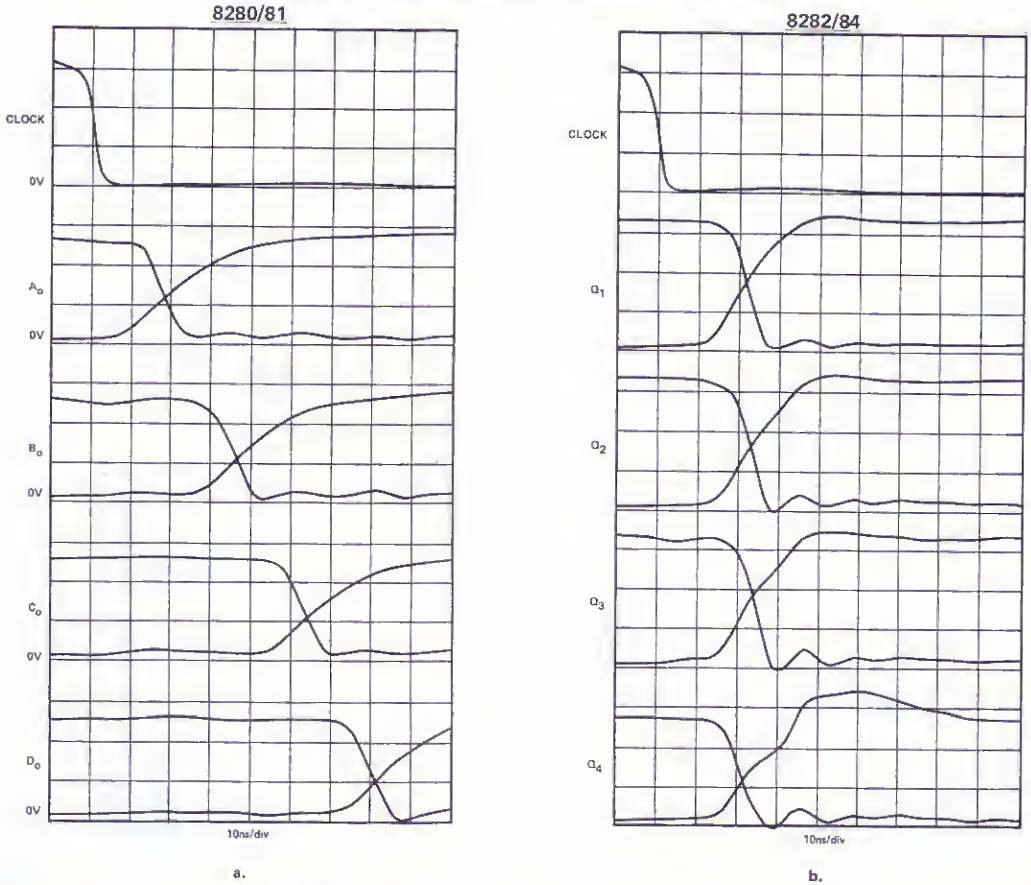
The typical propagation delay for both counter decoder systems from Clock input to decoded output is 30 nsec.

FREQUENCY MULTIPLEXER

The frequency multiplexer shown in Figure 7b uses two 8284's and one 8232, 8-Input Digital Multiplexer (Figure 7a). This circuit permits any one of the 8 outputs of the 8-bit synchronous binary counter (two 8284's) to be decoded. The decoded output frequency is determined by the inputs N_0, N_1, N_2 and Inhibit as shown in the truth table in Figure 7.

The propagation delay from the falling edge of the clock to the outputs of the multiplexer (8232) is the same for all decoded frequencies. This propagation delay is typically 37 nsec for true output (f_o) and 30 nsec for the inverted output ($\overline{f}_o$).

COMPARISON OF SYNCHRONOUS AND ASYNCHRONOUS COUNTERS



STROBE LATCH FOR ASYNCHRONOUS COUNTER

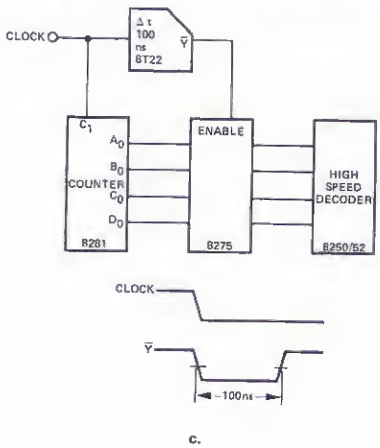
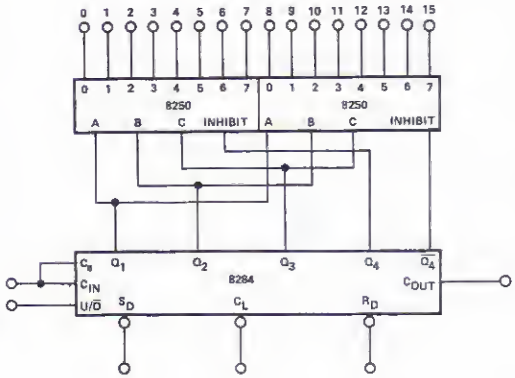


FIGURE 5

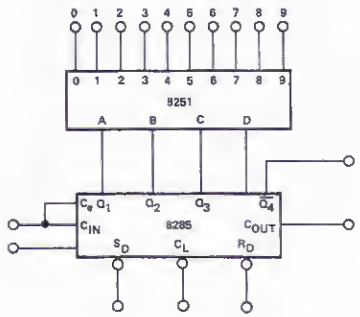
SYNCHRONOUS COUNTER DECODING

1-OF-16 COUNTER/DECODER



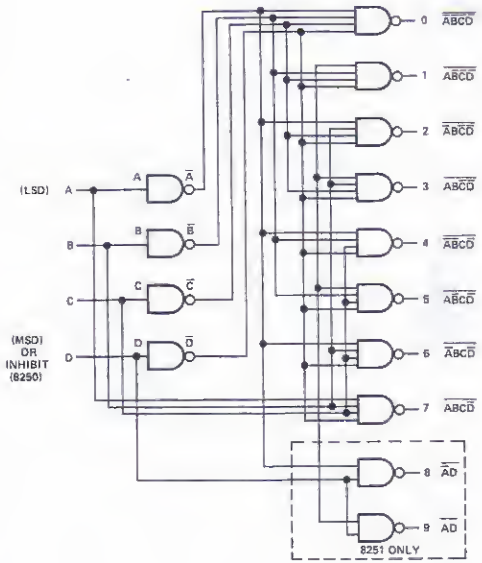
a.

1-OF-10 COUNTER/DECODER



b.

8250/51 OCTAL/DECIMAL DECODER LOGIC



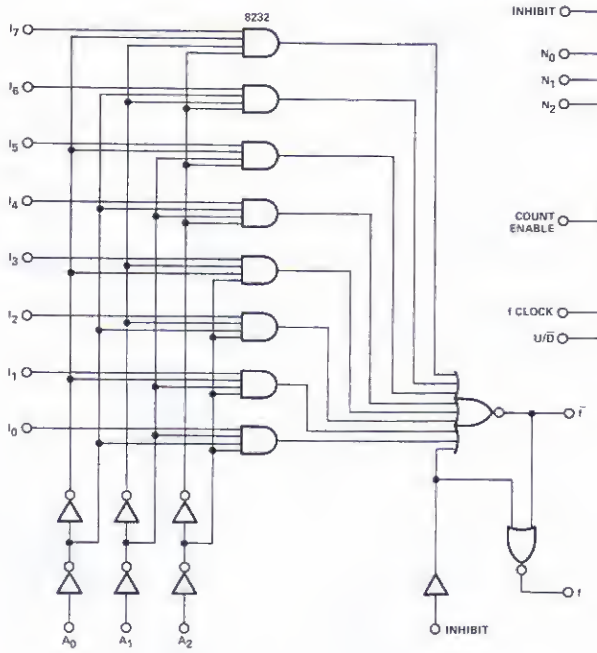
c.

FIGURE 6

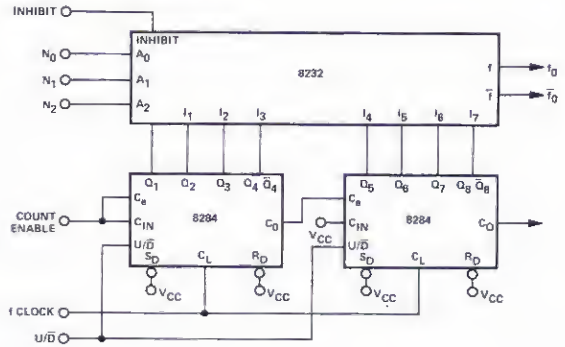
VARIABLE MODULUS COUNTER

Figure 8 shows a variable modulus counter or programmable frequency divider using synchronous counters (8284's or 8285's) and 4-bit Digital Comparators (8242's). The 8242 (see truth table) has open-collector outputs. As shown in Figure 8 for four 8284's or 8285's, a "1" logic level is generated at point Z when the counter's output digitally compare with the input binary (8284) or BCD (8285) sixteen bit word. The counter must be connected in the count UP (U/D = "1") mode. R_L was calculated for minimum propagation delay. The Reset ("0") pulse will be greater than 40 nsec. The Reset driver, such as an 8H90 Inverter, must be able to sink at least 24mA ($I0_o \geqslant 24mA$).

OCTAVE FREQUENCY MULTIPLEXER



a.



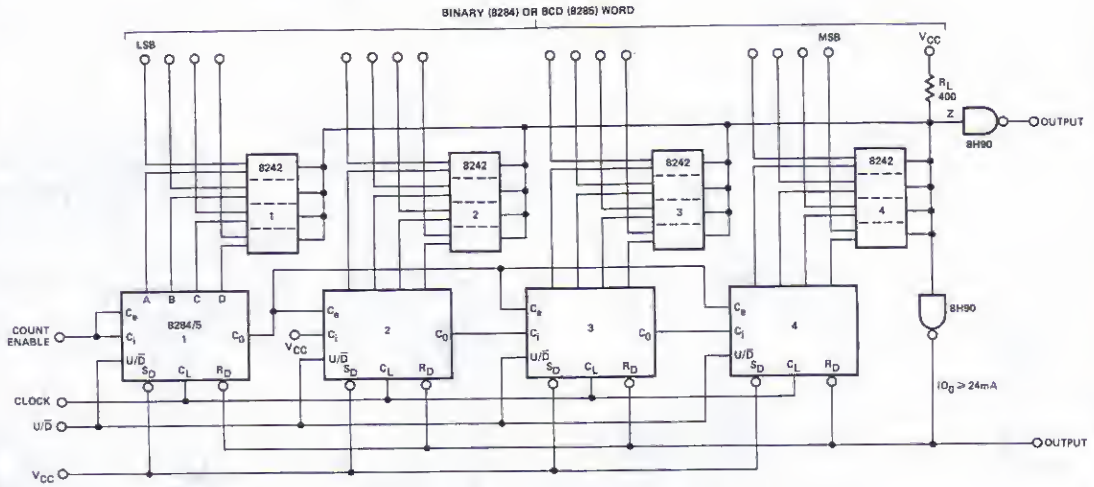
b.

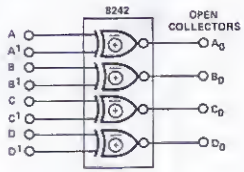
FIGURE 7

TRUTH TABLE FOR FREQUENCY MULTIPLEXER

N_0	N_1	N_2	INHIBIT	f_o	$\bar{f}_o$	
0	0	0	0	Q_1	$\bar{Q}_1$	f/2
1	0	0	0	Q_2	$\bar{Q}_2$	f/4
0	1	0	0	Q_3	$\bar{Q}_3$	f/8
1	1	0	0	Q_4	$\bar{Q}_4$	f/16
0	0	1	0	Q_5	$\bar{Q}_5$	f/32
1	0	1	0	Q_6	$\bar{Q}_6$	f/64
0	1	1	0	Q_7	$\bar{Q}_7$	f/128
1	1	1	0	Q_8	$\bar{Q}_8$	f/256
X	X	X	1	0	0	

VARIABLE MODULUS COUNTER





TRUTH TABLE FOR 8242 COMPARATOR OR EXCLUSIVE NOR

A	A^1	A_0
0	0	1
0	1	0
1	0	0
1	1	1

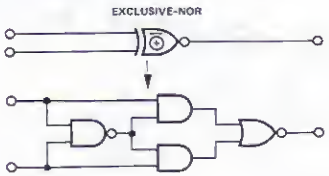


FIGURE 8

BCD ARITHMETIC UNIT

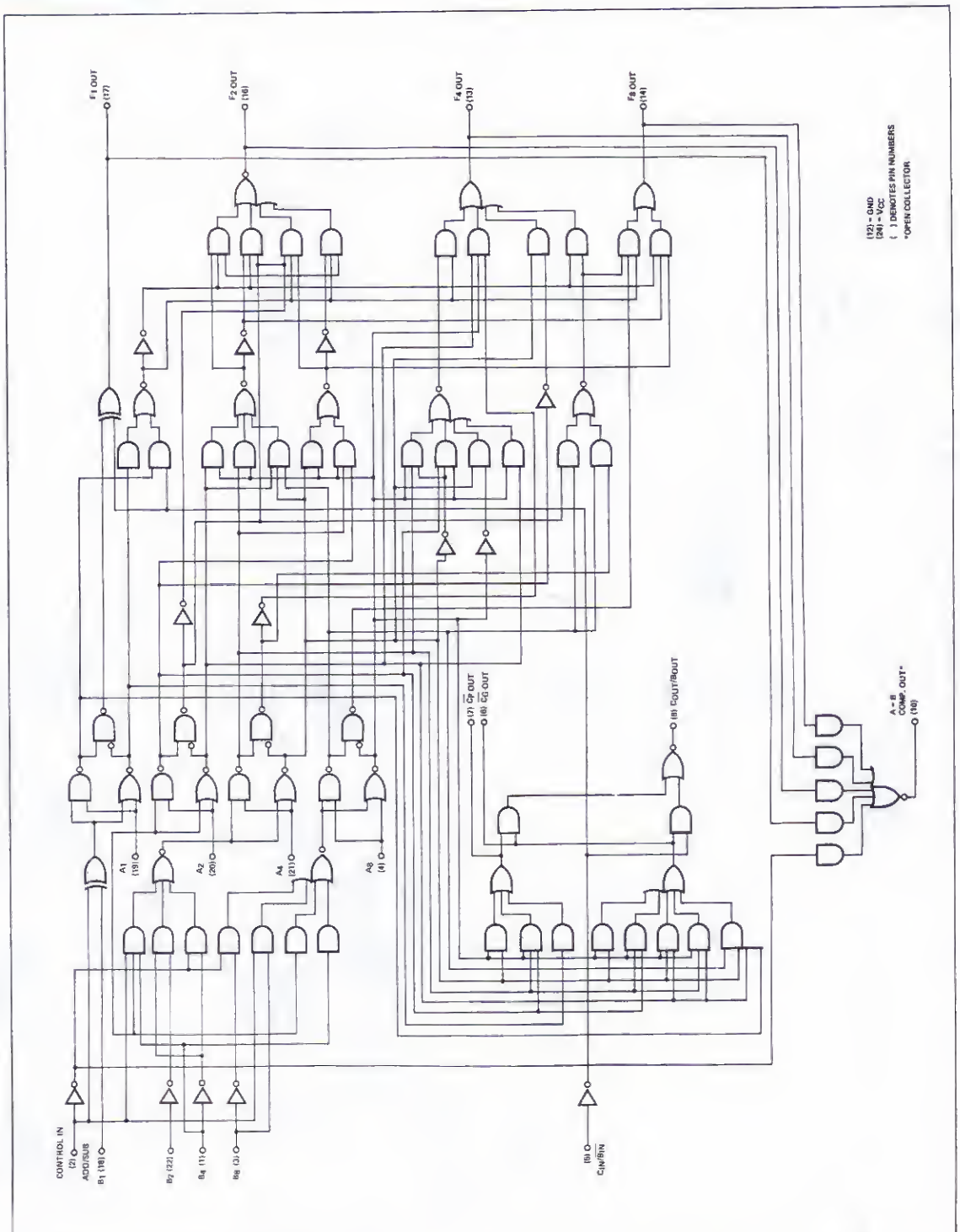
DESCRIPTION

The 82S82 BCD Arithmetic Unit is designed to provide the sum or difference of the 4-bit BCD numbers. Carry/Borrow inputs and outputs are provided to allow for cascading devices. The device also provides the $\overline{C_G}$ and $\overline{C_P}$ outputs to allow the 74S182, look-ahead carry generator, to be used for high speed, multiple digit arithmetic operations. A "Compare" output provides an indication that the A and B inputs are equal.

FUNCTION TABLE

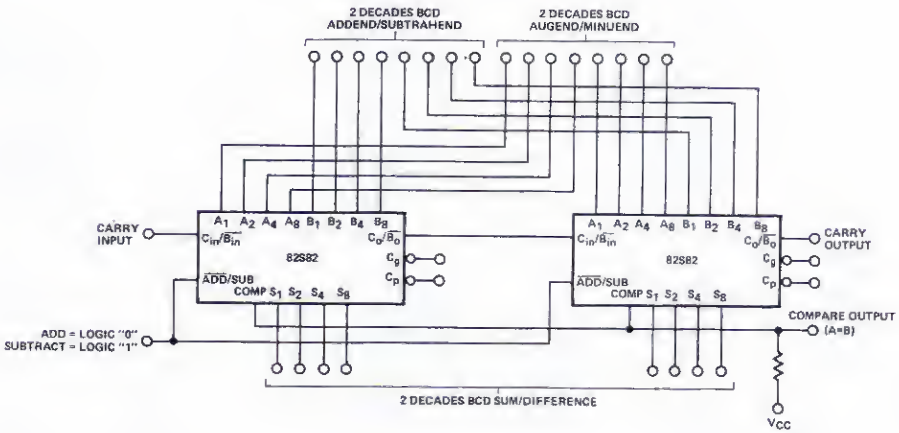
FUNCTION	Add/Sub	A_N	B_N	C_{in}/B_{in}	F_N	C_{out}/B_{out}	COMPARE
Add	0	Augend	Addend	0	A+B	"," it $F_N>9$	0
				1	A+B+1		
Subtract	1	Minnend	Subtrahend	1	A-B	"0" if	"1" if A-B=0
				0	A-B-1	$F_N<0$	"1" if A-B-1=0
Binary to	0	$0 \leq A \leq 9$	0	0	0-9	0	0
BCD Conv.	0	10	0	0	0	1	0
	0	11	0	0	1	1	0
	0	12	0	0	2	1	0
	0	13	0	0	3	1	0
	0	14	0	0	4	1	0
	0	15	0	0	5	1	0
	0	10	0	1	1	1	0
	0	11	0	1	1	1	0
	0	12	0	1	3	1	0
	0	13	0	1	4	1	0
	0	14	0	1	5	1	0
	0	15	0	1	6	1	0

LOGIC DIAGRAM

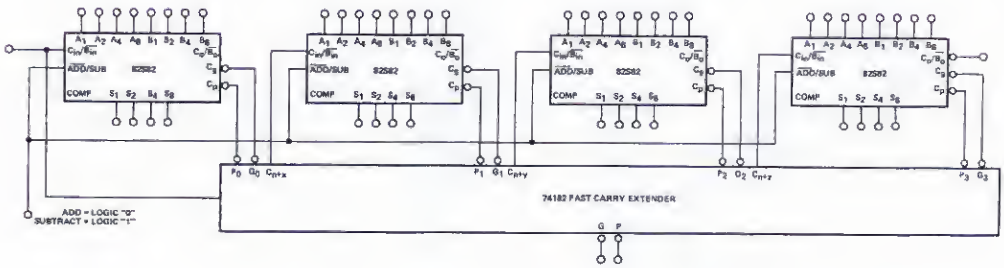


APPLICATIONS

2 DECADE ADDER/SUBTRACTER

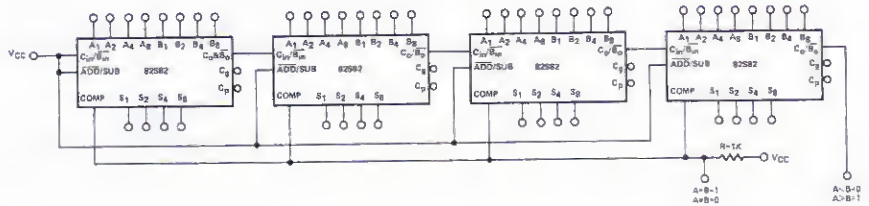


HIGH SPEED BCD ADDITON/SUBTRACTION USING FAST CARRY

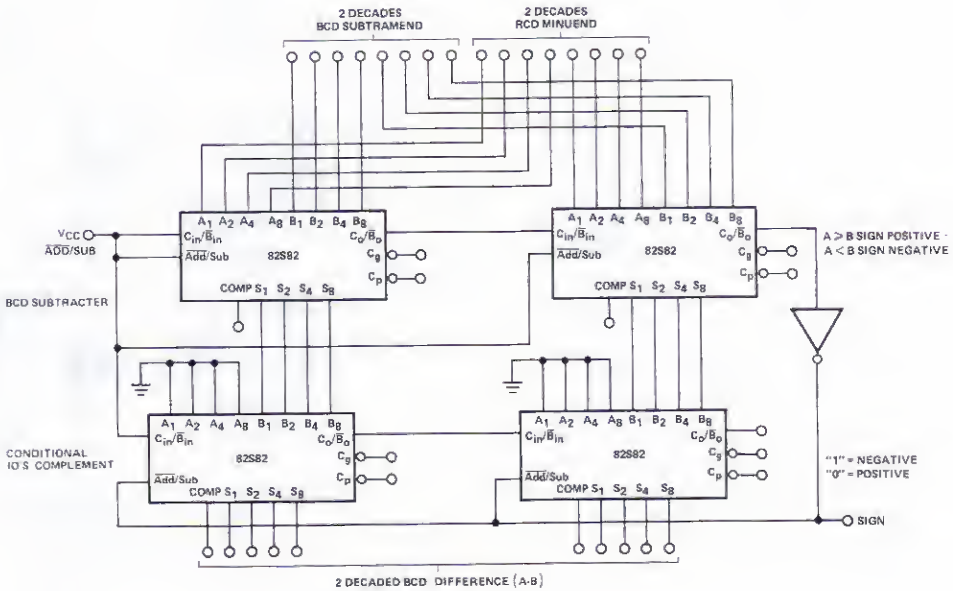


APPLICATIONS (Cont'd)

NUMBER COMPARISON OF BCD DECADES



SIGN AND MAGNITUDE GENERATION FOR A-B



BCD ADDER

DESCRIPTION

The 82S83 4-bit BCD adder is designed to provide the sum of two decimal number represented in the 8-4-2-1 code.

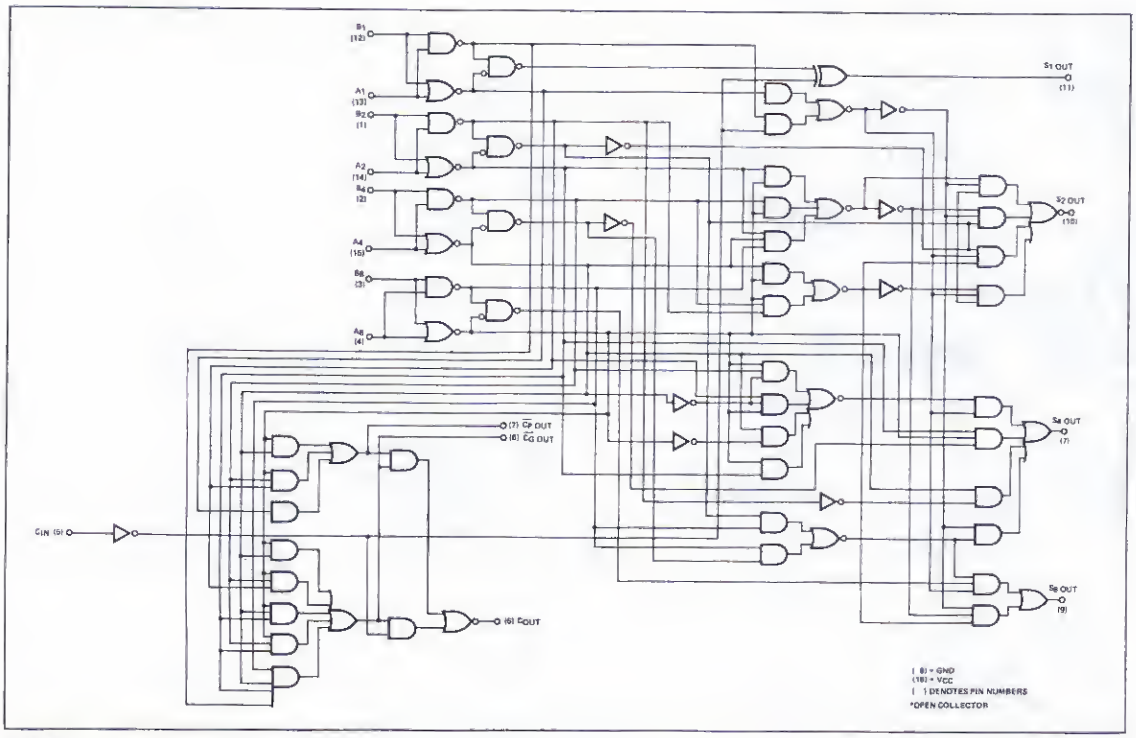
The device includes Carry In and Carry Out pins to allow for device expansion to any required number of decades.

TRUTH TABLE

C_{IN}	A_1 A_2 A_4 A_8	B_1 B_2 B_4 B_8	S_1 S_2 S_4 S_8	C_0
0	0101	0000	0000	1
0	1101	0000	1000	1
0	0011	0000	0100	1
0	1011	0000	1100	1
0	0111	0000	0010	1
0	1111	0000	1010	1
1	0101	0000	1000	1
1	1101	0000	0100	1
1	0011	0000	1100	1
1	1011	0000	0010	1
1	0111	0000	1010	1
1	1111	0000	0110	1

C_{IN}	A_1 A_2 A_4 A_8	B_1 B_2 B_4 B_8	S_1 S_2 S_4 S_8	C_0
0	0000	0101	0000	1
0	0000	1101	1000	1
0	0000	0011	0100	1
0	0000	1011	1100	1
0	0000	0111	0010	1
0	0000	1111	1010	1
1	0000	0101	1000	1
1	0000	1101	0100	1
1	0000	0011	1100	1
1	0000	1011	0010	1
1	0000	0111	1010	1
1	0000	1111	0110	1

LOGIC DIAGRAM



TYPICAL APPLICATIONS

FOUR DECADE BCD ADDER

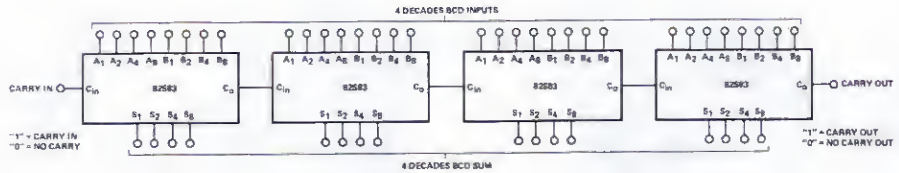


FIGURE 1

BINARY TO BCD CONVERSION

Binary to BCD conversion is obtained by applying any 4-bit binary number to the A_N or B_N inputs while the remaining inputs are grounded. For input codes 0 through 9 a BCD number results at the output as usual. If binary inputs 10 through 15 or 9 plus Carry In are applied, a Carry Out term is generated which, together with the Sum outputs, provides a BCD representation of the binary input. Conversion of binary numbers greater than 16 can be accomplished by cascading 82S83's as shown in Figure 2.

BINARY INPUTS

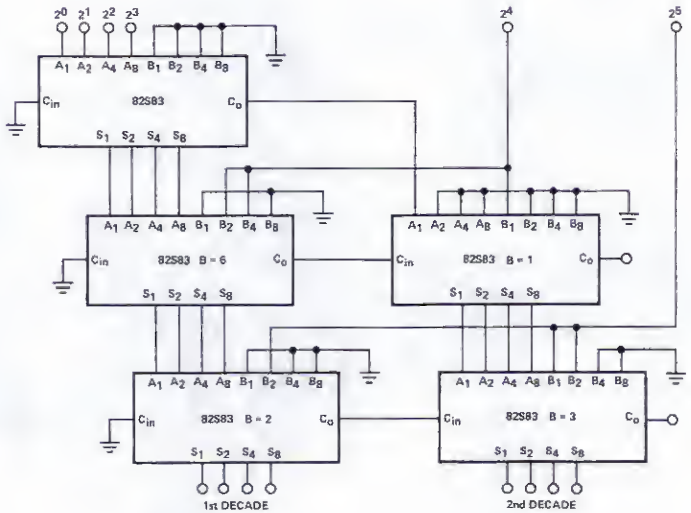
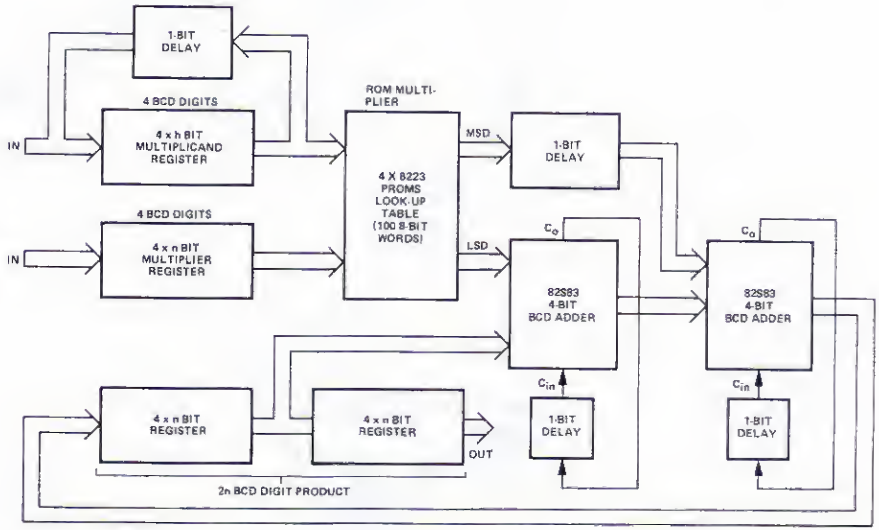


FIGURE 2

82S83 BCD ADDER APPLICATIONS

BIT PARALLEL-WORD SERIAL BCD MULTIPLIER



INTRODUCTION

The Signetics 82S83 BCD Adder and 82S82 BCD Arithmetic Unit provide designers with basic building blocks to implement a variety of BCD computing functions. The devices have been designed to provide substantial reductions in external logic requirements. The use of high speed Schottky technology permits usage in applications where high computation rate is critical.

BCD ARITHMETIC

BCD arithmetic is becoming increasingly important to engineers involved in new product designs. There are at least two trends in progress that are providing the push behind this. First is the increasing application of data computations to business rather than scientific areas. The prevalence of BCD coding in business environments is reflected in everything from Hollerith and ASCII codes to the instruction sets of business computers.

Secondly, remote computing is rapidly evolving from the early time-sharing systems which were basically remote teletypes, to terminals with substantial stand-alone computing capabilities. Examples of these are P.O.S. terminals and automated tellers. Decreased logic costs alone have opened up many new areas to BCD computing including digital instruments, specialized terminals, business machines and peripherals.

A common technique for performing BCD arithmetic is illustrated in Figure 1. The BCD source data is converted into binary numbers through a BCD-to-binary converter. The required computations are then carried out in binary and the results are converted back to BCD through another converter.

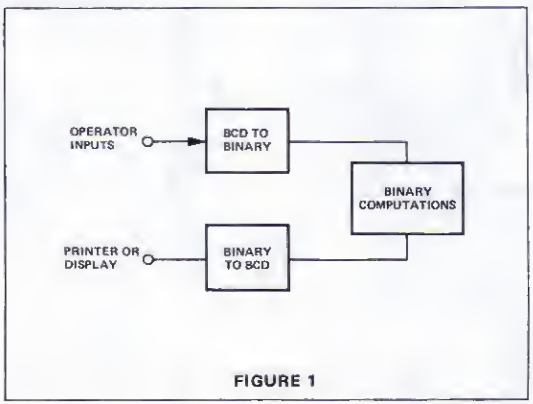


FIGURE 1

This technique is inexpensive if the incremental cost of implementing a BCD computing unit over an equivalent binary unit is greater than the cost of the BCD-to-binary and Binary-to-BCD converters. Performing the BCD computations directly, however, precludes the need for any conversion logic.

SERIAL OR PARALLEL ARITHMETIC

Since BCD numbers are represented as a series of 4 bit digits, there are three ways to perform a BCD addition or subtraction:

1. Bit serial, Digit Serial
   Arithmetic operations are performed on two BCD numbers a bit at a time. The total number of arithmetic operations required is equal to the total number of bits in the longest number. This type of BCD arithmetic unit has the longest execution time and storage for 4 bits is required to generate a carry output.
2. Bit Parallel, Digit Serial
   This type operates on BCD digits rather than bits. This provides an increase of roughly 4 times in operating speed. Since the carry bit can be generated directly from the two 4 bit inputs only a single bit of storage is required to propagate the carry from one operation to the next.
3. Bit Parallel, Digit Parallel
   This is the fastest type of BCD arithmetic since every digit of each number is operated on simultaneously to produce a resultant sum or difference. Carries generated in each decade immediately propagate through to the next decade so that no storage is required.

BIT SERIAL BCD ADDER

A serial BCD adder may be designed using two serial binary adders. The binary adder may be implemented in a number of different ways using gates and a flip-flop. The circuit in Figure 2 shows one possible design.

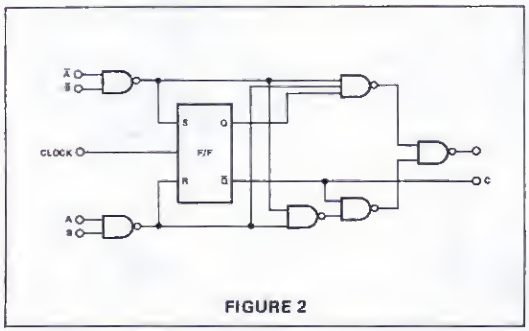


FIGURE 2

The serial BCD addition process consists of an initial binary addition. This is followed by a second addition which adds "6" if the result is greater than "9". The output of the second adder, then, is a number between zero and nine. Figure 3 shows a typical BCD adder design utilizing this technique.

A significant factor affecting the choice of serial or parallel arithmetic is the input and output data requirements. If two digits to be added are presented as bit-parallel numbers, then serialization is required in order to utilize a bit-serial adder. The same thing holds for the output sum where conversion from serial to parallel may be required.

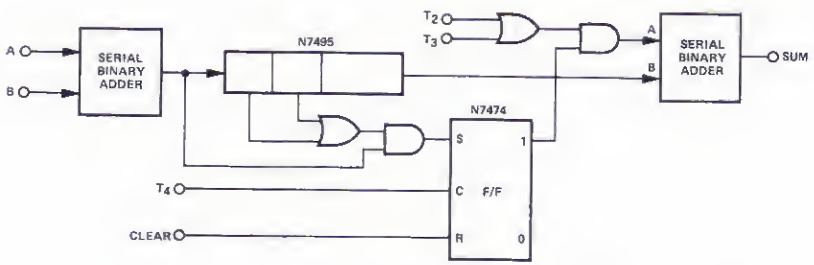


FIGURE 3

BIT PARALLEL, DIGIT SERIAL

Figure 4 shows a BCD adder design using the Signetics 82S83 which operates on two BCD digits at a time. A single flip-flop is required to store the "carry" from each operation.

This design will operate at approximately 4 times the speed of a serial adder and provides a reduction in parts count. For those cases where input data storage is not required, such as lines from thumbwheel switches, multiplexers may be used to sequentially steer digits into the adder. This technique is shown in Figure 5.

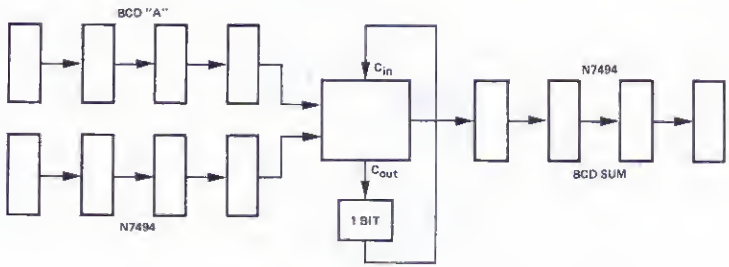


FIGURE 4

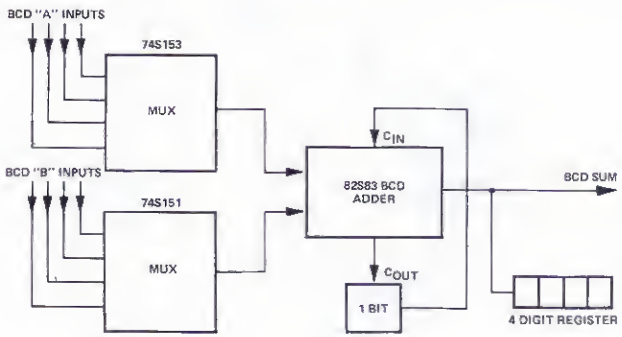


FIGURE 5

PARALLEL ADDITION

The fastest way to add two BCD numbers is by parallel addition where the entire sum is obtained in a single operation. Four-bit binary adders such as the 8620 or 7483 may be used to implement a BCD adder using the binary sum with BCD correction technique. Figure 6 shows a logic implementation of this technique using two 7483 adders per decade.

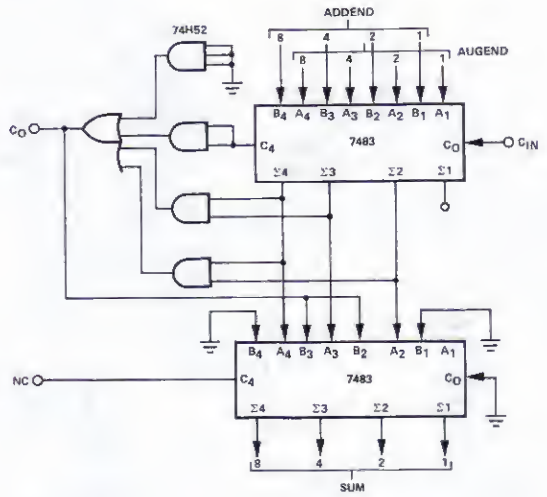


FIGURE 6

Another approach is to use a ROM look-up table for each decade as shown in Figure 7. Each ROM contains 200 5-bit words. Four bits provide the BCD output sum and the fifth bit provides a "carry" output. Nine inputs are required for the ROM to accommodate 2 4-bit digits and a "carry" input.

A third alternative is shown in Figure 8 where the 82S83 BCD Adder is used in place of ROMs. This provides a faster adder configuration at a cost substantially less than large ROMs. Regardless of which technique is used to provide parallel arithmetic, the cost of implementing the logic is directly related to the size of the numbers to be operated upon.

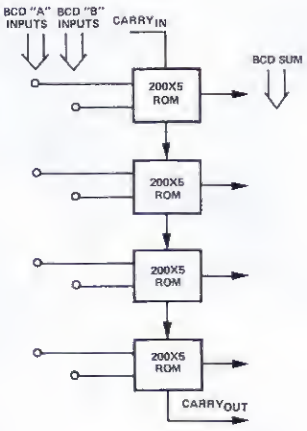


FIGURE 7

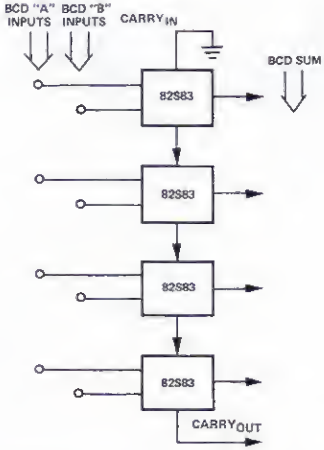


FIGURE 8

Bipolar ROMs and 4 bit BCD arithmetic units can be used as basic building blocks in implementing more complex functions such as multipliers, dividers, square root and function generators. An example of this is the high speed BCD multiplier shown in Figure 9. This design performs a multiplication by the entire multiplicand on successive multiplier digits. The partial product is stored in the series of 4 bit output registers and is shifted to the right, a digit at a time, once for each multiplier digit. Using an 82S82 with a 74S182 look-ahead carry generator, a 4 digit by 4 digit product can be obtained in under 200 n.sec.

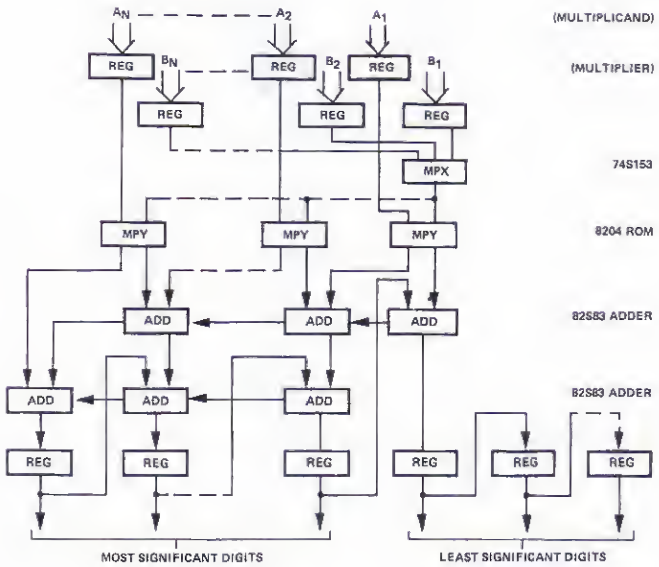


FIGURE 9

signetics

BIPOLAR
MEMORY
APPLICATIONS

4

BIPOLAR MEMORIES

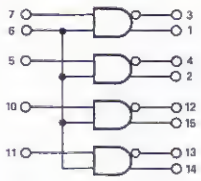
INTRODUCTION

The 10124 QUAD TTL to ECL LEVEL TRANSLATOR/LINE DRIVER and the 10125 QUAD ECL to TTL LEVEL TRANSLATOR/LINE RECEIVER have been designed for easy and economical implementation of interfaces such as:

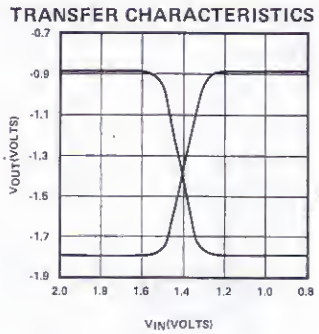
TTL/DTL to ECL LEVEL TRANSLATION
ECL to TTL/DTL LEVEL TRANSLATION
TTL to TTL DIFFERENTIAL DATA TRANSMISSION

The 10124 has TTL compatible inputs and complementary open emitter outputs identical to those of a standard ECL 10,000 gate. A strobe input is common to all four translating gates to permit easy control of data flow. In addition, all inputs are diode clamped to protect against negative ringing. Thus, the 10124 may be used as an inverting/non-inverting translator or as a differential line driver for twisted pair or ribbon cable. Each output is capable of driving 50 ohm and various transmission line terminations are discussed in the appendix. The logic diagram is shown in Fig. 1a and the transfer curve in Fig. 1b illustrates typical input/output behavior of the TTL to ECL translator.

10124 QUAD TTL TO ECL TRANSLATOR



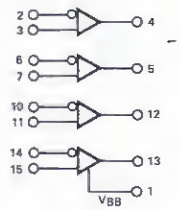
a.



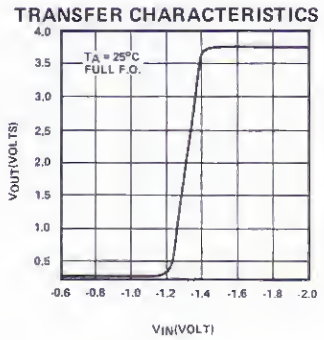
b.

FIGURE 1

10125 QUAD ECL TO TTL TRANSLATOR (TOTEM-POLE OUTPUTS)



a.



b.

FIGURE 2

For ECL to TTL translation, the 10125 interface has complementary differential inputs and Schottky TTL outputs. As shown in the logic diagram, Fig. 2a, the device may be used as an inverting/non-inverting translator or as a differential line receiver. Input pulldown resistors that are standard with other ECL 10,000 circuits are not needed in the 10125. In single-ended applications, the unused input should be referenced to $-V_{BB}$, available on pin 1, for proper logic operation. But even if both inputs are left open, as well as during power supply turn-on, the 10125 is internally protected by a fail-safe circuit that puts the outputs in the logic "0" state.

Differential signals as low as 200mV at the inputs of the 10125 result in defined TTL output levels. A typical transfer curve is shown in Fig. 2b. Outputs are Schottky TTL "totem poles" that can fan out to 10 TTL loads. In addition, the 10125 has a $\pm$1V common mode range when used differentially. This makes the device extremely attractive in data transmission applications where cross-talk or ground shifts are expected.

TTL/DTL to ECL LEVEL TRANSLATION

Figure 3a shows how TTL logic can be easily interfaced with high speed ECL 10,000 logic. Performing the TTL to ECL level translation on the TTL logic board with the 10124 is advantageous since it keeps noise out of the ECL system. By using differential data transmission, crosstalk will most likely appear as common mode noise on the twisted pair line driving the 10115 ECL line receiver.

The differential inputs do not respond to common mode voltage, V_{CM}, as long as it does not exceed the common mode range of the 10115 receiver, which is typically between +0.8V and −2.0V. (Note that a V_{CM} range of ±1V is guaranteed on the 10114 line receiver to be announced.)

Since the 10115 has voltage gain of about 6, differential input signals with at least 160mV amplitude will still result in defined ECL 10,000 output levels. Therefore, data transmission over long lines where signal attenuation is expected presents no problem.

As an example, performance of the 10124 driving 50 feet of twisted pair line into a 10115 line receiver is shown in Fig. 3b. Although the system may operate in the vicinity of 100MHz, only a 50 MHz data rate has been chosen to show that the system is properly terminated. Advantage has been taken of the 50 ohm drive capability of the 10124, which results in terminating the twisted pair with its characteristic impedance of approximately 100 ohms. Other termination schemes are shown in the appendix.

ECL to TTL LEVEL TRANSMISSION

When driving TTL from an ECL 10,000 source, the 10125 can be used as a differential line receiver that translates the signal levels on the TTL board which also has the advantage of isolating potential TTL noise from the ECL system. For short interconnects, such as those found on the same board, the interface between ECL and the 10125 receiver/level translator may be single ended. In that case, the unused inputs must be referenced to the bias voltage, V_{BB}, which is at the midpoint of the logic swing. For convenience V_{BB} is available on pin 1 of the 10125.

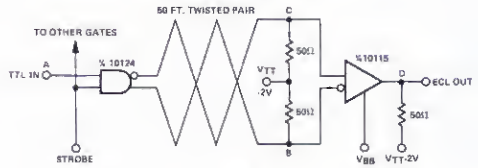
Long lines are best driven differentially as shown in Fig. 4a since it makes them less susceptible to induced noise or level shifts due to supply variations or temperature gradients. As mentioned earlier, most of the noise will appear as a common mode signal that is eliminated when using differential transmission as long as the 10125's common mode range of ±1V is not exceeded.

Because of a typical voltage gain of 8 in the input stage of the 10125, signals as low as 200mV are sufficient to guarantee TTL output levels. This fact is particularly beneficial when attenuation due to long lines or high frequency operation has to be overcome.

Figure 4 shows performance of the 10101-10125 system at 50MHz. Typically this configuration is capable of 100MHz operation. Again, advantage has been taken of the 50 ohm drive capability of the ECL 10,000 series in achieving the proper termination, but other termination possibilities are discussed later.

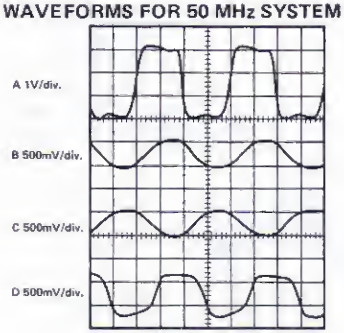
TTL TO ECL INTERFACE

10124 DRIVING 50 FT. TWISTED PAIR



a.

WAVEFORMS FOR 50 MHz SYSTEM

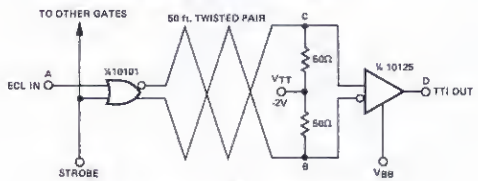


b.

FIGURE 3

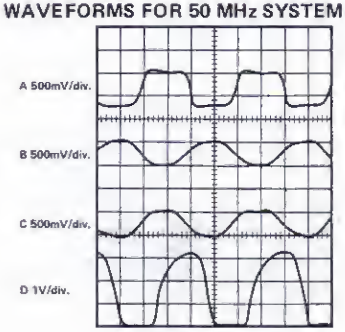
ECL TO TTL INTERFACE

10125 RECEIVING ECL SIGNAL OVER 50 FT. TWISTED PAIR



a.

WAVEFORMS FOR 50 MHz SYSTEM



b.

FIGURE 4

DIFFERENTIAL LINE DRIVER AND RECEIVER FOR TTL SYSTEMS

In TTL designs it is often desirable to drive long lines at high speed and low cost. The 10124 and 10125 can be used in an all TTL system to perform differential data transmission over twisted pair lines. Instead of conventional dual drivers and dual receivers the 10124/10125 combination only requires two IC's for four data channels.

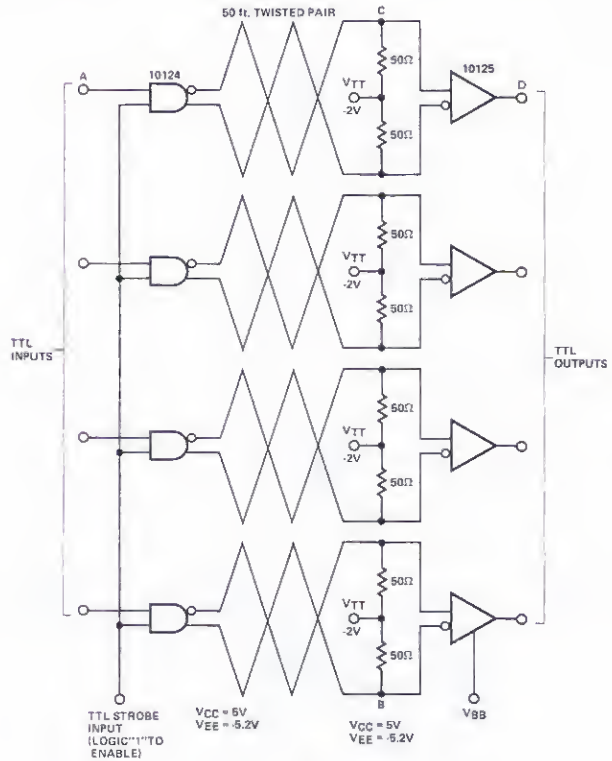
The system shown in Fig. 5a can be used with data rates up to 100MHz. Twisted pair lines driven differentially provide maximum noise immunity for noise that is coupled into the system appears on both wires equally (i.e., common mode).

The receiver senses only differential voltage between the lines as long as the common mode range of ±1V is not exceeded. It was previously discussed that the 10125 input signal may be attenuated to 200mV which still results in guaranteed TTL output levels. Thus from d.c. considerations twisted pair in excess of 1 mile may be driven which makes signal attenuation at high frequencies the limiting factor.

Performance data for a 10124 driving 50 feet of twisted pair at 50MHz and a 10125 line receiver is shown in Fig. 5b. Other terminations schemes are possible and discussed below.

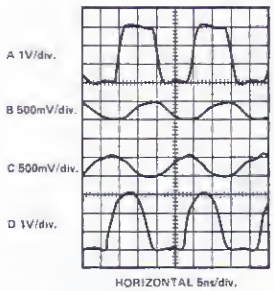
DIFFERENTIAL DATA TRANSMISSION IN TTL SYSTEMS

DATA TRANSFER OVER 50 FT. TWISTED PAIR



a.

WAVEFORMS FOR 50 MHz SYSTEM



b.

FIGURE 5

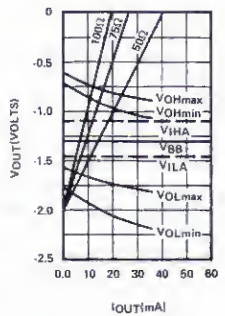
APPENDIX: TERMINATIONS FOR DIFFERENTIAL TRANSMISSION LINES

If transmission lines exceed approximately 6 inches they must be terminated in ECL 10,000 systems. The uncommitted emitter follower outputs of the ECL 10,000 series may be used with a variety of pulldown resistors depending on the available terminating voltage. The resistor values must be kept between the limits indicated in Figures 6a and 6b such that guaranteed noise margins are kept and output current capability is not exceeded.

If V_{TT} (−2V) is available, pulldown resistors as low as 50 ohms may be used. Thus, as shown in Fig. 7a, each end of the twisted pair is terminated to V_{TT} with $Z_O/2$ (50Ω) resulting in a net termination of Z_O, the lines characteristic impedance. This method of termination is most attractive since it results in minimum systems power dissipation.

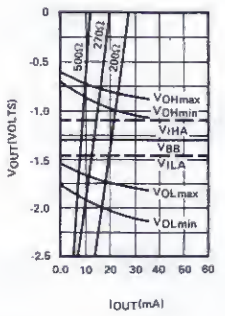
OUTPUT RESISTOR LOAD LINES FOR 10124

LOAD LINES FOR TERMINATIONS TO V_{TT}(2.0V)



a.

LOAD LINES FOR TERMINATIONS TO V_{EE}(-5.2V)



b.

FIGURE 6

Furthermore, the full output swing is available at the end of the transmission line except for line attenuation.

When V_{TT} is not available, recommended pulldown resistors to V_{EE} (−5.2V) may range from 200 ohms to 500 ohms. However, the end of the transmission line must still be terminated in its characteristic impedance Z_O. Fig. 7b shows the DC equivalent circuit for differential transmission lines using this method.

The voltage at the end of the transmission line depends on the voltage divider relationship between the pulldown resistor R_L and the terminating resistor R_{TERM}. Assuming that one of the complementary outputs in Fig. 7b is high while the other is low, the voltage developed across the termination is equal to:

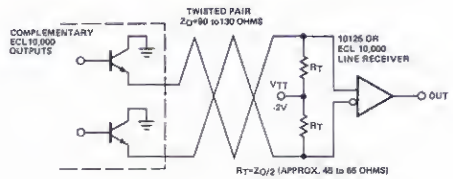
$$V_{TERM} = \frac{(V_{EE} - V_{OH})\, R_{TERM}}{R_L + R_{TERM}}$$

where: $V_{OH} = 0.9V$

For R_{TERM} = 100 ohms and R_L = 510 ohms, the differential voltage, V_{TERM}, at the input of the 10125 receiver is equal to 710mV. Notice that use of smaller pulldown resistors, R_L, in the above equation only allows the voltage, V_{TERM}, to become as large as 800mV and then the output in the low state will clamp at the low output voltage, V_{OL}.

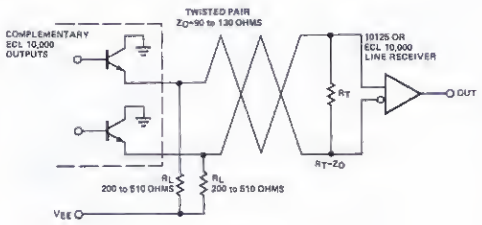
TERMINATION FOR DIFFERENTIAL DATA TRANSMISSION

IF ONLY V_{TT}(-2.0V) IS AVAILABLE



a.

IF ONLY V_{EE}(-5.2V) IS AVAILABLE



b.

FIGURE 7

signetics

ECL
APPLICATIONS

5

TTL TO ECL TRANSLATORS

256 BIT BIPOLAR RANDOM ACCESS STORAGE APPLICATIONS

INTRODUCTION

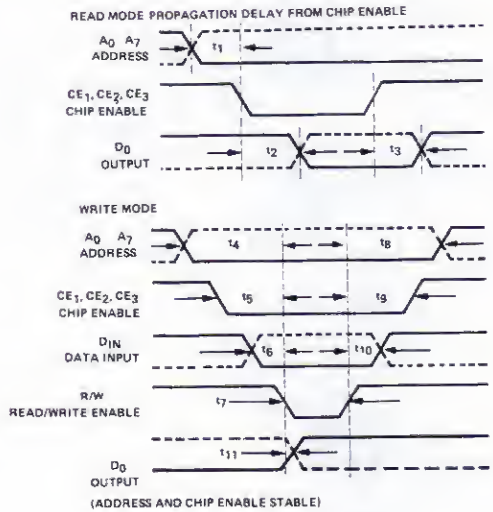
Bipolar memories are finding increasing use in computer systems, peripherals, terminals and many other digital devices. The purpose of this application note is to provide the logic designer with some memory configurations, suggest some current system applications and provide the designer with additional references on system applications.

MEMORY CONFIGURATIONS

The Signetics 82S06 and 82S07 are 256 bit bipolar devices and are easy to use. Their outstanding features are:

1. T^2L compatible inputs and outputs – interface directly with other members of 8000 and 54/7400 logic families.
2. High Speed – 30nSec typical read and write access time.
3. Low Power Dissipation – 1.8 mW/bit typically.
4. Low Input Loading – $-100\mu A$ for a "0" input allowing a single high speed TTL gate to drive many 256 bit RAMs.
5. Or-tie outputs with either tri-state (82S06) or open collector (82S07) for easy memory capacity expansion.
6. Three chip enables for easy memory word expansion.
7. Full binary on-chip decoding.
8. 256X1 organization.

TIMING DIAGRAM



MEMORY TIMING DESCRIPTION

t_1 = set up time for an address input to chip enable for valid data at output
t_2 = propagation delay from chip enable to valid data at output
t_3 = propagation delay from chip disable to output turn off
t_4 = set up time from address to write enable
t_5 = set up time from chip enable to write enable
t_6 = set up time from data input to write enable
t_7 = write enable pulse width
t_8 = hold time for address from write enable
t_9 = hold time for chip enable from write enable
t_{10} = hold time for data input from write enable
t_{11} = propagation delay from write enable to valid data at output

256X8 BIT MEMORY

Figure 1 shows the Signetics 256 bit RAM in a 256X8 configuration.

16394X1 BIT MEMORY

Figure 2 shows the basic configuration for a 16K X 1 memory. This illustrates the advantages of the multiple chip enable, low input loading and the or-tie outputs. Two Signetics 82S50 binary-to-octal decoders can be used with two of the chip enables to select any one of 64 RAM chips. Each octal output drives only 8 chip enables.

When building a memory of this size, the data output must drive 63 RAM outputs and the inputs of the other gates. One criteria for selecting either the open collector or tri-state output structure is the trade off between active pullup drive capability and the accurate chip enable timing control required, and the passive pullup with no such timing restrictions but less capacitive drive. When using the tri-state output (82S06) care should be exercised in controlling the X chip select ($\overline{CE}_1$) and Y chip select ($\overline{CE}_2$) to ensure only one RAM is selected at a time. This can be done by disabling all the RAMs by taking $\overline{CE}_3$ to the "1" level during address decoding.

If, during the selection time, two 82S06s are selected at the same time and one has a "1" level output while the other has a "0" level output, then a short circuit from V_{CC} to ground is created. Proper timing control eliminates this condition. During the chip selection time, momentary shorting of the outputs will not damage the circuit. Additional decoupling capacitance between V_{CC} and ground should be used to supply the added current required. The active pull-up output of the 82S06 can drive heavy capacitive loads with fast rise and fall times.

The open collector 82S07presents no such timing restrictions. If two RAMs are selected at one time with one at a "1" and the other at a "0" the output current is limited by the pullup resistor used. However, this passive pullup may have a slower rise time than the active pullup 82S06.

The 82S06 tri-state RAM sinks 16mA in the "0" state and sources −5mA in the "1" state. In the "off" state the RAM presents a high impedance output with leakage current less than −100μA. To drive 63 such outputs in the "1" state requires 63X100μA = 6300μA. If a standard TTL logic family is used with a maximum "1" input current of 40μA and if a fan out of 2 is desired the source current must be

$$I_{source} = 2x40 + 63x100 = 6380\mu A$$

Since the 82S06 will supply −5mA in the "1" state a pullup resistor to V_{CC} is required which will supply

$$I_R = 6380\mu A - 5000\mu A = 1380\mu A$$

Since the minimum "1" level output voltage is 2.6 volts the following resistor will supply the necessary current.

$$R = \frac{(5.0 - 2.6)V}{1380\mu A} \cong 1.7K \text{ ohm}$$

(a standard 1.6K ohm resistor will supply the required current)

256 x 8 BIT RANDOM ACCESS MEMORY USING 256 x 1 RAMS

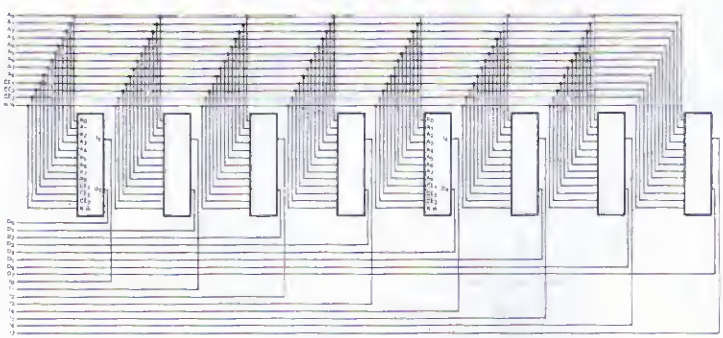


FIGURE 1

If the output is in the "0" state the driving circuit must sink the leakage of 63 RAMs in the "off" state, the current drawn from V_{CC} through the pullup resistor and the "0" input current for the two TTL loads, which are −1.6mA each. The maximum sink current required is then

$$I_{sink} = (2x1.6mA) + (63x100\mu A) + \frac{5.0 - .45V}{1.6K} = 12.3mA$$

The 82S07 open collector RAM will sink 16mA in the "0" state. In the "1" state, or with the chip disabled, the output leavage is less than 100μA. Driving the same load as above, the current and pullup requirements are

$$I_{source} = (2x40\mu A) + (63x100\mu A) = 6380\mu A$$

$$R = \frac{5.0 - 2.4V}{6380\mu A} \cong 407 \text{ ohm}$$ (a standard 390 resistor will supply the required current)

$$I_{sink} = (2x1.6mA) + \frac{5.0 - .45}{390} \cong 15mA$$

The input circuits of both these Signetics 256 bit bipolar RAMs are buffered with PNP emitter followers. Input PNPs have an F_t of about 100MHz and a beta in the range of 100. This minimizes the problems of driving input circuits. The maximum input currents for these RAMs are −100μA in the "0" state. A single Signetics N74S00N Quad 2 Input Nand Gate is capable of sinking 20mA in the "0" state and can easily drive the 64 Signetics 82S06 or 82S07 RAM inputs. The peak AC switching current may be greater than the DC current required and some care must still be taken to ensure enough input drive is provided to sink the worst case currents and discharge worst case input capacitance which may be as high as 8pf per input. For this example only 64X100μA = 6.4mA of DC current must be handled by the driver leaving approximately 10mA of "0" level current available to achieve fast input rise and fall times.

HIGH SPEED 2048 WORD MEMORY

The previous example showed the Signetics 256 bit bipolar RAM in a 16K x 1 memory array. This array uses two of the chip enables and two 82S50 for decoders. To provide a 2K word memory the use of all three chip enable lines allows a design requiring only high speed inverters, each as the Signetics N74S04N, as the decoder.

SYSTEM APPLICATIONS

Bipolar memories are currently being employed or will soon be used in:

a. Writeable control storage
b. Cache memories or buffer stores
c. Main memory
d. Memory protection schemes
e. Memory maps and virtual memories

The advent of relatively low cost high speed storage is having a dramatic impact on the architecture and design of current systems.

WRITEABLE CONTROL STORAGE

In microprogrammed devices it is possible to replace ROM (Read Only Memories)with read/write memories. Several important advantages result from using bipolar RAMs in the control section of a device. These are:

1. Programming errors in the control portion of a machine can easily be corrected in the field by issuing new control programs.
2. Control programs used infrequently such as emulators, diagnostics, special instructions which do not have to be simultaneously resident in control memory can be stored on disc, paper tape, or remotely and can be read in when needed.
3. Design times can be considerably shortened because no special purpose masks are required.

SYSTEM DIAGNOSTICS

Several computers put portions of their diagnostic routines into control memory. Examples of this are the Micro 810 and some of the larger models of the IBM System/360[1]. The advantage to putting diagnostics in the control memory is that small individual portions of the system can be exercised and checked. This means that faults can be pinpointed more precisely. Also, the starting diagnostics can be run with a smaller portion of the machine operating. Unfortunately,

16K x 1 BIT MEMORY USING 82S06 OR 82S07

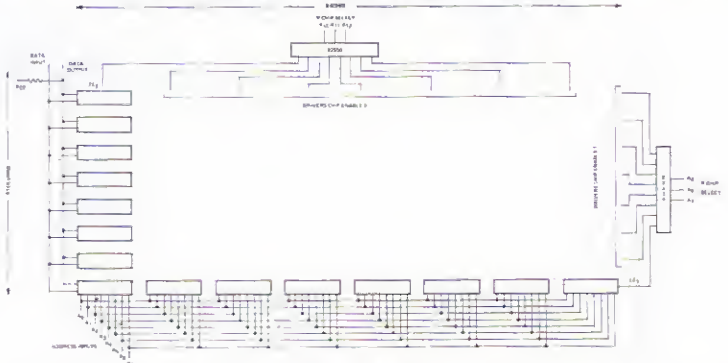


FIGURE 2

[1]W. C. Carter, H. C. Montgomery, R. J. Preiss and H. J. Reinkeimer, "Design of Serviceability Features for the IBM System/360," IBM Journal of Research & Development, Vol. 8, No. 2, April 1964, Pg. 115

[2]Neil Bartow and Robert McGuire, "System/360 Model 85 Microdiagnostics," AFIPS Conference Proceedings, Vol. 36, 1970, Pg. 191

[3]C. V. Ramamoorthy and M. Tsuchiya, "A Study of User - Microprogrammable Computers," AFIPS Conference Proceedings, Vol. 36, 1970, Pg. 165

because of the many words required to store the diagnostics, it is too expensive to put all of the diagnostics in read only memory. By making a portion of the control memory from read/write memory, this problem can be eliminated. Diagnostics can be stored off-line and read into the control memory under the control of a small read only memory and then executed. In one system the diagnostics used in this fashion contain 30 individual sections which can be loaded into the writeable control store.[2]

SPECIAL INSTRUCTION SETS

The instruction set of a machine can be easily tailored to the application or environment with writeable control store.[3] Typical applications for this are:

1. Emulators may be executed from the control storage.
2. Macros which reduce execution time for executive and production programs may be executed from the store.

Probably the major user benefits will result from putting certain high overhead functions that must be executed by executive programs into writeable control store.

PERIPHERAL AND TERMINAL APPLICATIONS

The application of writeable control stores in peripherals and terminals will also prove to be important. This is especially true in the case of terminals which usually do not have the ability to run diagnostic routines. With a small writeable control store, these routines can be stored remotely and transmitted to the device or read in from paper tape, cassettes, etc. They could then be executed. This type of application could have a significant effect on reducing maintenance costs because some terminal failures could be diagnosed remotely and separated from operator mistakes.

By incorporating different control programs into a terminal control storage, the characteristics of a terminal can be easily adapted to a job. For example, different format or control procedures could be established depending on the application.

MAIN MEMORY APPLICATIONS

Numerous computer manufacturers are considering the use of semiconductor main memory to replace core storage. IBM has announced the use of bipolar main storage in the 370/145. Prior to this event, IBM had been using bipolar memory in "cache" or buffer stores. Recent events point clearly toward a trend to replace a significant amount of core storage with bipolar and MOS RAM. The purpose of this segment of this note is to suggest how relatively small amounts of bipolar RAM can be used in support of large memory systems and to suggest its effects on systems currently in use.

BUFFER STORES (CACHE TYPE)

A buffer store used and implemented properly in a computer system can greatly enhance the effective performance of a system. With proper implementation, the main memory can be made to appear as if it has a speed approaching that of the buffer memory. For example, if the buffer memory is ten times faster than the main memory, then effective access times on the order of eight to nine times the speed of main memory can be achieved. The reason buffer stores can be so effective is primarily because the data or instructions being currently executed have a very high probability of being used again in the near future. This is often referred to as the "look behind" phenomena.

In the case of the IBM 370, it is claimed that up to 95% of storage accesses can be from the buffer store which has 80 ns cycle time as opposed to the cycle time of main core which is in the 1.2 to 2.0 μs range.

The effective access time for a 2.0 μs core in this case can be as high as

Effective Access Time $= 0.05 \times 2.0\ \mu s + .95 \times 0.080\ \mu s = .176\ \mu s$

The great advantage of this approach is that high performance memory can be achieved with low performance and low cost storage. In general, the size of main store is from 2^6 to 2^8 times larger than the buffer storage and therefore, if the cost per bit of buffer storage is a factor of 16 greater than the cost of main store, the actual storage cost is increased by a factor of

$$1 + \frac{16}{2^6} \geq \text{cost factor} \geq 1 + \frac{16}{2^8}$$

$$1.25 \geq \text{cost factor} \geq 1.0625$$

Therefore, memories with effective cycle times of less than 200 ns can be achieved with buffer stores and 2 microsecond main store in an economical fashion at cost per bit approaching the cost of 2 microsecond core storage. There are numerous ways in which buffer stores can be implemented and increasing evidence that the use of even small amounts of this type of storage can add tremendously to system performance. Because semiconductor memory in the 60 ns range is becoming so inexpensive, it is highly probable that many of the high performance small mini-computers will begin using it to increase their system performance. Some of the current approaches are:

1. Associative by Page-Address by Word. In this technique the buffer store and main store are divided into sectors consisting of, for example 1K bytes. A correspondence is then set up between the buffer store and the main store (see Figure 3). Because of the small size of the buffer store, most main store does not have a buffer sector assigned to it and consequently, an associative search must be performed on the sector addresses to see if the sector is present. This can be easily implemented using the Signetics 8220 Content Addressable Memory (CAM).

   When a program references data in main storage, not present in the buffer store, a section of the buffer store sector is reassigned. The sector chosen for reassignment is the one with the lowest current level of activity.

   When a buffer sector is assigned to a different main storage sector, the contents of all of the buffer storage sector are not loaded at once but only on a demand basis. In order to keep track of which words in the sector have been reloaded, validity bits are assigned to blocks of data. All of these bits are reset when the sector is reassigned and set on an individual basis when data is brought from memory into the buffer.

   Any store operation will cause main storage to be updated and therefore, it is never necessary to write the data in the buffer store back into main memory.[4]

[4] J. S. Liptay, "Structural Aspects of the System/360 Model 85 II The Cache," IBM Systems Journal, Vol 7, No. 1, 1968, Pg. 15

2. Associative by Word Buffer Store. In this configuration each word in buffer store has assiciated with it its main core address which is stored in a corresponding word of content addressable memory. The buffer store is first searched to determine if the desired word is resident and if it is, it is read out; if not, the word is retrieved from main memory (Figure 4). An algorithm must be developed for deciding which word to remove when new words are loaded in the buffer store. Algorithms of this type are easily implemented with Signetics 8220 CAMs and other 8200 series MSI devices. In general, this is done by flagging words in the store that have not been referenced frequently. The performance of this type of system has been thoroughly studied.[5]

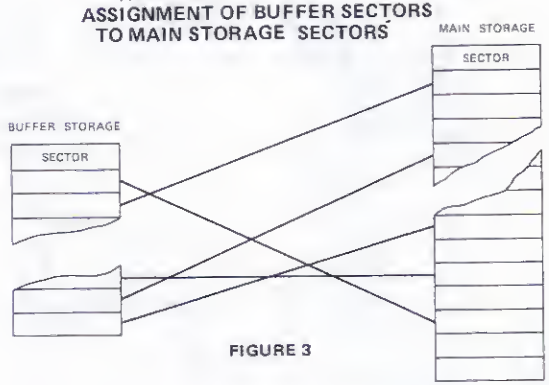


FIGURE 3

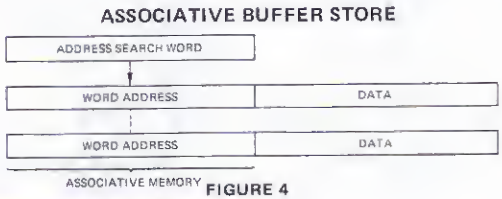


FIGURE 4

PORTIONS OF MAIN MEMORY

In small computers main memory is frequently used for storing I/O control words and in some of the earlier machines, program counters, index registers and accumulators were stored in core. Trends in recent years have been away from this type of organization; however, the availability of low cost semiconductor memory used as the first 256 or more words of main storage may cause this trend to be reversed. Significaant performance increases and very sophisticated computer organizations can be achieved by using semiconductor memory in this manner.

Some of the items that might be put into this type of memory are:

1. General registers
2. Floating point registers
3. Program counters
4. Status words
5. Index registers
6. Stack pointers
7. Direct memory access word count and word address registers
8 Subroutines with critical execution times

Undoubtedly there are many more. New architectures will begin to emerge over the next few years because fast access registers will be readily available and their copious use will have only a minor influence on system cost.

MEMORY PROTECTION

Memory protect features are being incorporated into even the smallest real-time systems. Small bipolar memories are especially adapted to this application. One of the simplest protect schemes is to assign a single protect bit to a block of memory. For example, in a minicomputer with a maximum storage of 65K words, the assignment of a protect bit to each 256 word block requires only 256 bits of bipolar storage. This type of protect scheme, though simple, can provide adequate protection in small real-time systems where the only concern is to inhibit users from writing over the executive or other users program.

More sophisticated schemes such as those employed in the Sigma 7 can also be easily implemented with bipolar RAMs.[6] In the Sigma 7 system two bits are associated with each 512 word page. (See Figure 5). These bits are interrogated before a slave program (a program run under the control of the executive) gains access to a page. The four states associated with this system are used to designate the following conditions:

1. Permit slave access to page for any reason.
2. Inhibit slave access for writing but permit reading.
3. Inhibit slave access for writing and instruction execution but permit operand read access.
4. Inhibit slave access for any reason.

Many other coding and variations of this scheme can be envisioned. The important aspect is that bipolar storage for this application is available at low cost in compact packages.

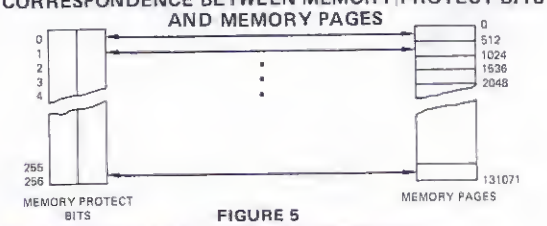


FIGURE 5

MEMORY MAPS AND VIRTUAL MEMORIES

The first major application of memory maps and demand paging were in the Atlas Computer developed at Manchester University.[7] In recent years these techniques have been applied in many modern computer systems. The advent of low cost bipolar storage will make it possible to use memory maps in very small computer systems.

The basic reason for using memory maps and virtual memory techniques is to make the management of memory resources easier for the system executive and user. By using these techniques, the user can work on a virtual machine which has apparent primary memory resources that are much larger than

[5]P. M. Melliar-Smith,"A Design For a Fast Computer for Scientific Calculations," AFIPS, Conference Proceedings, Vol. 35, 1969, Pg. 201

[6]Myron J. Mendelson and A. W. England, "The SDS Sigma 7 A Real-Time Time Sharing Computer," AFIPS Conference Proceedings, Vol. 29, 1966, Pg. 51

[7]T. Kilburn, D. B. G. Edwards, M. J. Lanigan, F. H. Sumner, "One-Level Storage System, "IRE Transactions on Electronic Computers, Vol. EC-11, No. 2, April 1962, Pg. 223

the actual memory. The second problem solved by using memory maps is that contiguous program segments can be loaded into core but need not be placed in contiguous memory location. With memory maps, the dynamic relocation of program segments becomes a simple task. With the advent of low cost bipolar semiconductor memories, it is easy to visualize 256 x 8 memories in small real time computers implementing this function.

A system which uses memory maps may place only portions of programs in main memory at any point in time. These program segments are located somewhat randomly. The job of the memory map is to identify which portions are in main memory and where they are located. In the Sigma 7, the seventeen bit address field is broken down into an 8 bit page address and a 9 bit word address.[6] The 8 bit page address is used to address one word of a 256 x 8 bit semiconductor memory. This addressed byte contains the real address of the page in memory and is used to access the data. (See Figure 6.) If the desired program segment is not in memory, the instruction is trapped so the program segment can be loaded into the system. Special instructions are provided so that the memory map can be loaded with a single instruction.

In other systems the memory map is augmented with protect bits so that memory protection can be accomplished in the same structure. One can also associate a "dirty" bit with each word in the memory map. This bit is set to "zero" when data is read into memory and will be set to "one" if the page of data or instructions is altered while it is in memory. If no alterations of the page takes place, it becomes unnecessary to write this page out in the second level of storage when bringing new data into memory in that location. Since many of the newer system and software designs do not alter program addresses, etc., the storage devoted to program will remain intact while in the system. This situation will, therefore, occur frequently.

SIGMA 7 TYPE MEMORY MAP

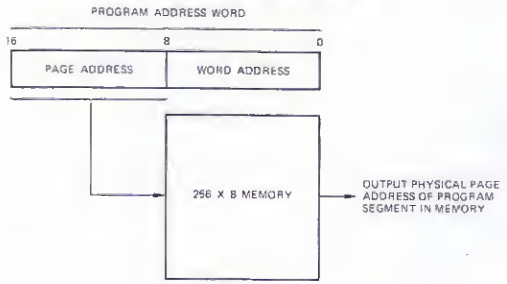


FIGURE 6

Associative implementations of memory maps have also been employed. While these are more costly to implement, they offer performance advantages. The basic structure is to have the associative memory store the page address and a program identification number. The memory can then be searched to find out if the program segment of the desired program is resident. By storing the program identification with the program address, the content of the memory map need only be altered when new segments are loaded into core and not when the computer switches from program to program (See Figure 7).

ASSOCIATIVE MEMORY MAP

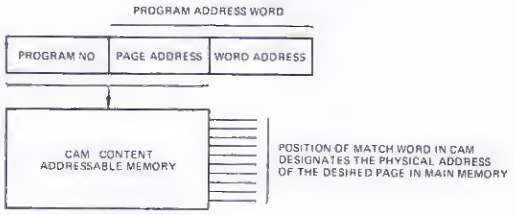


FIGURE 7

OTHER COMPUTER MAINFRAME APPLICATIONS

The new organization of computer systems creates many opportunities for the imaginative application of bipolar RAMs. Two of the most obvious are:

1. Register blocks
2. Working stacks

When a computer switches program environments, it is often convenient to switch to an entirely different set of registers. This means the computer does not have to incur the overhead of storing general registers and status words. Two examples of the use of this technique are the Varian 520i and the Sigma 7.

The 520i has two sets of registers whereas in the Sigma 7 there are up to 32 register blocks each containing 16 thirty-two bit registers. On the Sigma 7 when an interrupt occurs, the 5 bit register pointer can be changed to assign a new set of general registers and the machine. This 5 bit pointer is stored as part of the program status word.

Working stacks have been incorporated into numerous machines such as the Burroughs B-5000 series and the English Electric KDF9. In a stack oriented machine which processes operands from a stack, it is desirable to have fast access to these variables. In the early stack oriented machines only the first few stack registers were fast access. Now with the advent of bipolar semiconductor memory, most reasonable sized stacks can be implemented inexpensively in fast storage.

CONCLUSION

Probably all of the techniques discussed in this application note are familiar to the experienced system designer. Because of the variety of uses to which semiconductor memories can be put, it is impossible to mention all but a few. The important point this application note is attempting to make is that a new dimension of flexibility has been given to the system designer. Two-hundred-and-fifty-six 30 ns bits are now available in small 16 pin DIP packages, at one-tenth the cost of a few years ago. The two order of magnitude improvement in cost performance means the exotic features formerly only available on a few large machines can now be incorporated in smaller systems.

CONTENT ADDRESSABLE MEMORY ELEMENT (CAM)

INTRODUCTION

The concept of a Content Addressable Memory (CAM) or so called Associative Memory has been discussed in literature for some years. However, efficient hardware solutions have not been available in the past. Thus, the use of content addressable memories has been limited to small and specialized systems in which data association was implemented with the more basic Random Access Memory (RAM) and the use of suitable sub-routines.

The CAM element described here is an integrated circuit array of eight memory cells together with the necessary logic that permits direct data association. The more conventional memory functions of read-out and write-in can also be performed.

A CAM element is addressed by associating input data, or so called 'keys', with some or all of the stored words. This approach differs from the conventional memory organization where an arbitrary number which has no relation to the stored data is assigned to each address location.

Because of its organization the CAM is uniquely suited to do parallel searches by data association. Moreover, searches can be done on an entire data word or on specific fields only because of the ability to mask data columns. This gives the CAM inherent ternary search characteristics.

The CAMs usefulness is best described by an example: Suppose a list containing the names of persons, their birthdays, professions and home addresses is stored in a CAM. If we are interested in whether an engineer is on this list, the CAM is able to check every cell simultaneously by using the coded form for engineer as the address number. Therefore the data word ENGINEER, being an address at the same time, acts as a key in this example. As the key is associated with the stored data, this memory is often called ASSOCIATIVE MEMORY.

This next example shows another possible key combination. An engineer with the name Smith may be searched. When the two keys ENGINEER and SMITH correspond with one stored data, the location will be indicated and remaining data, date of birth and home address, can be retrieved.

To do the same search process with a conventional memory, all information must be read-out and compared with the key. This search is a serial process and, hence, time consuming. Thus, CAM elements are well fitted for information retrieval and have definite advantages over conventional memories.

LOGIC DIAGRAM FOR 8220 CAM ELEMENT

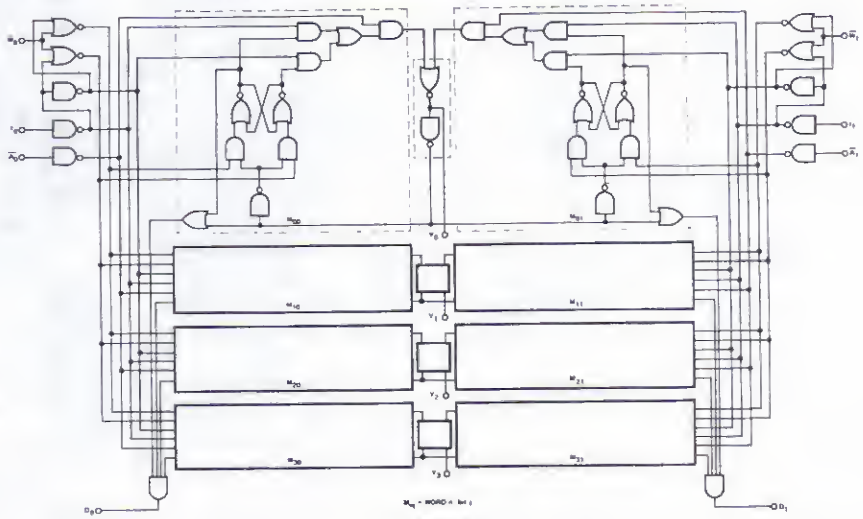


FIGURE 1

Using micro-programmed algorithms, a CAM array with some additional circuitry is a powerful tool for performing more sophisticated search operation. We may look for maximum or minimum values stored in the memory. By using a different algorithm, searches between or outside limits can be implemented.

The CAM has been found useful in many applications, some of which are file operations, list searching, traffic control, artificial intelligence, language translation, matrix manipulations and medical diagnosis.

ORGANIZATION AND LOGIC DIAGRAM

The CAM element consists of eight identical memory cells together with the necessary addressing and decoding logic to perform several modes of operation. These are Associate, Hold, Write-in, and Read-out.

The Memory cells (M_{nj}) are organized as four words of 2 bits each. However, Figure 1 illustrates that the CAM has two sections which may be operated independently. This versatility is especially useful in larger arrays since a section may be addressed while the rest of the memory is masked (that is, effectively disabled).

FUNCTIONAL DESCRIPTION

ASSOCIATE MODE

When the Associate controls ($\overline{A}_j$) are in the zero state while the Write controls are disabled ($\overline{W}_j$ = 1), the information presented to the data inputs (I_j) is compared simultaneously with the stored data cell content. This data cell association results in defined logic levels on the Y_n lines. If any or all of the stored data match the information on the data inputs, the corresponding Y_n outputs will be high. The remaining Y_n outputs will be low, indicating that no match occurred in those positions.

In numerous applications it may be of interest to look for data association in selected columns only. This is possible with the CAM element since the $\overline{A}_0$ input may be low while the $\overline{A}_1$ as well as the $\overline{W}_0$ and $\overline{W}_1$ are high. Consequently, only the I_0 is compared with the data cells in the zero column. Since all bits in the one column are not associated, they are effectively masked. Operation of the CAM can be seen from the table below.

$\overline{W}_0$	$\overline{W}_1$	$\overline{A}_0$	$\overline{A}_1$	I_0	I_1	FUNCTION	RESULT
1	1	0	1	X	X	Associate is $I_0 = M_{i0}$	Yes $Y_i = 1, Y_k = 0$ No $Y_i = Y_n = 0$

In an analogous manner, data association takes place between the I_1 input and the data cells in the one column.

If so desired, all data inputs (I_j) can be associated simultaneously with the memory content by enabling all the $\overline{A}_j$ inputs. As a result, a word at the inputs (I_0 and I_1) will be compared with all words in storage. Only if a stored word matches the key at the data inputs will the Y_j output show a match. For this mode of operation, the function table looks as follows.

$\overline{W}_0$	$\overline{W}_1$	$\overline{A}_0$	$\overline{A}_1$	I_0	I_1	FUNCTION	RESULT
1	1	0	0	X	X	Associate are $I_0 = M_{i0}$ and $I_1 = M_{i1}$	Yes $Y_i = 1, Y_k = 0$ No $Y_i = Y_k = 0$

HOLD MODE

When neither the Write Enable ($\overline{W}_j$) controls nor the Associate Controls ($\overline{A}_j$) are enabled, the CAM is in the Hold mode. This means that regardless of the state of the Data Inputs (I_j) no action takes place and the stored data will not be affected.

The logic diagram shows that the Y_i outputs will be at a "1" if no data association takes place. Thus, in the Hold mode, the D_j outputs reflect the following conditions:

$\overline{W}_0$	$\overline{W}_1$	$\overline{A}_0$	$\overline{A}_1$	I_0	I_1	FUNCTION	DATA OUTPUTS
1	1	1	1	X	X	Hold	$D_0 = M_{00} \cdot M_{10} \cdot M_{20} \cdot M_{30}$ $D_1 = M_{10} \cdot M_{11} \cdot M_{21} \cdot M_{31}$

WRITE-IN MODE

If we want to write-in information presented to the I_j inputs, the corresponding write lines have to be enabled ($\overline{W}_j$ = 0). Again, we have the option or writing in just 1 bit or a whole word since the memory is organized in two sections.

Whenever a write line is enabled ($\overline{W}_j$ = 0), all the data cells in the respective column are conditioned to accept input data. To see this point, recall that the Associate controls are high ($\overline{A}_j$ = 1) during the write cycle. Referring to the logic diagram, we find that under this condition all data cells are enabled. However, the Y_n outputs are of the open collector type and by using external logic they may be forced to ground. By forcing a Y_n line to ground, the corresponding data cells are inhibited and no write-in can occur in that word position.

Therefore, in contrast to the Associate mode (where the Y_n lines act as outputs), the Y_n lines are used here as address select inputs. Only in positions where the Y_i input is not forced to ground (Y_i = 1) will the data cells accept data. The write-in operations possible are summarized as follows:

$\overline{W}_0$	$\overline{W}_1$	$\overline{A}_0$	$\overline{A}_1$	I_0	I_1	FORCED Y_i	FORCED Y_k	FUNCTION	RESULT
1	0	1	1	X	X	1	0	Write-in	Write I_1 into M_{i1}
0	1	1	1	X	X	1	0		Write I_0 into M_{i0}
0	0	1	1	X	X	1	0		Write I_1 and I_2 into M_{i1} and M_{i0}

READOUT MODE

When the control variables A_0, A_1, W_0, and W_1 are high, the memory is described as being in the Hold mode. We now make use of the Y_n lines for address decoding as we did in the write operation. All Y_n lines are forced to "0" except the Y_j where a word has to be read out. The content of the selected memory cells is thus made available at the D_j output terminals as shown:

$\overline{W_0}$	$\overline{W_1}$	$\overline{A_0}$	$\overline{A_1}$	I_0	I_1	FUNCTION	FORCED Y_i	FORCED Y_K	RESULT
1	1	1	1	X	X		1	0	$D_0 = M_{i0}$
1	1	1	1	X	X	Readout	1	0	$D_1 = M_{i1}$
1	1	1	1	X	X		0	0	$D_0 = D_1 = 0$

HYBRID OPERATIONS

Since the four 2-bit words of the CAM element are organized in such a way that the two bits of each word have a common Y line, certain hybrid operations are possible. For instance, the I_0 data input may be associated with the M_{i0} data cells. If a match exists, this will be indicated by having the corresponding Y line high. The Y_n output states can now be used as address decoding for the other half which may be put into the write mode. Thus we can write I_1 into M_{i1} where I_0 matches M_{i0}. A similar argument holds true for writing data into M_{i0} when we have a match in the M_{i1} half. The following table shows these conditions.

$\overline{W_0}$	$\overline{W_1}$	$\overline{A_0}$	$\overline{A_1}$	I_0	I_1	REMARK	RESULT
1	0	0	1	X	X	is $I_0 = M_{i0}$	Yes Write I_1 into M_{i1} No Don't write
0	1	1	0	X	X	is $I_1 = M_{i1}$	Yes Write I_0 into M_{i0} No Don't write

SUMMARY

For convenience, the different modes of operation of the CAM element are tabulated below:

W_0	W_1	A_0	A_1	I_0	I_1	FUNCTION	REMARKS (Ref. Definitions and Glossary)
1	1	1	1	X	X	HOLD	NO OPERATION
							Question → Answer → Output State
1	1	1	0	X	X		? $I_1 = M_{i1}$ → YES → $Y_i = 1, Y_k = 0$; → NO → $Y_i = Y_k = 0$
1	1	0	1	X	X	ASSOCIATE	? $I_0 = M_{i0}$ → YES → $Y_i = 1, 1, Y_k = 0$; → NO → $Y_i = Y_k = 0$
1	1	0	0	X	X		$I_1 = M_{i1}$ and $I_0 = M_{i0}$ → YES → $Y_i = 1, Y_k = 0$; → NO → $Y_i = Y_k = 0$
							Forced Y_i Y_k
1	0	1	1	X	X		1 0 WRITE I_1 INTO M_{i1}
0	1	1	1	X	X	WRITE–IN	1 0 WRITE I_0 INTO M_{i0}
0	0	1	1	X	X		1 0 WRITE I_1 and I_0 INTO M_{i1} and M_{i0}
1	1	1	1	X	X		1 0 $D_0 = \begin{matrix} 1 - \text{IF } M_{i0} = 1 \\ 0 - \text{IF } M_{i1} = 0 \end{matrix}$
1	1	1	1	X	X	READ OUT	1 0 $D_1 = \begin{matrix} 1 - \text{IF } M_{i1} = 1 \\ 0 - \text{IF } M_{i1} = 0 \end{matrix}$
1	1	1	1	X	X		0 0 $D_0 = D_1 = 1$

GLOSSARY OF TERMS–SUBSCRIPTS

n = Word number = 0,1,2, and 3
j = Bit number = 0 or 1
i = Input/output number(s) associated with cell(s) upon which a "Write-In", "Read-out" or other function is being performed.
k = Input/output number(s) other than "i" above.
M = Designation of Memory Cell (word) — eight identical cells in each package.

EXAMPLES

I_j for bit "1" equals I_1
$M_{nj} = M_{10}$ = word "1" bit "0"
Y_i 0, Y_k = 1: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3} = 0$ and $Y_{0,2} = 1$

CAM ARRAYS

The 8220 CAM element can be easily expanded into larger arrays by connecting the D_j and Y_n lines. A 64-bit CAM implementation is shown in Figure 2. The D_j and Y_n lines are open collector outputs and are connected together to perform the logical AND. An external pull-up resistor is returned to V_{CC} to enhance the speed of operation.

64–BIT CAM ARRAY

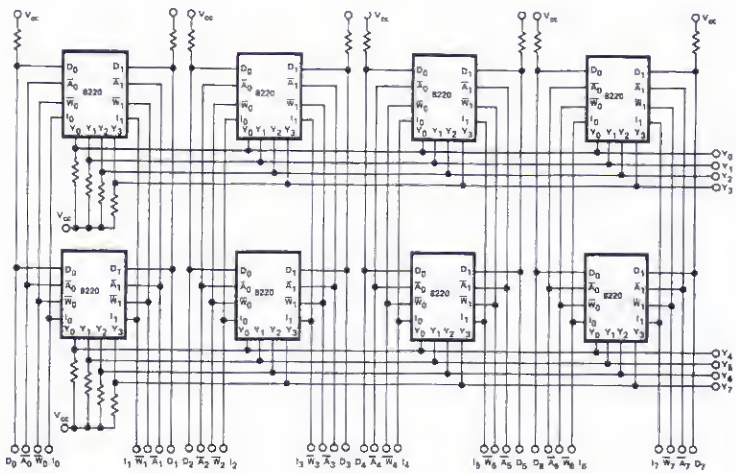


FIGURE 2

APPLICATIONS:

INFORMATION RETRIEVAL

CAM elements may be interconnected such that a word at the data input is compared simultaneously with the total memory content. If one or more words in the memory match the key, the corresponding Y_n line will be high (Y_n = 1) when the Associate line is activated.

By enabling the Write line, the word that is present at the data inputs is written into the locations selected by the Y_n lines. An address location is made available by letting Y_i stay at 1 while the remaining Y_n are forced to "0".

An arrangement like the one shown in Figure 3 is very useful when used in conjunction with larger memories. For information retrieval, searching a CAM for a match is very fast since it is done in parallel. The matching word may be read out and used as a key for larger conventional memories.

INFORMATION RETRIEVAL

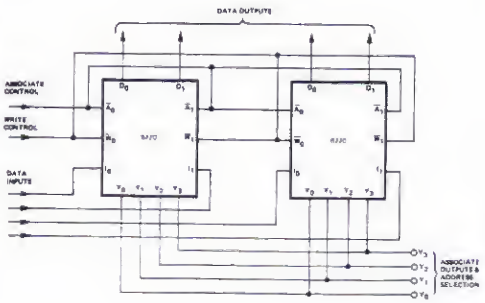


FIGURE 3

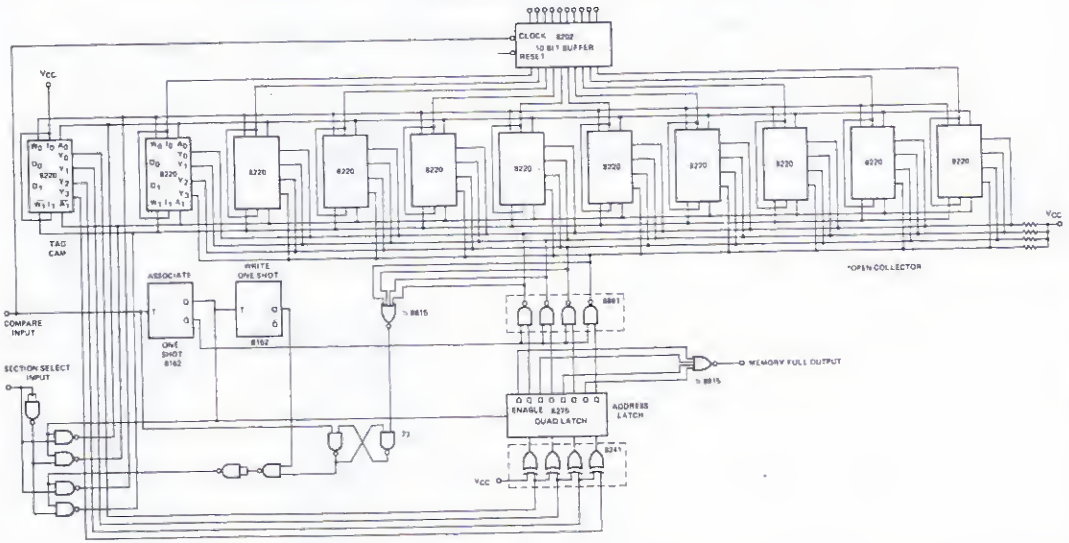
LEARNING MEMORY

This system (Figure 4) is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being eight 10-bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in number of words and word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word is already contained in storage, no need for learning, (data acquisition) exists. This fact is indicated by a match from one of the Y_n lines (Y_i = 1) and thus the write command is inhibited.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

LEARNING MEMORY



NOTE: All other gates 8880

FIGURE 4

MASKED SEARCH

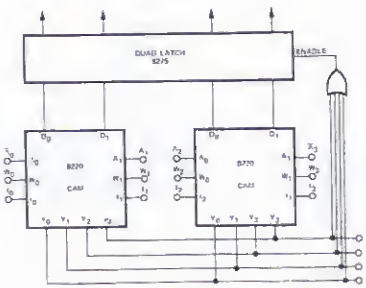


FIGURE 5

MASKED SEARCHES

If it becomes desirable to search for matching conditions in selected columns only, use can be made of the masking technique. In Figure 5, only the first column will be associated with its input data. Let us say we are searching for 1's (I_0 = 1) in the first column. If a match exists, the word is read out.

For convenience we shall say that the data cells are filled as follows:

$$M = \begin{bmatrix} M_{00} & M_{01} & M_{02} & M_{03} \\ M_{10} & M_{11} & M_{12} & M_{13} \\ M_{20} & M_{21} & M_{22} & M_{23} \\ M_{30} & M_{31} & M_{32} & M_{33} \end{bmatrix} = \begin{bmatrix} 0 & X_{01} & X_{02} & X_{03} \\ 1 & X_{11} & X_{12} & X_{13} \\ 0 & X_{21} & X_{22} & X_{23} \\ 0 & X_{31} & X_{32} & X_{33} \end{bmatrix}$$

where

$$X_{ij} = 0 \text{ or } 1$$

The instructions given to the control lines are given below:

CONTROL LINES								DATA INPUTS				ASSOCIATE LINE				DATA OUT			
$\overline{W}_0$	$\overline{W}_1$	$\overline{W}_2$	$\overline{W}_3$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3	D_0	D_1	D_2	D_3
1	1	1	1	0	1	1	1	1	X	X	X	0	1	0	0	1	X_{11}	X_{12}	X_{13}

Only one matching event occurred in the M_{10} position and in response to it $Y_1 = 1$. This enables the Quad Latch and the data word ($1\ X_{11}\ X_{12}\ X_{13}$) is read out. If more than one matching event is being expected, the matching data addresses $Y = (Y_0\ Y_1\ Y_2\ Y_3)$ must be stored. Subsequently, the different data sets $D = (D_0\ D_1\ D_2\ D_3)$ are read out serially.

For example, let us assume that another data set M is stored in the CAM array:

$$M = \begin{bmatrix} 1 & X_{01} & X_{02} & X_{03} \\ 0 & X_{11} & X_{12} & X_{13} \\ 1 & X_{21} & X_{22} & X_{23} \\ 0 & X_{31} & X_{32} & X_{33} \end{bmatrix}$$

where

$$X_{ij} = 0 \text{ or } 1$$

We are searching for 1's in the first column as we did in the previous example. Initially, the instructions to the control lines remain the same. Since we have two matching events now, i.e. M_{00} and M_{20}, the read-out of the two data words has to be done serially. Therefore, the response of the Associate outputs is stored in a shift register before a read cycle is initiated.

In addition to the shift register information, which is made available serially, a binary counter and decoding is necessary to condition the Y_n lines for readout. The hardware solution is shown in Figure 6.

CAM IMPLEMENTATION FOR MASKED SEARCHES

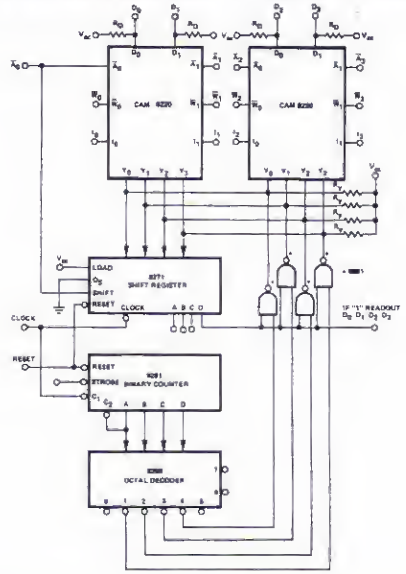


FIGURE 6

SEARCH FOR MAXIMUM OR MINIMUM VALUES

Let us assume that only numbers are stored in a CAM array. Thus, we may want to find the largest number in the memory. This can be done by a micro-programmed algorithm, which is a process of successive data association.

We first search for 1's in the column where the most significant bits (MSBs) are located while the other columns are masked. The key associated with the data in MSB column is given by $I_0 = 1$.

If at least one matching condition exists, the key is modified to include the next lower order bit in the data association, such that $I_0 = 1, I_1 = 1$.

However, if no matching condition exists with the key $I_0 = 1$, we know that the content of all the cells in the MSB column is equal to "0". In this case, the key will have to be modified in the second step, namely, $I_0 = 0$, $I_1 = 1$ rather than $I_0 = 1$, $I_1 = 1$ as above.

Finally, the key $I = (I_0, \ldots . I_n - 1)$ will be equal to the largest number stored while the Y_n lines will indicate its address location.

As an illustration of the described technique, the following set of numbers is considered.

MSB ↓ LSB ↓

$$M = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

A search for 1's in the left most column is done by these instructions:

$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	1	1	1	1	X	X	X	1	1	0	1

Since three matches exist on the Y_n lines, the key will be modified in the second step:

$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	1	1	1	1	X	X	0	0	0	0

However, no match is shown on the Y_n lines which means that the key must be altered as shown:

$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	1	1	1	0	X	X	1	1	0	1

In the next step, three bits are associated:

$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	0	1	1	0	1	X	0	1	0	0

No modification takes place since at least one matching condition exists. The last association gives us the following results:

$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	0	0	1	0	1	1	0	0	0	0

which implies a modification has to be made in the last position:

$$I = (I_0\, I_1\, I_2\, I_3) = (1\ 0\ 1\ 0)$$

This is actually the largest number stored in the array and when it is associated with the stored numbers, the Y lines indicate its location. Namely, $Y = (Y_0\, Y_1\, Y_2\, Y_3) = (0100)$ indicates that it can be found in row 1.

On the other hand, if the smallest number stored in the array has to be found, we will first search for 0s in the MSB column. If a matching condition exists, the key will be modified to include the next bit, namely, $1 = (I_0, I_1) = (0,0)$.

However, if the Y outputs now show a mismatch, it will have to be altered to 1 = (10). We see that the procedure is the same as discussed before.

A hardware implementation that finds the largest number is shown below (Figure 7). Two CAM elements are interconnected to form the array. The shift register is used to enable the ASSOCIATE inputs which are stepped in successively, one for each clock pulse. To provide the key for the data lines, the outputs of a binary counter are decoded to drive a bank of flip-flops. Their outputs are in the 1 state, except when the key has to be modified on the next clock pulse.

Such a condition exists, every time the Y outputs are decoded as Y = (0000) showing a mismatch.

CAM IMPLEMENTATION FOR MAXIMUM VALUE SEARCH

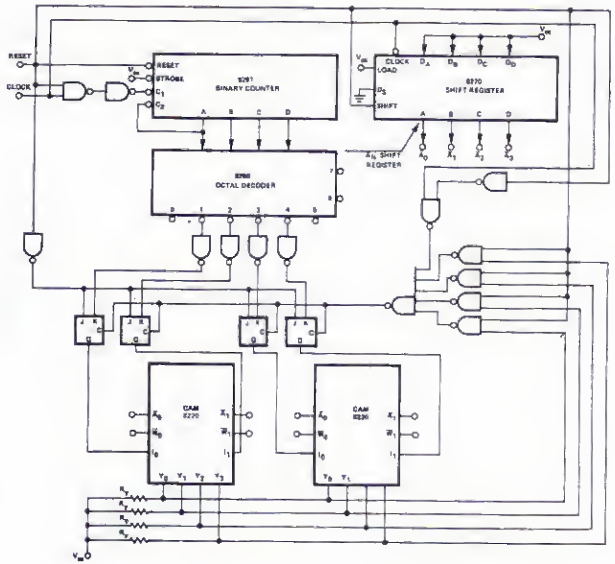


FIGURE 7

A HIGH SPEED READ - WHILE - WRITE RAM

When to a 64 bit RAM, one adds an on chip latch the capabilities of the device are greatly expanded. The 82S21 is such an integrated circuit and it is manufactured using the Signetics high-speed high-density 3μ epitaxial Schottky process for added performance. The 82S21 features include: 1) 32 X 2 organization to optimize the 16 pin package; 2) bit masking to provide the device to be used as two independent 32 X 1 RAMs or a single 32 X 2 buffer; 3) on chip output latches which can be effectively bypassed for standard RAM usage, or utilized to hold data for read-out while writing any information into any word of the memory; and 4) high current open collector outputs for high speed expansion without the generation of noise so probable in tri-state devices. These features provide the capability for several unique applications.

OPERATION

Storage of the 32 words of 2 bits is accomplished in 64 memory cells as shown in figure A. These diode coupled cells are actually arranged in a 16 X 4 matrix. Each cell has two sense lines per bit row and sixteen word select lines. Input A_4 multiplexes the sense lines (see figure A; Gates G_9, G_{10}, G_{11}) to form the 32 by 1 organization for the read sense amplifiers as well as the write mode logic (see figure A; Gates G_5, G_6, G_7, G_8). The address gates use an unusual technique of combining two address lines to form four word select logic lines to match propagation delays. This prevents internal race conditions eliminating reading or writing in unselected cells while changing the address lines (see figure A).

82S21 FUNCTIONAL DIAGRAM

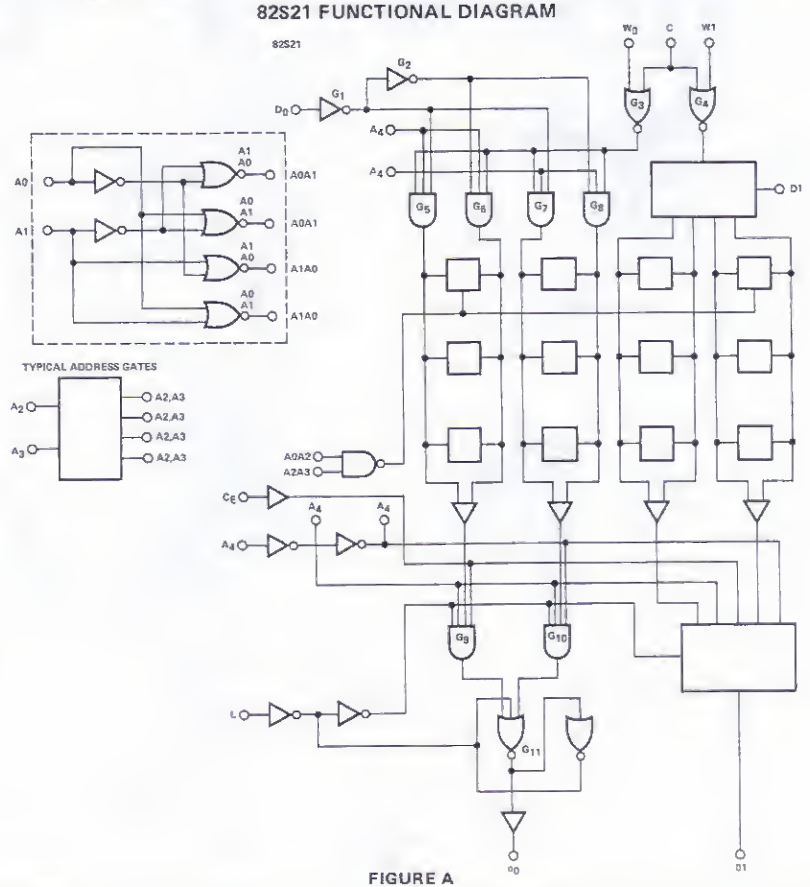
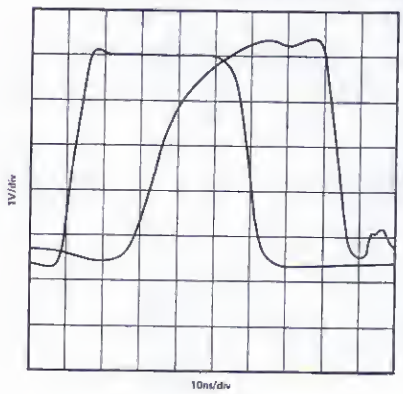


FIGURE A

The output latch and the chip enable are arranged such that the data may be retained in the latch even when the chip is disabled (see figure A). The separation of latch control from the chip enable line allows data stored in one memory chip to be read while addressing a word in another device with the outputs of the several parts bussed together. This separation of control lines also makes it possible to write information into the memory while the outputs are held in the disabled state. This is accomplished by simply disabling the chip, activating the latch, then enabling and writing.

The open collector outputs each have a minimum of 48mA of drive capability. This high current output allows busing and driving very high capacitive loads with high speed. The rise and fall times of a fully loaded output with 100pf will be approximately 4ns through the threshold of the driven TTL inputs (see figure B).

OUTPUT RISE TIME FOR 82S21 UNDER HEAVY LOAD



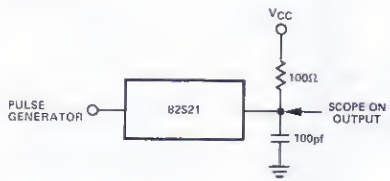


FIGURE B

All the inputs are fully buffered and require only −1.6mA of low level "0" input current to allow a 320 word buffer to be driven from standard TTL. The three write pins; W_0, W_1, and C; provide the capability of writing into either cell of the addressed word individually or both cells simultaneously allowing the device to be used as two separate 32 X 1 stores or a single 32 X 2 RAM. Furthermore, writing can be done asynchronously to the system clock or the internal write inputs can be enabled by W_0, and W_1 and strobed with the system clock driving the C line, providing the ability to compensate for timing due to logic delays (see figure C).

SYNCHRONIZING WRITING DATA INTO THE 82S21 WITH SYSTEM CLOCK

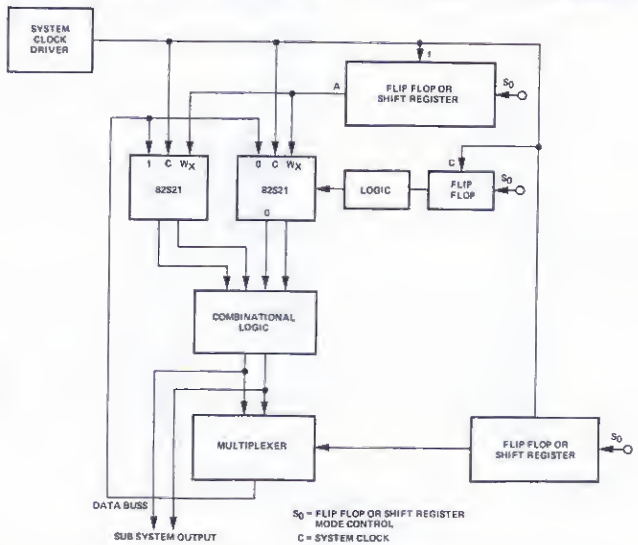


FIGURE C

HIGH SPEED ACCUMULATOR

Figure D shows the 82S21 used as a buffer register in an accumulator section that can be hardwired to perform the function A+B A with a minimum number of integrated circuits at high speed. The function A+B A can be performed in typically 70 nanoseconds when starting with data stored in the 82S21's used as registers A and B. The use of the 32 X 2 RAM with on chip latches eliminates the need for an external holding register. The data path takes information from the RAM and latches the information in the on chip latch, through the 74181 ALU and the 82S33 Quad two input multiplexer and back into the A register. Data can initially be loaded into the A register through the other set of multiplexer inputs.

BASIC 8 BIT FULLY BUFFERED ACCUMULATOR

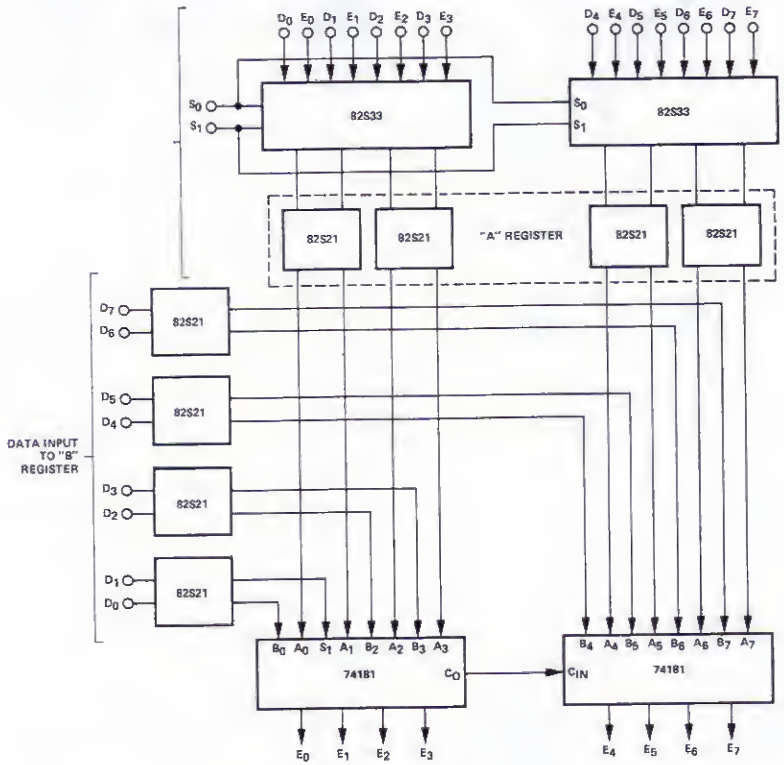


FIGURE D

By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32 X 8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B — A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

SYNCHRONOUS CONTROL OF THE WRITE FUNCTION

The 82S21 can be embedded in the TTL logic with the system clock controlling writing synchronously while propagation delays of the other TTL elements which are driven by the same clock. This synchronizing of writing is accomplished by having the system clock drive the C control line of the RAM and the clock line of flip-flop (or shift register) A in figure C. The output of flip-flop (or shift register) A directly drive the W_X line(s) of the RAM. Data is then written into the memory only when the C and W_X are at logical 0.

USE OF BIT MASKING

The 32 X 2 organization, with independent bit write control (bit masking), provides the ability to manipulate individual bits. This allows a multiple byte oriented buffer memory with individual byte parity to be implemented with a minimum number of memory devices. A 32 word by 2 byte system with byte parity maintained is shown in figure E. In this application four of the RAMs are used to store 32 words (bytes) of information. Since the devices have independent bit write control lines, W_X, only one

32 WORD BY 2 BYTE MEMORY WITH BYTE PARITY MAINTAINED

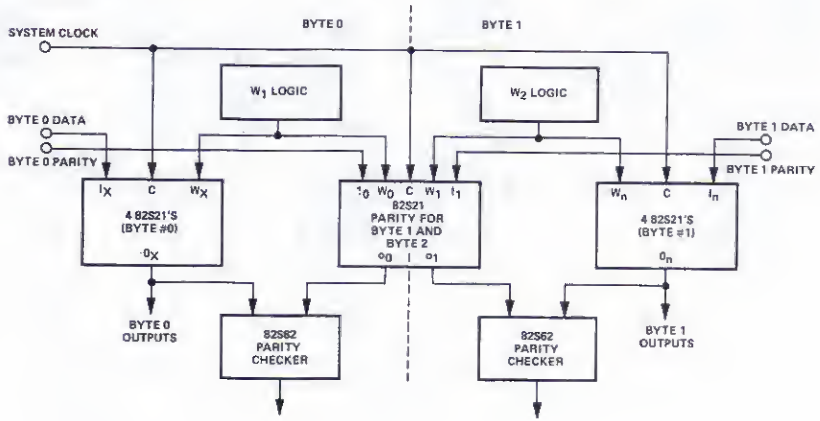


FIGURE E

additional RAM is required to store parity bits for both bytes by using word 0 for byte 0 and word 1 for byte 1.

A masking operation is shown in figure F. The mask word is loaded into a register connected to the W_X inputs. Data to be masked is connected to the 1 inputs. When the strobe occurs the logical product of the data and mask registers is written into the addressed location. It should be noted that for positive logic the data in the mask register must be inverted since a "0" at W_X is the enabling condition.

CONCLUSION

The unique features incorporated in this RAM allows its use in many applications where a normal scratch pad would have to be accompanied by additional logic elements such as flip-flops and high current open collector gates. Furthermore, the 82S21 has several features not available in other bipolar memories and cannot be easily implemented by the simple addition of other components. These features are bit masking; 25 nanosecond typical access time, including latch delay; and edge triggered write control. The combination of these features allows the design engineer to optimize his system requiring small, fast memory elements.

ECONOMIC ADVANTAGES OF MICROPROGRAMMING

- SYSTEM COST OF IC's
- COST OF MICROPROGRAMMED CONTROL
- TYPE OF CONTROL MEMORY TO USE
- CONCLUSION

ABSTRACT

A set of economic arguments are presented for using microprogrammed control in place of random logic. It is shown that a single 4096 bit ROM can potentially save the user $119 for each ROM employed or about 2-½ cents per bit. The types of control memory elements (ROM, RAM, and FROM or Fusable Read Only Memory) are reviewed and the situations in which they should be applied are discussed.

All prices in this report in dollars — the measurement of cents/bit being the usual standard for measurement of system costs.

ECONOMIC ADVANTAGES OF MICROPROGRAMMING

Microprogramming was originally conceived by M. V. Wilkes as a systematic and orderly approach to designing the control section of any digital computer. Since Wilkes first advanced his idea in 1951, numerous papers and reports have been written on the subject. In recent years the technique has come into widespread use. References 2, 3 and 4 will give the reader adequate background to understand the techniques used in designing microprogrammed systems. The purpose of this paper is to point out some of the economic and other advantages which the system designer will enjoy if he employs bipolar semiconductor storage to implement the control store in a microprogrammed device.

By using bipolar RAM's and ROM's to replace random bipolar logic in the control section of any digital system, the designer can, depending on the complexity of the system, save significant amounts of money, space and power. An exact analysis of the savings is almost impossible unless one is willing to perform both conventional and microprogrammed designs of a number of highly complex systems. No published data of this type is known to the author. However, any reasonable set of assumptions leads one to the conclusion that microprogramming is truly a better way, by a wide margin, to design any complex digital system which can work with a basic control memory cycle greater than 100 nanoseconds.

In order to understand why this is true, one must first examine the true cost of putting an IC into a digital system.

SYSTEM COST OF IC's

The direct cost of putting an IC into a system is over $1.00. Figure 1 shows a breakdown of these costs which one experienced manufacturer of digital systems considers reasonable. When all of the direct costs in fabricating a system are taken into account, such as indicator lamps, maintenance panels, system cabling, etc. and the total system manufacturing cost is divided by the number of IC's, a figure of $2.00 per IC is frequently arrived at. The $1.05 number of figure 1 will be used during the rest of this discussion because there seems to be general agreement that getting rid of one IC will usually save a manufacturer that much money.

It is interesting to note that under the assumptions of figure 1 even if IC's were free, the total manufacturing cost could be reduced only by 30%. Assuming designers continue to use conventional SSI (Small Scale Integrated) circuits and packaging approaches in design of their systems, there will be almost no further significant decrease in the manufacturing cost of digital systems.

If one assumes that the average IC contains 3 gating functions, then the direct cost per gate installed in a system will be on the order of 35 cents.

SYSTEM COST/16 PIN DIP ON 88 PIN 60 IC BOARD	
IC	.30
Incomming Inspection	.05
PC Cord	.25
Component Insertion and Fabrication	.03
Board Check Out	.05
Connector	.05
Capacitor	.03
Wiring	.09
Power Supply $1.00/Watt	.10
Cabinetry/Card Guides/Fans/etc.	.10
	$ 1.05

FIGURE 1

COST OF MICROPROGRAMMED CONTROL

For the most elementary type of devices random control logic will always be the most economical way to design a system. If, for example, a device can be controlled by a single pre-set counter, it is impractical to become involved in the intricacies of microprogrammed control. This is because a microprogrammed device has a base cost associated with the address sequencing and memory selection circuitry which is incurred no matter how simple the device is. This is represented in figure 2. Properly designed semiconductor control storage has most of the memory selection circuitry integrated into the chip and this greatly reduces the base cost.

Figure 2 shows the cost of microprogrammed control increasing slowly with the number of sequencing cycles. This is because each additional sequence cycle will in general require one additional wordf control store. If, for example, the control memory of a device used 32 bit words and the control store cost only 0.25 cents/bit, as such devices will in the future, then the cost of an additional control cycle is only 8 cents.

The cost of conventional control in figure 2 is shown increasing at a fairly fast rate. One can see that if an additional control cycle required only one additional gating function or some type of storage element to distinguish it from all the other control states, then at least one gate or 35 cents direct cost must be added to the system cost. For this simple example, the cost of conventional control increases at over four times the rate per sequencing cycle of microprogrammed control.

COST COMPARISON OF CONVENTIONAL AND MICROPROGRAMMED CONTROL

FIGURE 2

There are few hard facts to back up any estimates on the efficiency of microprogrammed devices but most designers seem to agree that somewhere between 8 and 16 bits of ROM can be used to replace a gating function. If 16 is considered to be a pessimistic number and 8 an optimistic one, then a 4096 bit ROM is capable of replacing between 256 and 512 gating functions. This ratio provides a great incentive to the designer to employ microprogramming.

COST OF ROM IN MICROPROGRAMMED SYSTEM

	1¢/BIT	0.5¢/BIT	0.25¢/BIT
IC (4096 BIT ROM)	40.00	20.00	10.00
Incomming Inspection	.50	.50	.50
PC Cord	.25	.25	.25
Component Insertion and Fabrication	.03	.03	.03
Board Check Out	.15	.15	.15
Connector	.05	.05	.05
Wiring	.22	.12	.12
Power Supply $100/ Watt	.50	.50	.50
Cabinetry/Cord Guides/ Fans/etc.	.10	.10	.10
	$41.80	$21.70	$11.70

FIGURE 3

Figure 3 shows the direct cost of putting a 4096 bit ROM in a microprogrammed system assuming costs per bit of 1, 0.5 and 0.25 cents. If R bits of ROM replace a single gating function, then the dollars saved by employing a single 4096 bit ROM at 0.25 cents/bit are:

$$\text{Savings} = 0.35 \times \frac{(4096)}{R} - \$11.70$$

These savings are plotted in figure 4 for various costs of ROM.

NUMBER OF ROM BITS TO REPLACE A GATE FUNCTION

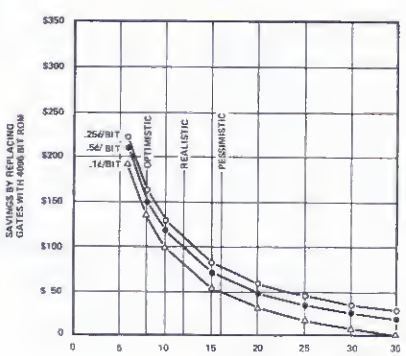


FIGURE 4

While 12 bits is probably a realistic number per gating function replaced, it is interesting to note that the breakeven points for 1, 0.5 and 0.25 cents per bit ROM's are 36,66 and 122 bits. With a 4096 bit bipolar ROM there can be a tremendous margin of error in the assumptions and still have microprogramming be the most economical approach to system design.

Other savings result as well. These are tabulated in figure 5. For example, if one assumes 12 bits of ROM will replace a gate function, then the use of 4096 bit ROM's in the control portion of a digital system will save about 114 packages, 8.5 watts of power and 100 cubic inches of volume in addition to $119 per 4096 bit ROM employed.

Systems today are beginning to use RAM's in their control memories. When RAM's are used in the control memory, it is referred to as WCS (Writeable Control Store). It can be argued that fewer bits of RAM are capable of replacing a gate than are bits of ROM. Because the control store can be altered it can be loaded with information which will tailor the device to the application or environment. For example, the basic IBM 360/85 contains a 512 word control store which can be loaded with any of 30 sections of non-resident microdiagnostics which are up to 512 words in length. These diagnostics are used to isolate malfunctions in the system. An emulator option consisting of another 512 words of WCS is also available with the system. This option is used principally to enable the IBM 360/85 to emulate an IBM 7090/7094. Obviously other machines could be emulated by reprogramming the control store. The important point is that bits of control store take on multiple uses. Some bits will be used in as many as 30 different ways in the IBM 360/85.

SAVINGS BY USING 0.25¢/BIT ROM IN MICROPROGRAMMED CONTROL OF DIGITAL SYSTEM

	BITS PER GATE FUNCTION		
	8 OPTIMISTIC	12 REALISTIC	16 PESSIMISTIC
No. of Dips Saved	170	114	85
PC Cards Saved 60 Dips/Board	3	2	1.5
Power Saved in Watts	12.8	8.5	6.4
Volume Saved in IN^3	150 IN^3	100 IN^3	75 IN^3
Dollars Saved per 4096 BIT ROM	$168	$119	$83

FIGURE 5

Once again there is no precise way of determining how may bits of RAM will be required to replace a gate. Designers seem to feel comfortable in assuming a number in the range of 5 to 12 bits. Figures 6, 7 and 8 show costs and savings involved in using WCS in the same fashion as figures 3, 4 and 5 did. Figure 9 shows the total savings involved in both types of control stores assuming ROM costs 0.25 cents/bit and RAM costs 2 cents/bit. It is interesting to note the saving of ROM over RAM differ less than two to one. RAM, however, offers the designer a great deal more flexibility to correct errors.

The designer is faced with some difficult choices. He must decide whether he wants to commit his design to a semiconductor ROM which cannot be altered, or use more expensive RAM.

COST OF WCS (RAM) IN MICROPROGRAMMED SYSTEM

	10¢/BIT	5¢/BIT	3¢/BIT	2¢/BIT
IC 256 BIT RAM	25.00	12.50	7.50	5.00
Incoming Inspection	.10	.10	.10	.10
PC Card	.25	.25	.25	.25
Component Insertion and Fabrication	.03	.03	.03	.03
Board Check Out	.05	.05	.05	.05
Connector	.05	.05	.05	.05
Wiring	.07	.07	.07	.07
Power Supply $1.00/Watt	.50	.50	.50	.50
Cabinetry/Card Guides/Fans/etc.	.10	.10	.10	.10
	$26.15	$13.65	$8.65	$6.15

FIGURE 6

NUMBER OF RAM BITS TO REPLACE A GATE FUNCTION IN WRITEABLE CONTROL STORE SYSTEM

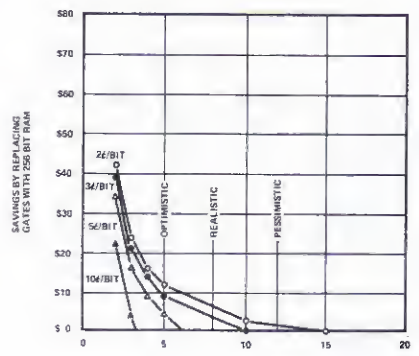


FIGURE 7

SAVINGS BY USING 2¢/BIT RAM IN WRITEABLE CONTROL STORE OF DIGITAL SYSTEM			
	BITS PER GATE FUNCTION		
	5 OPTIMISTIC	8 REALISTIC	12 PESSIMISTIC
No. of Dips Saved	17	11	7
PC Cards Saved 60 Dips/Board	.28	.18	.12
Power Saved in MW	600	300	—
Volume Saved in IN^3	14 IN^3	9 IN^3	6 IN^3
Dollars Saved per 256 BITS RAM	$12	$4	$2.50

FIGURE 8

TOTAL SAVING FOR DIFFERENT SIZE CONTROL STORES				
	16K BIT	32K BIT	64K BIT	128K BIT
Micro Programmed ROM Savings	$ 476	$ 952	$ 1904	$3808
Micro Programmed WCS Savings	$ 256	$ 512	$ 1024	$2048

FIGURE 9

THE TYPE OF CONTROL MEMORY TO USE

Three types of semiconductor memories adaptable to the control section of a device exist today. These are ROM's, RAM's and FROM (Fusable Read Only Memories). ROM's offer the customer the lowest cost per bit but require moderately expensive tooling. Errors in programming ROM's cannot be corrected. This, combined with high tooling costs, makes these devices most suitable for volume applications where small numbers of bits (under 65,536 bits) are used. These types of applications are more easily debugged and therefore, field changes to the ROM's will not be required. Furthermore, they permit the tooling to be written off over a large number of units.

FROM's are programmed by blowing fuse links. This fusing can be done either by the customer or at the factory. FROM's of course cannot be altered once they are fused and so errors cannot be corrected. FROM's require little or no tooling to generate a new pattern but their cost per bit is higher than ROM's. This makes them most suitable for low volume, low capacity production.

Writeable Control Store offers the customer the advantage of being alterable and of requiring no tooling. However, systems using WCS must have a way of reloading their control stores. Because of the higher cost per bit, WCS is most commonly found in applications where tooling and lack of alterability would create significant problems, or where alterability will provide significant advantages. These areas are mainly systems with large control stores and low volume production.

Combinations of techniques will find use in the large capacity control memories in volume production. These different applications are shown in figure 10.

APPLICATION FOR VARIOUS TYPES OF CONTROL STORE		
	LOW CAPACITY IN BITS	HIGH CAPACITY IN BITS
Low Production Volume	FROM	WCS
High Production Volume	ROM	ROM + WCS

FIGURE 10

CONCLUSION

This paper has attempted to put a perspective on the application of control memories. While the arguments presented here are imprecise and cannot be proven, they are based to a great degree on the feelings of individuals who are making these decisions. It seems that most decisions about the use

of control memories have been based somewhat on intuition. The author has attempted to document these intuitive feelings. It is highly unlikely that truly factual data of a general nature will ever be developed.

The most interesting point set forth in this study is that the primary factor in determining system cost if conventional SSI is used is the number of packages and not the cost of the IC's. The circuit costs are now so dominated by the other system costs such as fans, power supplies, pc cards, etc., that no further significant cost reductions can be made without employing new technologies. Microprogramming using 4096 bit ROM's with a system cost of $11.70 can reduce system costs by about $119 per ROM. This offers the designer the opportunity to reduce parts cost of the control portion of his device by up to 80%.

DESIGN OF MICROPROGRAMMABLE SYSTEMS

INTRODUCTION

The advent of low cost, high speed ROS (Read Only Storage) has motivated a great increase in interest in microprogrammable devices. Microprogramming techniques are now being applied in terminals, calculators, peripheral controllers, central processors, instruments, etc. A great deal of general information exists on microprogramming but there are very few documents that explain how to implement a system. The purpose of this article is to explain more about the technique, and give the designer some practical ideas on how to go about implementing a microprogrammable system.

There are numerous advantages to microprogrammed implementation. These will be discussed later but it is perhaps worthwhile to list them now so the reader may reflect on these points as he reads this note:

- Reduction of random logic and resulting more structured organization.
- Emulation of a number of devices (not just another processor) can be carried out by a single general purpose device.
- Diagnostics and service aids may be easily implemented in the control portion of the system.
- Field changes can be easily made by changing control stores.
- Special purpose adaptations can be made of the device by changing a few program words.
- Performance can be economically expanded at lower cost than in a conventional system.
- Final system definition can be postponed to a later time in the design cycle.
- Documentation and service training costs can be reduced.

Admittedly these are a lot of advantages to claim for one approach, but the author will review each of these points again at the end of this note and explain in more detail how these benefits can be derived.

To the reader who is unfamiliar with microprogramming, all of the above statements will probably raise the following question in his mind. "If this technique is so good, why hasn't everyone been using it?" The answer is fairly simple — microprogramming just wasn't as attractive until the advent of high speed, high capacity, low cost and low power bipolar ROS. Before the advent of devices such as the SMS 4096 bit bipolar ROS, microprogramming was much more costly and technologically more difficult to implement.

BACKGROUND

The idea of microprogramming is normally attributed to Wilkes. His stated objective was to provide "a systematic alternative to the usual somewhat ad hoc procedure used for designing the control system of a digital computer." Actually, many logic devices being implemented today are far more complex than the computers which are deriving benefits from microprogrammed implementation. Some experts today are forecasting that most complex logical systems of the future will use microprogrammed techniques for the same reasons that motivated computer designers to select this alternative.

In a general sense, any sequential logic device can be viewed as transferring information from one set of storage elements to another through a logic network. In the case of a computer, the execution of an instruction involves a sequence of information transfers from one register in the processor to another, some of which takes place directly and some through an adder or other logical network. A machine or computer instruction is made up of a number of these transfers which Wilkes likened to a program and hence, he termed the individual steps microinstructions and the sequence of steps a microprogram.

The mechanism Wilkes suggested for implementing the system is shown in figure 1. The microprogram was held in a read only diode memory which is shown as consisting of two matricies A and B. The outputs of matrix A were used to control the transfers between the various registers. The outputs from matrix B were passed through a delay and were then used as inputs to a decoding tree. These inputs to the decoding tree directed the timing pulses to the next selected data line in the control store. Information from the sign flip-flop of the accumulator was used to select alternate paths through matrix B and hence to change the next selected data line in the memory. This is represented by one of the lines from matrix A which branches before it enters matrix B. The signals coming from matrix A control arithmetic gates, register paths, etc., which Wilkes viewed as incremental logical operations and called micro-operations. A collection of these operations performed at one time was a microinstruction.

WILKES MODEL OF MICROPROGRAMMED DEVICE

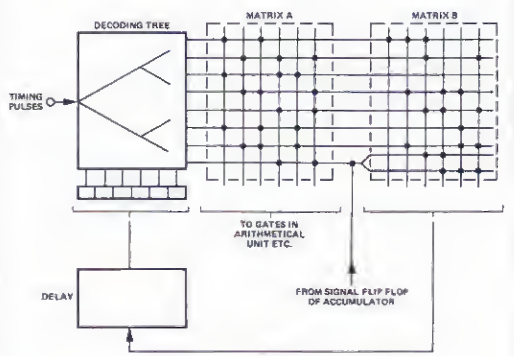


FIGURE 1

Wilkes' example segmented the microprogrammed control into two parts — one for operating the gates which control the data paths, and the other for selecting the next step in the control sequence. Today all microprogrammed devices are organized in a similar fashion. The essence of designing a good microprogrammed system is the selection of the proper strategies for data paths and logic function control as well as the implementation of the control sequence section.

BUILDING A SIMPLE MICROPROGRAMMED SYSTEM

Figure 2 shows a simplified computing element. In reality it could be a word organized single address stored program computer. In this over-simplified version, assume the control portion of the machine generates the following signals shown in Table 1. These signals are called micro-operations. By combining these, instructions can be generated. Assume further that the control portion of the machine contains a ROS (Read Only Store) and that words are read from that ROS under the control of an address register. Words are read from the ROS in sequence unless one of the Jump instructions, JMP, JIFO or JOPC is executed.

MICRO INSTRUCTIONS FOR SIMPLE MACHINE

CODE	MEANING
MARM	Gate MAR onto M bus
MBRM	Gate MBR onto M bus
PCD	Gate PC onto D bus
IAD	Gate IA (instruction address) onto D bus
ACD	Gate AC onto D bus
R	Read memory into MBR
W	Write MBR into memory
PLUS	Add M bus to D bus in address and place on S bus
DTS	Gate D bus through adder to S bus
MTS	Gate M bus through adder to S bus
ONE	Gate D bus through adder to S bus and add one
SMAR	Gate S bus into MAR
SMBR	Gate S bus into MBR
SPC	Gate S bus into PC
SIR	Gate S bus into IR
SAC	Gate S bus into AC
JMP	Jump to address in address field of microinstruction if AC = 0
JIFO	Jump to address in address field of microinstruction if AC = 0
JOPC	Jump to address of OP code field

TABLE 1

SIMPLE MICRO PROGRAMMED MACHINE

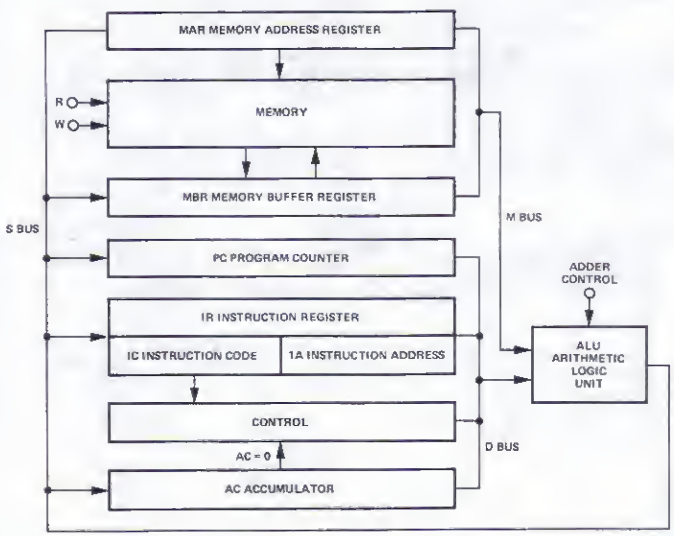


FIGURE 2

Figure 3 shows a ROS instruction word with the appropriate fields labeled. The instruction words are shown under the fields in which they appear in the microinstruction word. There are of course many different microinstruction formats. For example, the Interdata Mod IV on Micro 810 computers use 16 bit formats whereas systems such as the IBM 360/85 use 128 bit formats. The reason for these choices will be discussed later. Figure 3 is meant only as a tutorial example and is not necessarily intended as a practical model.

REPRESENTATION OF MICRO INSTRUCTION WORD						
MEMORY CONTROL	JUMP INSTRUCTION	ADDER CONTROL	M BUS CONTROL	D BUS CONTROL	S BUS CONTROL	JUMP ADDRESS FIELD
R W	JMP JIFO JOPC	PLUS MTS ONE DTS	MARM MBRM	PCD IAD ACD	SMAR SMBR SPC SIR SAC	

FIGURE 3

Figure 4 shows what kinds of simple operations can be accomplished by combining microinstructions. In the example, the contents of memory are added to the accumulator in the following manner:

Line 1 The contents of the program counter are transferred to the memory address register.

Line 2 The instruction is read from memory into the memory buffer register.

Line 3 The instruction is transferred from the memory buffer register to the instruction register.

Line 4 The control of the microprocessor is determined by the operation code of the instruction.

Line 5 The contents of the address portion of the instruction register are transfered to the memory address register.

Line 6 The desired data is read into the memory buffer register.

Line 7 The memory buffer register is added to the accumulator and the result stored in the accumulator.

Line 8 One is added to the program counter so it is ready to fetch the next instruction and the result is stored in the program counter.

Line 9 Control of the microprocessor is transfered to start the next sequence.

It is fairly straightforward to envision more powerful devices than the one given in the example that perform many of the operations determined by separate lines in parallel and which have many more instruction codes.

MICROPROGRAM TO ADD CONTENTS OF MEMORY TO ACCUMULATOR								
		MEMORY CONTROL	JUMP INSTRUCTION	ADDER CONTROL	M BUS CONTROL	D BUS CONTROL	S BUS CONTROL	JUMP ADDRESS FIELD
INSTRUCTION FETCH	1			DTS		PCD	SMAR	
	2	R						
	3			MTS	MARM		SIR	
INSTRUCTION DECODE	4		JOPC					
EXECUTIVE	5			DTS		IAD	SMAR	
	6	R						
	7			PLUS	MBRM	ACD	SAC	
RETURN	8			ONE		PCD	SPC	
	9		JMP					START

FIGURE 4

This example does not really discuss how the ROS is controlled. It merely points out that a control memory can emit signals capable of controlling the data paths in a system. Most articles on microprogramming point out how easy it is to control the data paths using microprogramming techniques and stop. The real essence of microprogramming is focused on controlling the address sequencing of the control memory itself. A substantial portion of this note will be devoted to this point.

To any individual who has done assembly language programming, the similarity between the symbolic microcode shown in figure 4 and assembly language is obvious. The similarity suggests that some techniques used frequently in programming might be useful in doing microprogramming. In fact they are. Three of the most frequently employed techniques are:

- Use of subroutines
- Indexing
- Parameterization

Subroutines are programs designed to be used by other routines to accomplish a particular purpose. These routines can be called into action from numerous points within the main body of the program. In microprogramming, subroutines are also used. This is becuase many microprograms contain similar or identical sections of code. For example, many memory reference instructions in a computer system all use the same logical sequence in generating the address for an instruction, and therefore, this sequence could be a subroutine called from within a body of code which executes the addressing algorithm.

Indexing is a technique used in programming to locate data within a memory and to count the number of times operations are performed. Indexing is frequently used to point to a data item in a list of data words. Indexing techniques can be used very effectively in microprogrammed implementations. For example, they can be used to count the number of times an inner loop in a multiply instruction is traversed. Also, modern computers frequently contain register files. Operations are performed between strings of data in these files. Indexing is extremely useful in scanning these files.

Parameterization is a technique of storing parameters which characterize the state of program. This is sometimes accomplished by storing these in program status words. Information in these words can be tested and actions initiated based on these parameters. In microprogrammed controls similar techniques can be used. Parameters which characterize the state of the control portion of the system can be set and tested by the control processor in the same way that overflow, carry, less than, etc. indicators can be tested in some of today's computers.

Knowledge and experience in programming in assembly language is helpful in both designing and programming microprogrammed devices. Well designed microprocessors will begin to incorporate more and more features that will make commonly used assembly language programming techniques easier to employ.

Figure 5 shows a simple microcontrol for a system. It more closely represents one you would find in practice today. The two sections of the system are clearly in evidence. The one set of outputs used to control the data paths is labeled data path control and the other set of outputs used in determination of the next address is fed into a logic network where it is combined with status information from the data paths and then used to select the next address. The information in the data path control section of the ROS will, for example, gate data from the various registers into the arithmetic unit, select the function the unit will perform on the data and gate the result into the appropriate register.

MICRO CONTROL USING ROS

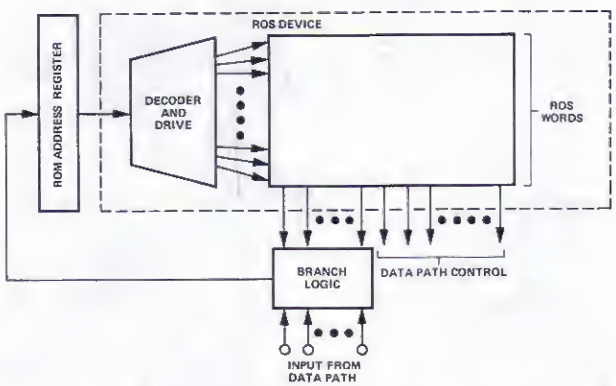


FIGURE 5

Figure 5 represents a control section similar to the one found in many large computer systems. Typically, for a large system the ROS would contain a few thousand words, 50 to 150 bits in length. The ROS will, in general, be accessed once for each basic control cycle of the device. For example, if the basic machine cycle is 150 ns, then one ROS access would usually be made during each of these periods. For reasons which will be discussed later in the section on timing, it is highly desirable to have the ROS read cycle as small a fraction as is possible of the basic

machine cycle. This gives the system the maximum amount of time to select the next microinstruction.

The data path control portion of the ROS and its functions are easily understood. The example presented here is from a paper by Tucker. He presents a look at a simplified portion of the arithmetic unit of a particular System/360. Figure 6 shows an arithmetic system with three 32 bit registers – T, A, and B and a 56 bit arithmetic unit to add the contents of these registers. Also represented in this figure are other gating functions which can be used to control the data path. For example, by applying certain signals from the ROS, it is possible to cause data coming into the adder to be complemented, transmitted uncomplemented (true), and shifted to the left one or two positions. Also, the shifter at the output of the adder can be programmed to shift data to the left or right four positions or transmit the data on through. On a single machine cycle, there is time to gate the data from the register through the logic on the input to the adder, perform an addition, post shift the data and then store the result back in a specified register.

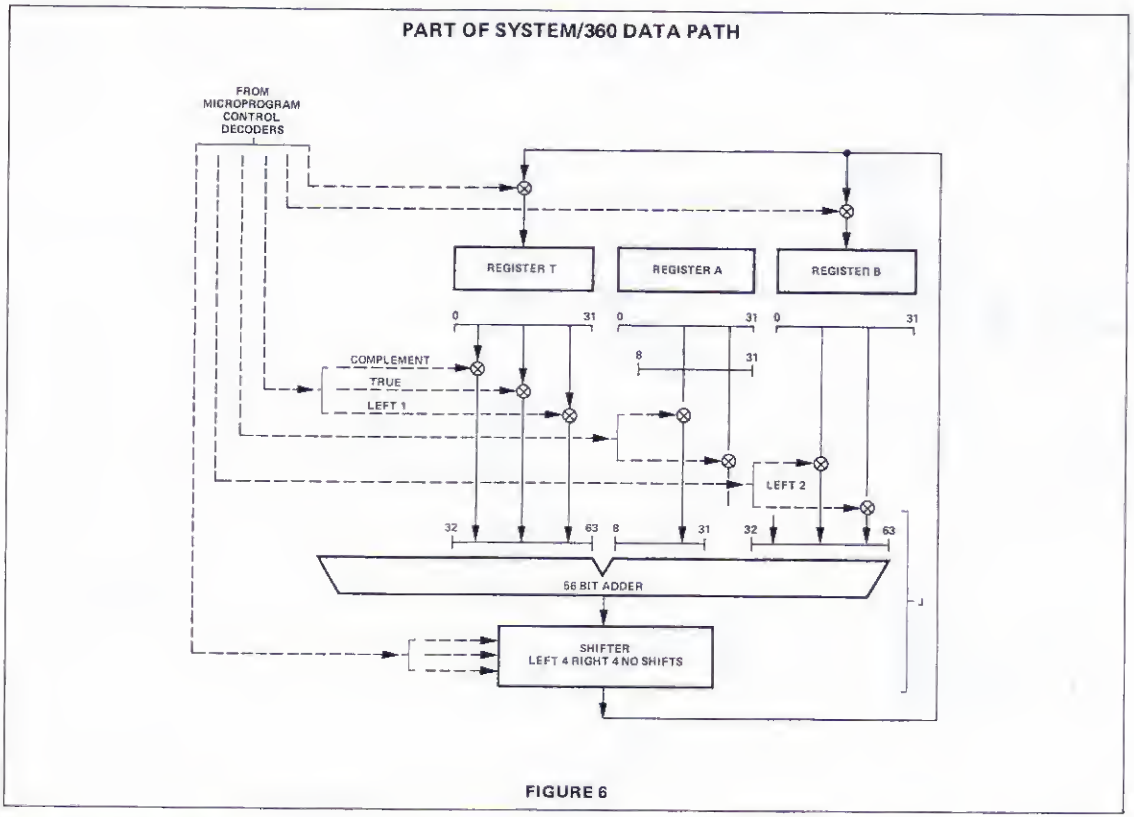


FIGURE 6

TERMINOLOG REVIEW

- The operations making up a single step are called micro-operations.
- A collection of micro-operations executed in one basic machine cycle is a microinstruction.
- A sequence of microinstructions is a microprogram.

Numerous small systems have been built using microprogrammed techniques. Figure 7 shows two microinstruction formats for small computers. Figure 7a is one of the instruction formats used on the Interdata Mod 4. The opcode field specifies the function the arithmetic unit will perform on the inputs to the unit. One input to the ALU (Arithmetic and Logic Unit) is the register addressed by the S field. The other is the AR register. The results of the operations are placed in the register designated by the D field. The second format is one used in the Micro 800. In this format the opcode specifies an operation which will be performed between the designated file register f and the contents of the memory buffer register. The results of the operation can also be stored simultaneously in a second register, designated by the R field which is used primarily in control of the microprogrammed device. If the bit designated by an * is "one", the result of the operation is inhibited from being placed in the register designated by the f field. The C field controls certain instruction options; for example, certain C codes will force a one into the least significant bit of the adder.

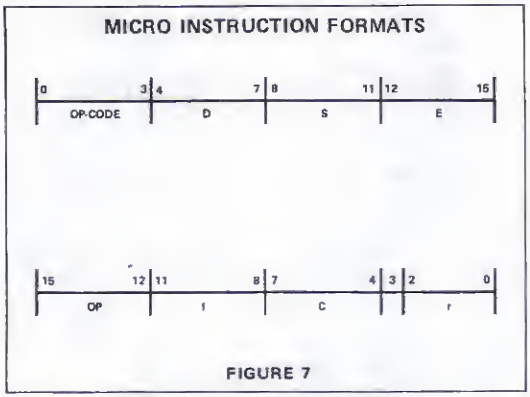


FIGURE 7

One way to control the data paths in a machine is to have one ROS control bit for each data path or data path option. For machines with complex data paths such as the System 360/65 this would require approximately 250 bits for the arithmetic unit alone. This would be wasteful of ROS bits. As a matter of fact, since many of the micro-operations are mutually exclusive, most of the bits in such a ROS word would be "zero" assuming "zero" meant no operation would be performed. The obvious technique for reducing these bits is to use a more sophisticated coding scheme. By properly grouping mutually exclusive operations, the number of bits can be greatly reduced. For example, certain MSI arithmetic units perform 32 arithmetic and logic functions on input data. They require a five bit input code to specify the operation and not 32 input lines, only one of which would be true during any microinstruction. Basically, a careful search of the various micro-operations must be performed in order to select which of these can be coded together.

It is worth noting that designers today are overly conditioned to saving bits of ROS just as they were for years overly concerned about saving flip-flops and gates. Dramatic ROS breakthroughs such as the SMS 4096 bit ROS will have a significant impact on this thinking, primarily because ROS costs have decreased and because of the increase in ROS density.

It is easy to envision designers using longer and longer ROS words as the cost of ROS decreases eliminating the need for deciding networks on the output of the control memory.

The branch logic and the section of ROS devoted to determining the next instruction is the other critical portion of a microprogrammed system. In a simple microprogrammed device, each instruction could contain the address of the next microinstruction to be executed. For example, if there was a 4096 word ROS, each microinstruction could contain a 12 bit address to designate the next instruction. The advantage of such a scheme is that no program counter is required for the microprogrammed system. The output from the ROS can be gated directly into the address register to select the next instruction. Conditional branch instructions in a system such as this are implemented in the branch logic network. For example, one technique would be to require one target word in a conditional branch always have an even address. This word would always contain a zero in the last bit. To skip the next instruction, one need only "or" the condition tested for into the last bit. Thus a jump to the next odd numbered location would be forced. Other techniques would be to include a second address with each instruction word for conditional branching.

The important point to grasp at this time is how the technique works. The remainder of the application note will be devoted to suggesting practical techniques for microprogrammed implementations. Whether or not a system is economically implemented with microprogramming techniques depends on how cleverly the system designer implements the coding of ROS words and the selection of next microinstruction words. The trade off designers are faced with, is the longer, within reason, the microinstruction word is, the more expensive the ROS is, but the simpler the rest of the machine logic becomes. As ROS becomes less expensive, the tendency will be to use long ROS words to save random logic. The true benefit of LSI will be obtained by using regular arrays such as ROS, and using low cost ROS bits somewhat inefficiently in place of random logic arrays. This is similar to the situation which took place when IC's were introduced. The cost of logic became so low it was desirable to use more logic and save time than concentrate all one's attention on minimizing the number of gates.

In every microprogrammed device there must be some logic which controls the ROS and does the basic system timing. The complexity of this logic depends to a high degree on the microprogrammed implementation. In a microprogrammed device with short ROS words where very few bits in the microprogrammed instruction word are devoted to determining the next instruction, the control logic will become fairly sophisticated. In these systems a ROS program counter will generally exist and the control logic will ensure the next ROS control word is selected by augmenting the program counter by one just as the program counter is augmented in a typical computer system. In microprogrammed devices with longer words, the control will be conceptually simpler. For example, if each instruction might contain the address of the next instruction, and then there would be no need for a program counter, only a ROS address register.

Figure 8 shows the timing in a typical microprogrammed system. The first set of timing pulses strobes the output from the ROS into the output buffer register. This register will exist in higher speed systems because of the desirability of overlapping the access for the next microinstruction with the execution of the current one. In slower systems, the output of a semiconductor ROS can fulfill this function since it is a DC output, not pulsed as in the case of magnetic E core or capacitive type ROM. Furthermore, since the output of ROS, such as the SMS 4096 ROS, can in some cases drive ten TTL typical loads, there is little need to provide extra output drive.

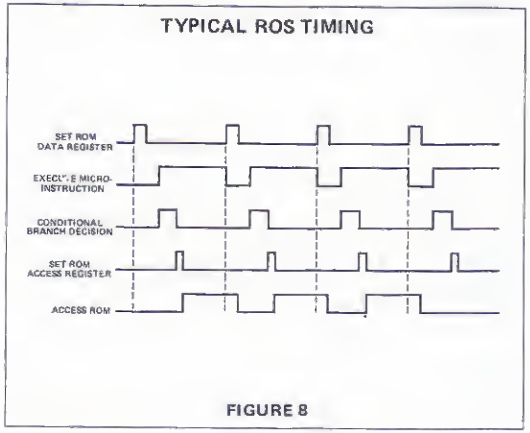


FIGURE 8

As soon as the output buffer has settled, the execution of the microinstruction can begin. This is indicated in the second line of the timing diagram. The execution time will be long enough to permit the most basic microinstruction execution to take place. However, some of the longer operations might take two or more microinstruction times to execute. For example, suppose the time to gate data from source registers to the adder and perform an "add" is 300 ns. If the basic microinstruction cycle is 150 ns, then an add operation could require two microinstruction times. This could be accomplished by executing the same microinstruction twice with the one exception that data would not be stored in the destination register until the second instruction is executed. Another way to handle long instruction execution times is to let the microinstruction have a bit or bits which will be used to extend the microinstruction execution time. Still another obvious way for simpler systems is to merely let the longest instruction dominate the timing. For example, of 300 ns is the longest register-to-register cycle time, then the basic cycle could be selected as 300 ns. In general, any system will have certain microinstructions which require several basic machine cycles. For example, a fast microprogrammed device may be hooked to a slow core memory which as an access time of 800 ns compared with a basic microinstruction execution time of 200 ns. Having some interlocks which enable this type of delay to be conveniently accommodated is desirable.

The fourth line in figure 8 shows the time at which the ROS address register is loaded. This timing pulse will clock the output of the branch logic in figure 5 into the ROS address register. If a conditional branch is going to be executed, the logical decision must be made during the time shown in line 3. Obviously, this is not always possible. For example, if a branch is to be made on overflow, probably the information will not be developed until too late by the adder to enable a branch decision to be made for that instruction. Consequently, one instruction and one instruction execution time is lost because the branch decision must be made on the next instruction.

The fifth line of the timing diagram shows the time devoted to the access of the ROS. One reason for the importance of fast access in the ROS can now be understood. The shorter the access time the more time is available for making decisions. Since a high percentage of microinstructions contain conditional branches, many instructions and instruction times can be saved by making this time as small a percentage of the basic control cycle as is possible.

There are obviously many variations of the timing schemes. The timing technique must be selected to match the application and the objectives of the designer.

PRACTICAL MICROPROGRAMMED IMPLEMENTATIONS

The microprogramming art is today evolving at a rapid rate. Whereas a few years ago only a few machines employed this technique, today it is used throughout the IBM 360 and 370 series, in both the CPU and peripheral controllers, in the RCA Spectra 70 series, in the Honeywell 4200, in the Interdata Mod 4, Micro 800, etc. Numerous other manufacturers are designing the next generation of equipment, both controllers and processors, using this technique.

Inspection of the architecture, design techniques and memory devices used in existing implementations provides the practical engineer with a bewildering array of techniques, ideas and practical design tricks. Most of these approaches exist for good reasons. They provided the designer with the best set of economic trade offs in meeting his objectives.

The remainder of this section of this application note will be devoted to reviewing some of these techniques and explaining some of the reasons why these techniques are useful and what motivates a designer to select one of these approaches.

ROS ADDRESSING TECHNIQUES

Wilkes' basic implementation shown in figure 1 generated the next address to read out the next microinstruction directly from the output of the B matrix. Therefore, if there were 1024 words of ROS, the output from this matrix would be a 10 bit code used to designate one of these words. While this technique is adequate, it fails to couple the microprocessing device in a tight fashion to its external environment and leads to an inordinately long response to an input stimulus. To see this, consider the problem of interpreting a 5 bit code and branching one of thirty-two points determined by the code. This is the type of operation which occurs in interpreting the operation code of a computer, terminal, or peripheral instruction. In the Wilkes model, each bit must be tested separately and a branch must be taken at each step. This involves 5 separate tests, one for each bit and 31 branch type instructions in a decision tree, plus an additional 32 branch instructions to get to the starting point of the various routines.

Wilkes' group suggested introducting multiple address sources. This greatly simplifies and speeds the solution to the above problem. To see this, consider the ROS address register shown in figure 9 where the bits R_i are output from the address selection section of the ROS. Consider the bits S_j as bits from another register, for example, the instruction register in a computer. In order to interpret a 5 bit code, one need only let the bits R_{11} to R_5 select the starting address of a table in memory which contains 32 starting addresses of ROS sequences. The bits S_4 and S_0 could select any one of 32 entries in this table which could direct the microprocessing element to the proper location. Instruction decoding could, therefore, be accomplished with one microinstruction.

TWO ADDRESS SOURCE FOR MICROPROCESSOR ADDRESS REGISTER

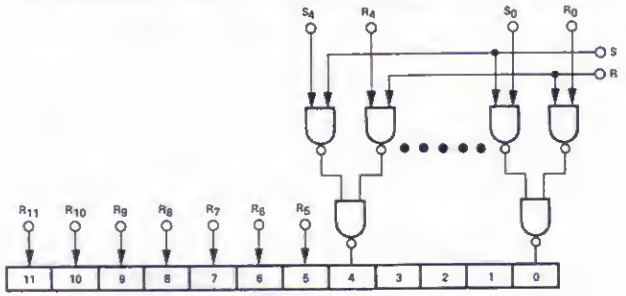


FIGURE 9

The importance of this technique goes far beyond the concept of instruction decoding. Any set of conditions could be introduced as an input in the low order bit positions and therefore, this represents one technique for developing a fast response based on the status of the external environment. For the example above, any one of 32 alternative courses of action could be taken in response to an input. This action could be initiated in one microinstruction cycle instead of six, meaning a much faster response time. With today's semiconductor memories, microprocessors with 100 ns cycle times are easily constructed meaning a response to an external environment can begin very quickly. Furthermore, this technique saves 31 ROS locations.

It is obvious that this technique can be extended and rather than truncating the second address source, the address source could be extended to encompass the entire address field. One possible choice is to externally introduce the full starting address of the response routine. This eliminates the need for storing a jump table in the ROS, but may greatly complicate the external address circuitry. Speed of response can potentially be obtained by eliminating the first search cycle and substituting for it the time required to do the external address generation. One device which does an excellent address generation job is another ROS. Figure 10 shows such a scheme in which the external input conditions are used to address a ROS which generates the proper starting address. The source of the address is selected by either the S_a or R_a address source lines.

MICROPROGRAMMED ROS ADDRESS GENERATION

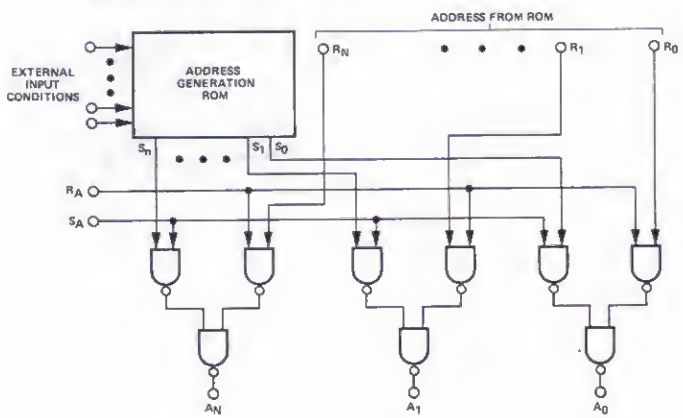
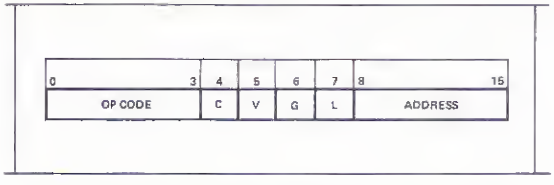


FIGURE 10

The addressing schemes discussed to this point all assume that the complete address is generated externally. Since microprograms in general execute instructions sequentially, a program counter can be used to select the next instruction in sequence. Gerace proposed this type of scheme where the ROS address register could act as either a counter or as a device which was loaded by data externally.[4]

A potentially more useful generalization of Gerace's scheme is to permit the address register to count up and down in steps of ±1, ±2, or ±4, as well as being externally setable. Whether this ability is useful or not to the system designer depends on the remainder of his microprocessor structure. Frequently one desires to go around a loop of instructions a number of times. For example, one might be transferring 128 characters of data to an output device or performing a multiply instruction. In such instances, sequences of two to five instructions may be frequently used and counting the address register down by −1 permits a two instruction sequence, by −2 permits a three instruction sequence, etc.

The existence of a ROS program counter carries with it the implication that the next instruction will be selected automatically unless something is done to override the procedure. This of course introduces more external circuitry; however, it can potentially save large numbers of ROS bits. Obviously, if the next address is selected by a counter, there is no need to have these bits presented at the output of the control store except when an out of sequence address is desired. Microprogrammed devices which use this technique, in general have jump instructions similar to those of a conventional computer in which one portion of the microinstruction will be interpreted as the next address for the control store. Figure 11 shows the branch instruction format for the Interdata Mod IV. A branch can be taken to any one of 256 locations depending on the test conditions C-Carry, V-overflow, G-Greater than, and L-less than zero. In the Interdata Mod IV, the absence of such an instruction, or the execution of a microinstruction of the format shown in Figure 7a, causes the ROS program counter to be incremented by one.



Saving ROS bits to specify addresses can also be accomplished by truncating the address field emitted from the ROS. To a much greater extent than in a conventional computer, most microprograms are short and involve operating on data or using program segments which are quite near in an address distance sense. For example, many program sequences will be less than 8 words and most less than 16. This means for a great majority, the next instruction selection can be specified by a relatively few bits from the ROS, the rest of the bits already being present in the address register. Therefore, it is not uncommon to find next address fields which are 4 to 6 bits in length. Obviously other instructions are required to branch outside this restricted field. In a 2048 word ROS going to a 5 bit truncated address saves on the order of 10 thousand bits.

If a truncated address scheme is used, care must be taken to ensure one does not try to jump across page boundaries with a truncated address. For example, if one wishes to use a 6 bit truncated address, the next instructions selected by that address would have to be contained within a 64 word page. Addresses outside the page would be reached through a more global branch type of instruction or technique. This could be specified by selecting a different instruction format.

Microprogrammed devices are sequential logic circuits using ROS, which within constraints of time can be used to simulate the performance of any sequential logic network. The simulation process is referred to as emulation. The ability of the device to emulate effectively is determined to a great degree by the address selection or sequencing portion of the unit. From the numerous alternatives presented here, some reasonable variation must be selected which meets the objectives of the designer. In microprogrammed devices with short microinstruction words, this usually involves combining a program counter technique with a global branch instruction format. In larger systems truncated addressing schemes are more frequently used.

MICROINSTRUCTION WORD ENCODING

If bits of ROS cost nothing, the simplest machine configuration would be to use one output bit from the control store to control each gating path. To conserve bits of ROS, the control signals, as was discussed earlier, are encoded. For example, eight gating paths may never be used at the same time and therefore, one three bit field can be used to designate the desired gating path. This three bit field is fed into a decoding network whose outputs control the data paths. The designer must select sets of mutually exclusive operations. In many cases the choices are obvious. For example, the adder network may perform only one function at a time and therefore, it is reasonable to encode the inputs to the adder network which select the function. If too many mutually exclusive gating functions are encoded together, the cost of the decoding network at the output of the control store and the delay through that network are prohibitively large. These trade offs can be made by careful study of the problem.

In large systems, speed is attained by allowing many operations to procede simultaneously. The greater the degree of simultaneity, the fewer the number of mutually exclusive gating operations. The obvious consequence is to cause words of control storage to become longer. Consequently, in machines such as the IBM 360/85, a computer with a great degree of simultaniety, 128 bit control words are

used. In small systems, multiple use is made of bus structures rather than provide multiple bus structures. Control decisions are made sequentially and therefore, shorter ROS words can be used. One frequently used technique in small systems is to have a number of different instruction formats. Each of these formats will generally be dedicated to one major type of operation. This greatly reduces the length of the ROS words but also slows down the system performance. For example, in short word length microprogrammed devices, one instruction will be used to add two registers, a second to test the result and a third to branch to a location based on the result of test. Each of these instructions might have a different format whereas in a longer word length control store this would be accomplished in one microinstruction word.

The Micro 800, which is a small microprogrammed device, uses three instruction formats in order to conserve ROS bits. These are shown in figure 12. The literal format is designated by placing a hexidecimal number in the range 1 to 7 in the most significant hexidecimal digit position; the operate format is designated by placing a hexidecimal number in the range from 8 to f in the same position and the execute format is designated by placing an ϕ in the first digit. The literal format is used to introduce constants into the system, perform operations between the literal and a designated register and to implement global jumps.

INSTRUCTION FORMATS FOR MICRO 800

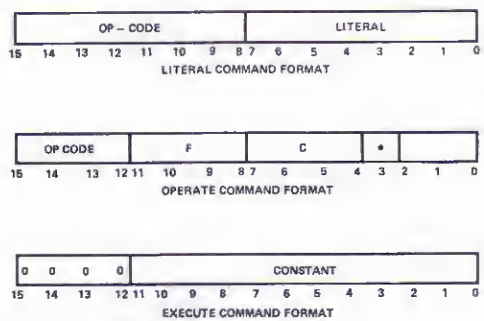


FIGURE 12

The process of introducing constants into the system from the output of the control store is a frequently used technique in almost all microprogrammed systems. The field in the control word which does this is called the emit field. Output from the emit field is frequently used in the Micro 800 to set up control registers and introduce data into the working registers. The operate commands are used to perform arithmetical and logical operations between the file registers (f) and source register. The C field is used to control certain options such as introducing a 1 into the low order carry of the adder, etc. The r field is used to transfer the result of the selected operation to certain control registers. Thus the result of an arithmetic or logical operation can be performed between a file register f and another source register and the result stored in both the file register and a control register.

The * bit is used to inhibit storing the result in a file register. The final format, the execute format, is used in conjunction with another register to generate microinstructions. The technique employed permits indexing operations to be performed to access data from the file registers.

MISCELLANEOUS TECHNIQUES

There are very few techniques that have been widely publicized for writing efficient microprograms or developing efficient microcode. A few of the more frequently used techniques discussed earlier which are finding application in microprogramming are:

- Indexing
- Subroutines
- Paramaterization

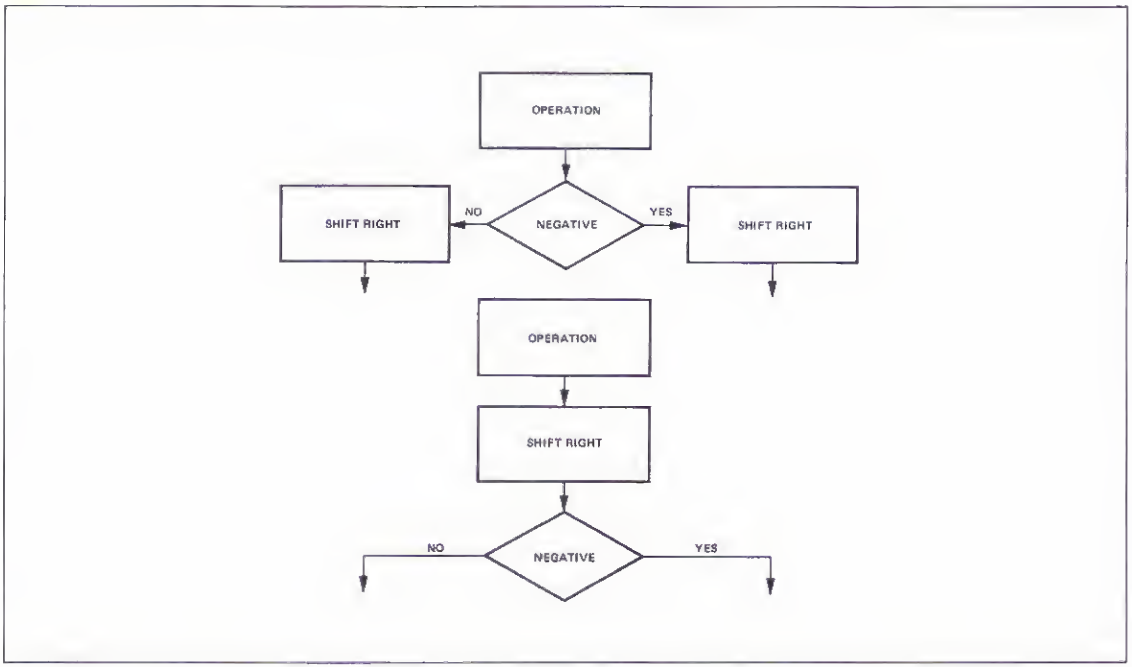
Many arithmetic operations are made up of a sequence of repetitive operations. For example, a multiply is made up of a sequence of adds and shifts. This sequence will be executed over and over again until the operation is completed. Index registers have been used in computers to count the number of times one goes through a sequence of instructions. The same technique is applicable to microprogramming.

More and more devices are being designed with local stores. These stores are memories used in the implementation of register files, general registers, channel control words, etc. In many instances, the arithmetic unit will process only small sections of the word stored in the local store. For example, several systems use 32 bit words but have 8 bit arithmetic and logic units. In these cases an indexing type function can be used in a fashion identical to their use in computers where they are used to both address data and count the number of operations on the data.

The use of subroutines in computer programming is well known and well understood. Frequently many microinstructions can be saved by using subroutines and using sections of microcode as subroutines in many different programs. If this is to be done, a provision must be made for storing and restoring the current address for the ROS. Many techniques for accomplishing this are known. In many microprogrammed systems this will be accomplished by placing the output from the address register onto one of the data buses where it can be stored in a register. This temporary storage register can then become one of the address sources for setting the ROS program counter.

As discussed earlier, parameterization is a technique of recording parameters which characterize a system in storage elements such as status bits. Status bits are frequently used in information processing systems to store information

about the conditions of the device. For example, in a computer system these bits will hold information about whether the result of the last arithmetic operation was positive or negative or whether an overflow occurred. Frequently, program words can be saved if it is possible to set certain bits based on a condition of the network and then test these bits at subsequent instruction times. Microprograms can frequently be shortened by the use of status bits. Tucker points out that branches in the microprogram frequently can be made a number of instruction cycles after the status bits are set. This eliminates premature branching and the unnecessary duplication of microinstructions. For example, suppose a microprogram requires a correction cycle if the result of an operation is negative, and also requires the data be shifted right independent of the result. If the information about the negative result is stored in a status indicator, the shift right can be performed and then a branch taken on the basis of status. If no way exists to store the condition, a branch must be made immediately. This means that both the routines for the positive and negative result will have to contain a shift instruction. This situation is illustrated in figure 13. In figure 13a, the shift is performed after the branch and hence, a 4 word sequence is required, while in figure 13b, the test for negative is performed after the shift, and requires only three words of code.



Frequently, microprograms have segments which differ by one instruction from program to program. For example, the shift right and shift left instructions in a computer might have microprograms which were similar in every respect save for the one instruction which performs the shifting. For this reason, it has been often found convenient to store bits external to the ROS output register which contain codes to control the arithmetic unit. The technique could be used in other areas of control. The emit field of the microinstruction can be used to place data in this register which is sometimes called a function register. For example, the logical shift and arithmetic shift right instructions of a computer might all call the same subroutine to perform the repeated shifts making up the instruction. However, the function performed by the arithmetic unit might differ greatly for each of these instructions. For example, in some cases, "zero" might be introduced in the most significant bit position, while in other instances, "one's" would. If the microprogrammed portion of the system contained a function field, then the function of the arithmetic and logic unit could be made different for these different cases but major portions of the code could be preserved.

As discussed in the section on timing, branch decisions must be made early in the microprogrammed control cycle so the next word can be read from memory. The decision time can be increased by having a control store with faster access. One way to speed up the apparent access time to the control memory is to phase the access to them. This technique and its application to the RCA Spectra 70/45 has been reviewed in Husson's recent book. Variations of this technique may find greater use in semiconductor memories because the address circuitry is so inexpensive and therefore, it is relatively inexpensive to provide multiple or

phased accesses to a system. Suppose one was willing to include two truncated addresses in each microinstruction, and suppose further that the memory was organized with odd numbered words in one bank and even numbered words in the other. If one enforced the restriction that multiple branches must always be made to one even and one odd address, the result would be that two target words could be accessed simultaneously.

In SMS memory products the access time from chip enable to output is a fraction of the total access time. Therefore, a decision can be made at the last instant as to which memory bank will be enabled and the data will appear at the output register with very little delay. This technique avoids wasting a control cycle on a two way branch.

WRITEABLE CONTROL STORAGE

One of the most significant trends in computer system architecture today is the replacement of ROS in the control store with random access storage (RAS). Writeable control storage is the name given to read/write memories used in the control portion of a system. The trend is significant because it enables the system designer to change the external characteristics of the system. For example, a computer can have several different control programs, one of which makes the computer be compatible with the IBM 360 series; another of which lets it emulate the performance of an IBM 709, and still another which can be used to emulate the performance of a Honeywell 200 system. The process of using control storage in a host machine to give that machine the external characteristics of another device is called emulation.

While microprogrammed devices can be used to emulate numerous different systems, the inclusion of certain specific hardware features will greatly influence the performance of the host machine in doing emulation. Many of the host microprogrammed devices are so tailored to a specific target architecture that they are relatively ineffective at emulating any other structure. Fortunately, the computer industry as it has matured has begun to standardize in many ways. This makes it easier to emulate a wide variety of machines in a single host machine. Probably the most significant trend in this respect is the move toward using computer words composed of an integral number of 8 bit bytes. In the past a number of serious emulation problems were caused when one tried to emulate 36 bit word length computers on 32 bit machines.

Writeable control store leaves the design of the system open-ended. It is possible to add features or add emulation routines after the hardware design is frozen. Even though the WCS is more expensive than ROS implemented store, the flexibility provided the designer makes this trade off worthwhile. The basic reasons are that:

- It becomes a simple problem to correct errors in the implementation of the device.
- A large library of control programs can be loaded on demand.

The first point is perhaps obvious but it deserves a few comments. As systems become more and more complex, an increasing number of design errors are discovered after the system is installed. Prior to the introduction of WCS, these changes were made by physically making wiring changes in the field or by replacing portions of the hardware. With WCS, many of these repairs can be made by distributing a new control program and writing it into the control store. Since machines using WCS have hardware control store loaders, this is very simple to do. For example, in the IBM 360/25 the control store can be loaded through the card reader by enabling a special loading mode with a switch.

It is highly desirable to be able to load any one of a number of library programs into a control store. The machine can then use a small amount of control storage to perform a number of different emulation or operations in sequence. For example, a computer running in a time-sharing, batch and remote batch environment might want to emulate the performance of an IBM 1401 for a batch problem. It could do so and then change its control store and operate as a Honeywell 200.

In the IBM 360/85 diagnostic routines are executed from the WCS. There are 30 sections of non-resident diagnostics, each section of which contains a maximum of 512 words. Since WCS is used, only 512 words of storage are needed to execute all diagnostics. Diagnostics executed from control store can be much more specific than those implemented at the machine language level. They can test small segments of the machine and they can run with smaller portions of the system operational. This is especially desirable on larger systems since the larger the system, the greater the probability that it will not be running and the greater the probability that the basic structure required to run any diagnostic will not be operational.

The application of WCS will not be limited to large systems. Terminals offer a particularly attractive area for the use of WCS. A large number of terminals will be multifunction devices and used in numerous different applications. By using WCS, local control can be put in the terminal to tailor its characteristic to the application. Furthermore, one of the key problems in terminal system design is to diagnose failures precisely and separate machine failures from operator errors. WCS will facilitate the diagnosis of failures. Diagnostic programs can be loaded either from a remote source or locally. Diagnostic routines can then develop fairly precise information about the system malfunction.

One of the most serious difficulties encountered in the use of WCS is the control of undesired access to the memory. Unless care is taken to limit user access, the key has been provided to Pandora's box. Many technical articles have waxed eloquent on the dangers which have failed to materialize in fact. However, some danger does exist which can be best controlled by having well defined policies and possibly denying the user access to certain points in the system. Certainly uncontrolled creative improvements to

properly functioning systems can present the service engineer with an opportunity to solve problems of significant magnitude.

THE ADVANTAGES OF MICROPROGRAMMING

In the introduction to this note, a number of statements were made about the advantages of microprogramming. After discussing the technique, a background has been established against which to test these statements.

- Reduction of random logic and a resulting more structured organization.
  The control portion of non-microprogrammed digital systems is generally quite random. It contains counters, special flip-flops, decoding networks, etc. In microprogramming, a regular memory structure replaces most of this. The randommess still exists in the system but it does so in terms of random data stored in the control memory. The organization does indeed become more structured because fewer alternatives exist for implementing functions. Lots of flip-flops, etc., have beer removed.
- Emulation of a number of devices can be carried out by a single general purpose device.
  There are numerous practical examples of this. One is the System 360 in which certain models emulate the IBM 1401 and others the IBM 709. Some companies which must design a number of peripheral controllers have decided to design one more general purpose device and adapt it through microprogramming to a number of devices. In this case, the host controller emulates the performance of a number of special purpose controllers.
- Diagnostics and service aids may be easily implemented in the control portion of the system.
  Some very small systems store their diagnostics in ROS control store. Many models of the IBM 360 also do and this trend will spread. One of the main problems with most system diagnostics is that too much of machine must be running to run the diagnostic. Furthermore, computer instructions tend to check fairly large portions of the machine and therefore, it is difficult if not impossible to precisely pinpoint faults. In many instances, there is no way to check out the functioning of specific portions of the internal control network.
  Microprogrammed implementations are truly oriented toward servicing and diagnostics. For example, large portions of the control network can be checked by putting parity on the output of the control store. Furthermore, the microporcessor can both set and test internal control states not available to the machine language programmer.
- Field changes can be easily made by changing microprogrammed stores.
  Field changes to correct logic errors in computer systems have become increasingly difficult to make because of the trend toward functional electronic packaging where the circuit interconnections are made on the PC card. It is very convenient to make changes in WCS and if the control memory is implemented in ROS to swap out portions of it. Indeed, as systems become more and more sophisticated, there are going to be fewer individuals capable of installing field changes properly and there will be a tendency to rely more heavily on either total subsystem replacement or changing of control programs.
- Special purpose adaptations can be made of the device by changing a few program words.
  Just about every system designer is faced with the selection of devices which would be perfect if only this or that feature were present in the basic structure. Microprogrammed devices are inherently open-ended and features can be easily added to adapt the device to the environment. For example, one manufacturer of a microprogrammed system offers the customer special options to make the system operate in a communications environment. In this way, the system can be tailored to the environment.
- Performance can be economically expanded at lower cost than in a conventional system.
  For very simple systems, conventional control logic is an economical way of implementing a design. As the complexity of the system increases, the cost of the control logic increases at a fairly rapid rate. In microprogrammed implementations, the cost of the simplest system is somewhat higher but adding features only requires the addition of more control memory and therefore, the cost of adding features relatively small.
  In fact, the low incremental cost for adding features was one of the primary motivations for selecting microprogrammed inplementations of the System 360. Because of this, it became possible to put very complex sets of instructions into small versions of the System 360, which made product line compatibility easier to achieve.
- Final system definition can be posponed to a later time in the design cycle.
  As people use and work with a design, ideas always come up about ways to improve it. Worse yet, it is frequently discovered that significant portions have been left out. As long as the basic system structure is sound, additions and changes can be made by changing the control store. The cycle for doing this can be very short. Furthermore, the effects on system hardware documentation are minimal since only a control program is changed.
- Documentation and service training costs can be reduced.
  Certainly the most difficult portion of a system to document and train service engineers on is that portion which contains random logic. By reducing the amount of random logic, this job is similarly reduced. Furthermore, the service engineer is dealing with the same basic structure programmed in a number of different ways. In a random logic network, he must learn both about the network sequencing as well as the structure for each option.

CONCLUSION

Most people recognize the significant advantages that can

be obtained using a microprogrammed approach. With the advent of semiconductor memories, both ROS and RAS, a truly satisfactory component has been found to implement the control store for microprogrammed systems. Undoubtedly, these developments will motivate a broadly based trend to implement new devices in this fashion.

A new class of software system designer is going to emerge. He will design and implement the system control algorithms. Many of the jobs once performed by the logic designer will become the province of these highly skilled microprogrammers.

MICROPROGRAMMING AND SYSTEM APPLICATIONS FOR READ ONLY STORAGE

INTRODUCTION

The development of large low cost and fast semiconductor ROS (Read Only Store) will have far reaching effects on the computer industry. The critical breakthroughs made in the design of these devices now make it economically feasible to use read only memory to realize even the simplest logic functions. In the near future, microprogrammable devices using ROS as a control memory will replace many sophisticated logic systems. The technological advances in ROS that make this feasible for the first time are:

- Sub 100 nanosecond speed which is required to make logic networks react quickly.
- Substantially lower cost per bit.
- Extremely high bit densities at very low power levels which mean microprogrammable devices will use less PC board area and consume less power than non-microprogrammable units.

The SMS 4096 bit bipolar ROS represents a significant advance in the state-of-the-art and will accelerate the trend to wider use of ROS.

HOW READ ONLY STORES ARE USED

There are four major application areas for ROS. These are:

- Table look up – where a code conversion or transformation is performed by using the input code to address the ROS and reading out the transformed data.
- Pattern generation – this is really a special form of table look up where an input code is used to address a memory location containing the desired pattern.
- Program storage – several small computers currently use ROS in place of conventional read-write storage to store programs which are to be permanently made a portion of the computer's operation.
- Microprogrammable devices – where read only store is used as a control memory to control the function of logic networks.

TABLE LOOK UP

Table look up techniques are frequently used when it is desired to determine the value of a function quickly. For example, the value sine of an angle can be quickly derived by using the binary expression of θ to address a word of memory containing the sine of the desired angle. Another frequent use of table look up ROS is for code conversion. There are a number of commercially available code converters which convert ASCII (American Standard Code for Information Interchange) to EBCDIC (Extended Binary-Coded-Decimal Interchange Code) and EBCDIC to ASCII. The EBCDIC code is shown in figure 1 and ASCII in figure 2. In a 512 X 8 word ROS this code conversion can be carried out by using the first 256 words to convert ASCII to EBCDIC and the second 256 words to convert EBCDIC to ASCII. Figure 3 shows an example of this type of code converter. A 4096 bit ROS makes it possible to do this code conversion with a single integrated circuit.

EXTENDED BINARY-CODED-DECIMAL (BCD) INTERCHANGE CODE

Bit Positions → 01 / 23 / 4567

	00	01	10	11
0000	NULL			
0001				
0010				
0011				
0100	PF	RES	BYP	PN
0101	HT	NL	LF	RS
0110	LC	BS	EOB	UC
0111	DEL	IDL	PRE	EOT
1000				
1001				
1010				
1011				
1100				
1101				
1110				
1111				

01	00	01	10	11
	BLANK	&	–	
			/	
	.		,	"
	?	!		:
	.	$	;	≠
	←	*	%	@
	(	)	⁀	'
	+	;	–	=
	∓	¢	±	√

10	00	01	10	11
	a	j		
	b	k	s	
	c	l	t	
	d	m	u	
	e	n	v	
	f	o	w	
	g	p	x	
	h	q	y	
	i	r	z	

11	00	01	10	11
	>	<	‡	0
	A	J		1
	B	K	S	2
	C	L	T	3
	D	M	U	4
	E	N	V	5
	F	O	W	6
	G	P	X	7
	H	Q	Y	8
	I	R	Z	9

FIGURE 1

8-BIT REPRESENTATION OF THE 7-BIT AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

Bit Positions 76 / X5 / 4321	00	01	10	11
0000	NULL	DC_0		
0001	SOM	DC_1		
0010	EOA	DC_2		
0011	EOM	DC_3		
0100	EOT	DC_4 STOP		
0101	WRU	ERR		
0110	RU	SYNC		
0111	BELL	LEM		
1000	BKSP	S_0		
1001	HT	S_1		
1010	LF	S_2		
1011	VT	S_3		
1100	FF	S_4		
1101	CR	S_5		
1110	SO	S_6		
1111	SI	S_7		

00	01	10	11
BLANK	0		
!	1		
"	2		
#	3		
$	4		
%	5		
&	6		
'	7		
(	8		
)	9		
*	:		
+	;		
,	<		
–	=		
.	>		
/	?		

00	01	10	11
		@	P
		A	Q
		B	R
		C	S
		D	T
		E	U
		F	V
		G	W
		H	X
		I	Y
		J	Z
		K	[
		L	\
		M	]
		N	↑
		O	←

00	01	10	11
			p
		a	q
		b	r
		c	s
		d	t
		e	u
		f	v
		g	w
		h	x
		i	y
		j	z
		k	k
		l	l
		m	m
		n	ESC
		o	DEL

FIGURE 2

EXAMPLE OF ASCII TO EBCDIC CODE CONVERTER

INPUT ASCII ADDRESS	ASCII CODE SYMBOL	EBCDIC CONTENT OF CORRESPONDING ROS WORD	EBCDIC CODE SYMBOL
X 7 6 5 4 3 2 1		0 1 2 3 4 5 6 7	
0 0 0 0 0 0 0 0	NULL	0 0 0 0 0 0 0 0	NULL
0 0 0 0 0 0 0 1	SOM	0 0 0 0 0 0 0 1	–
0 0 0 0 0 0 1 0	EDA	0 0 0 0 0 0 1 0	–
0 0 0 0 0 0 1 1	EDM	0 0 0 0 0 0 0 0	–
•			
•			
•			
1 1 0 0 0 0 0 1	A	1 1 0 0 0 0 0 1	A
1 1 0 0 0 0 1 0	B	1 1 0 0 0 0 1 0	B
1 1 0 0 0 0 1 1	C	1 1 0 0 0 0 1 1	C
1 1 0 0 0 1 0 0	D	1 1 0 0 0 1 0 0	D
•			
•			
•			
1 1 1 1 1 1 1 0	ESC	1 0 0 1 1 1 0 0	–
1 1 1 1 1 1 1 1	DEL	0 0 0 0 0 1 1 1	DEL

FIGURE 3

PATTERN GENERATORS

Pattern generators are just a special form of table look up devices. Today they are most commonly used to convert an input code into a video signal in order to generate alphanumeric characters on the face of a TV screen. For a limited character set, a 5 X 7 dot matrix provides adequate resolution. For a larger character set (96 to 128 characters) 7 X 8 and 7 X 9 arrays are used. In high performance terminals two 4096 bit stores can be used to generate ninety-six 7 X 8 characters and do EBCDIC to ASCII and ASCII to EBCDIC code conversions as well.

Figure 4 shows some dot matrix patterns for the characters A, W and Y. In most systems the last 3 bits of the address word are used to address the lines of the character and the first 7 bits are the character code. If vertical scanning of the characters is desired the patterns are rotated 90 degrees. There are, of course, numerous other character generation techniques. Some systems use a series of vectors and curves to write a character. This produces characters of slightly higher quality. In these systems the ROS can store codes used to direct the generation of character vectors.

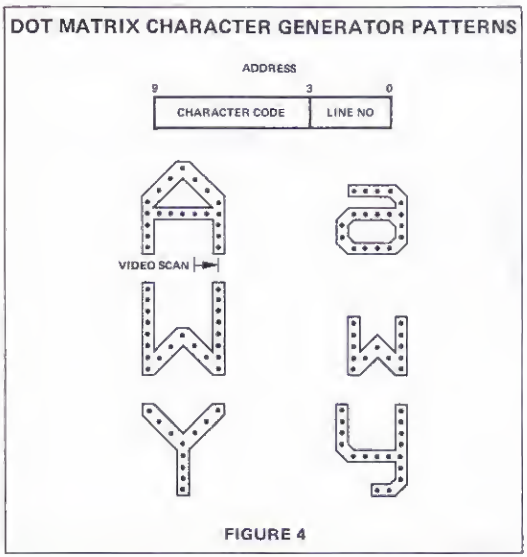


FIGURE 4

MAIN MEMORY APPLICATIONS

Contemporary computing systems do not require significant modification of systems programs stored in high speed main storage. Consequently these programs could be stored in read only storage. In the past ROS technology did not offer enough cost performance advantage to warrant its use. This obstacle has now been overcome. ROS is now being used in minicomputers for program storage. Its use will undoubtedly become more widespread for the following reasons:

- ROS speeds now are ten times faster than core storage speeds and computer systems are being designed with asychronous memory buses so they can take advantage of this speed.
- The cost per bit of ROS is significantly less than the cost per bit of much slower read/write memory.
- System architectures no longer are heavily dependent on physically modifying addresses of program words. The needed modifications are now carried out by indexing.

Now that 8192, 32 bit words of 60 ns ROS can be easily put on two printed circuit cards at costs below that of 1 μs core, there will be a trend to commit debugged portions of the executives, frequently used macros, portions of customer programs where high performance is desired, etc. to ROS.

MICROPROGRAMMING

M. V. Wilkes was responsible for introducting the term microprogramming to the computer industry. His objective in developing microprogramming techniques was to provide a systematic alternative to the usual somewhat ad hoc procedure used for designing the control portion of a digital computer. In recent years a number of equally cogent reasons have been set forth for employing microprogramming techniques. Several of these outlined by Tucker in his 1967 article were:

- Microprogramming provides an economical means of providing large instruction sets in small machines.
- Maintenance and diagnostic aids can be incorporated which provide excellent diagnostic information to service engineers.
- Emulation of different machines is possible.
- Microprogramming provides a flexible design to which new features can be added in the future.

An excellent example of point 4 is provided by Rosin.[0]

> "It is also the case that field modification and upgrading will be less expensive, since only the microprogram need by changed in some cases. Consider as a case in point the redefinition of floating-point arithmetic across the entire System/360 line of computers which took place in 1968. Preparation of this change for most of the models involved required only rewriting and debugging the appropriate microprograms and then installing these programs in the vast number of hardware systems in the field. The corresponding change, if made at the hardware level, could have been an economic catastrophe of major impact in IBM. Indeed, in the latter case the change might never have been attempted let alone completed in spite of its generally recognized value."

The application of microprogramming techniques to central processors has been frequently reported in the literature. These techniques, however, have often been used in the design of I/O controllers for the same reasons as those listed above. Furthermore, more and more logical networks are being designed using microprogramming techniques. Some prominent experts in the field are forecasting that most complex logical systems of the future will be microprogrammed. Indeed, the move toward functional packaging techniques using a higher proportion of logic interconnections on the circuit cards will accelerate this trend because logic changes by rewiring the back plane can no longer be made. However, ROS can be altered and replace those devices already on circuit cards. In this fashion, logic changes can be made to the machine's structure.

FUNDAMENTALS OF MICROPROGRAMMING

The basic ideas advanced by Wilkes were that one could envision the control portion of a computer as effecting a

number of transfers between registers. Some of these transfers might be effected in serial and others in parallel. Also, transfers might be made through logic networks such as adders which generated functions of the input data. The individual steps were generally referred to as microinstructions. A combination of these steps which executed a machine instruction was called a microprogram. Indeed in almost all sophisticated logical networks transfers of this type do take place. Therefore, these networks are adaptable to microprogramming techniques.

Figure 5 shows a simplified computing element. In reality, it could be a word organized single address stored program computer. In this simplified version assume the control portion of the machine generates the following signals shown in Table 1. These signals are called microinstructions. By combining these, computer instructions can be realized. Assume further that the control portion of the machine contains an ROS (Read Only Store) and that words are read from that ROS under the control of an address register. Words are read from the ROS in sequence unless one of the Jump instructions, JMP, JIFO or JOPC is executed.

SIMPLE MICRO PROGRAMMED MACHINE

CODE	MEANING
MARM	Gate MAR onto M bus
MBRM	Gate MBR onto M bus
PCD	Gate PC onto D bus
IAD	Gate IA (instruction address) onto D bus
ACD	Gate AC onto D bus
R	Read memory into MBR
W	Write MBR into memory
PLUS	Add M bus to D bus in address and place on S bus
DTS	Gate D bus through adder to S bus
MTS	Gate M bus through adder to S bus
ONE	Gate D bus through adder to S bus and add one
SMAR	Gate S bus into MAR
SMBR	Gate S bus into MBR
SPC	Gate S bus into PC
SIR	Gate S bus into IR
SAC	Gate S bus into AC
JMP	Jump to address in address field of microinstruction if AC = 0
JIFO	Jump to address in address field of microinstruction if AC = 0
JOPC	Jump to address of OP code field

TABLE 1

SIMPLE MICRO PROGRAMMED MACHINE

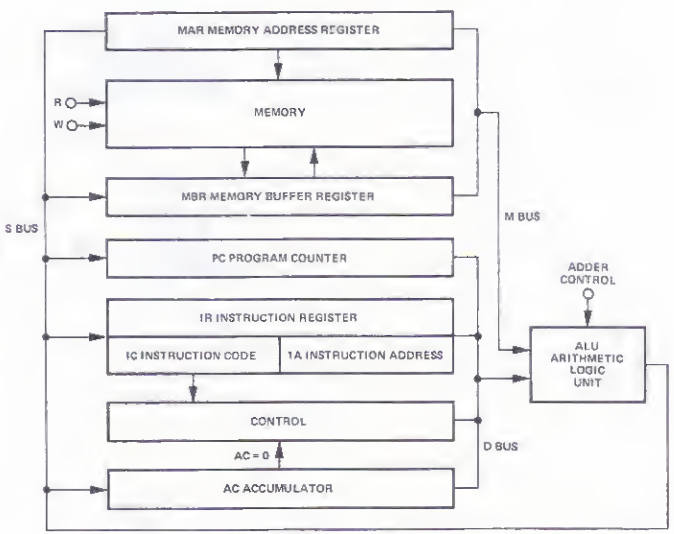


FIGURE 5

Figure 6 shows an ROS instruction word with the appropriate fields labeled. The instruction words are shown under the fields in which they appear in the microinstruction word. There are of course many different microinstruction formats. For example, the Interdata Mod IV or Micro 810 computers use compact 16 bit formats whereas systems such as the IBM 360/85 use 128 bit formats. The reason for these choices will be discussed later.

REPRESENTATION OF MICROINSTRUCTION WORD						
MEMORY CONTROL	JUMP INSTRUCTION	ADDER CONTROL	M BUS CONTROL	D BUS CONTROL	S BUS CONTROL	JUMP ADDRESS FIELD
R W	JMP JIFO JOPC	PLUS MTS ONE DTS	MARM MBRM	PCD IAD ACD	SMAR SMBR SPC SIR SAC	

FIGURE 6

MICROPROGRAM TO ADD CONTENTS OF MEMORY TO ACCUMULATOR							
		MEMORY CONTROL	JUMP INSTRUCTION	ADDER CONTROL	M BUS CONTROL	D BUS CONTROL	S BUS CONTROL	JUMP ADDRESS FIELD
INSTRUCTION FETCH	1	R		DTS		PCD	SMAR	
	2							
	3			MTS	MBRM		SIR	
INSTRUCTION DECODE	4		JOPC					
EXECUTE	5			DTS		IAD	SMAR	
	6	R						
	7			PLUS	MBRM	ACD	SAC	
RETURN	8			ONE		PCD	SPC	
	9		JMP					START

FIGURE 7

Figure 7 shows what kinds of simple operations can be accomplished by combining microinstructions. In the example, the contents of memory are added to the accumulator in the following manner:

Line 1 The contents of the program counter are transferred to the memory address register.

Line 2 The instruction is read from memory into the memory buffer register.

Line 3 The instruction is transferred from the memory buffer register to the instruction register.

Line 4 The control of the microprocessor is determined by the operation code of the instruction.

Line 5 The contents of the address portion of the instruction register are transferred to the memory address register.

Line 6 The desired data is read into the memory buffer register.

Line 7 The memory buffer register is added to the accumulator and the result stored in the accumulator.

Line 8 One is added to the program counter so it is ready to fetch the next instruction and the result is stored in the program counter.

Line 9 Control of the microprocessor is transferred to start the next instruction sequence.

It is fairly straightforward to envision more powerful devices than the one given in the example that perform many of the operations determined by separate lines in parallel and which have many more instruction codes.

MICROPROCESSOR INSTRUCTION WORDS

Microprogrammable controllers have word sizes generally no smaller than 16 bits and in large high speed systems such as the Iliac IV computer, as large as 280 bits. Generally, machines using short word lengths are slower because they perform fewer operations in parallel.

In short word length microprogrammable machines there are too few bits to control all of the required gates. Therefore, some of the bit codes in a word are used to specify how the instruction format should be decoded. A good example of this technique is the Interdata Mod IV.

In the Interdata Mod IV, four word formats shown in Figure 8 are used (the test and command formats are considered to be the same). Based on the code appearing in bits 0 to 3, the microprocessor control decodes the remainder of the instruction according to the specified

format. Because the microinstruction words work directly with the internal registers and control functions, the company claims a 10 to 1 speed improvement can be made over coding certain programs in machine language.

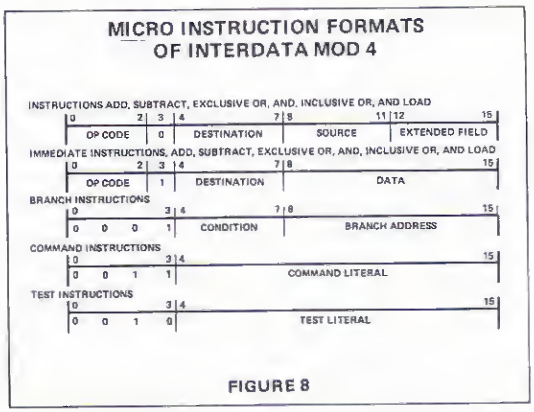


FIGURE 8

The five classes in instructions shown in Figure 8 perform the following functions:

- Instructions add, subtract, exclusive-or, and, inclusive-or, and load combine the contents of the source register with the A-register and store the result in the destination register. The extended field is used to control actions of carry flip flops, word shifts, etc.
- Immediate instructions add, subtract, exclusive-or, and, inclusive-or, and load combine the contents of the A-register with the data field of the instruction (bits 8 to 15) and store the result in the destination register.
- Branch instructions are used to test processor conditions and branch to the proper microinstruction depending on the processor status.
- Command instructions are used to initiate certain actions in the system. For example, they initiate a memory read or memory write cycle.
- Test instructions are used to test for certain machine conditions and will set internal flags depending on whether they are true or false.

The format of the Interdata Mod IV closely resembles that of conventional machine code and this makes microprogramming the device considerably easier. The disadvantage of this type of format is that only one major operation can be specified at one point in time. In machines with longer microinstruction words such as the IBM 360/50 which uses a 90 bit word, many micro-operations can be specified simultaneously and overlapped. Figure 9 shows the 360/50 instruction word.

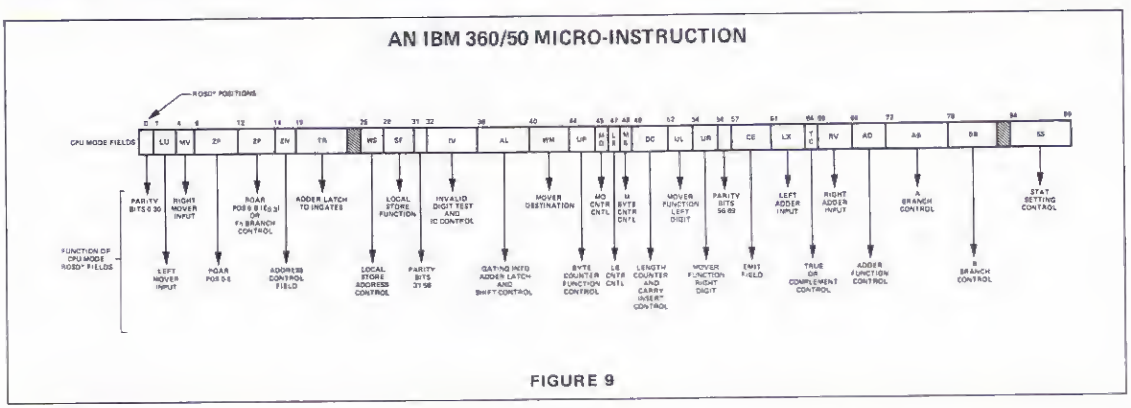


FIGURE 9

In the 360/50, the Read Only Memory consists of 2815 words of 500 ns cycle time. The 90 bit word is divided into a number of fields each by which determines a specific machine function. The address of the next microinstruction is determined partly by the current microinstruction and partly by the result of the current microinstruction operations.

ADVANTAGES OF MICROPROGRAMMING

Having reviewed some techniques used in microprogrammable devices, it is worthwhile to investigate in greater depth the advantage claimed by various manufacturers and authors for microprogrammable devices. Frequently both ROS and RAS (Random Access Store) have been used in the control store for microprogrammable devices. When the latter is used it is called WCS (Writable Control Store). Writeable Control Store is used in machines such as the IBM 360/85 and IBM 360/25. In general, WCS is used to store microprograms which are used infrequently such as emulators and diagnostics. The writeable store can be loaded via an ROS control program. Only as much control store need be provided to run the longest microprogram segment which must be in memory at any one time. This tecnhique can then be used to reduce the size of the control memory.

One of the first major commitments of large scale commercial computer architecture to a microprogrammable implementation was the IBM 360 system.

The various systems used the following speed ROS in their control memory.

Model	ROM Cycle Time μs
30	1.0
40	0.625
50	0.5
60	0.25
62	0.25

The most frequently claimed advantages for microprogrammable implementations of devices are:

- More structured organization. Usually the control portion of a system is made up of a great deal of random logic. Microprogrammed structures require a certain amount of random logic in their implementation but this does not increase as new control routines, instructions and features are added. These features can be implemented purely by adding more control memory.
- Emulation. One of the most frequent applications of microprogrammable devices is in emulation modes. Emulation is a process whereby one computer has its control programmed so that it can perform the operations of another. For example, the IBM 360/85 can emulate the operation of the IBM 7090 and thus programs which run in the 7090 will run in the 360/85.
- Diagnostics. Several computers put portions of their diagnostic routines into control memory. Examples of this are the Micro 810 and some of the larger models of the IBM 360. The advantage of putting diagnostics in the control memory is that individual portions of the system can be exercised and checked. Therefore, faults can be pinpointed precisely. Also, the starting diagnostics can be run with a smaller portion of the machine operating. In some systems parity bits are added to the control memory. This simplifies the location of faults in the control logic.
- General Purpose Nature of Microprogrammable Devices. One of the basic reasons for designing microprogrammable devices is their inherent general purpose nature. For example, many peripheral controllers used on large computer systems are microprogrammed. Because of this one basic controller can be used to control discs, magnetic tapes, etc. While there may be less expensive special purpose implementations from a component point of view, the microprogrammable implementation offers savings in design time, maintenance training and documentation.
- Field changes. One of the most frequent arguments against microprogrammable devices is the fact that a service technician can no longer change the device in the field. The concept has always been that if updates had to be made, an individual could always change the wiring. However, because electronic systems are being functionally packaged – i.e., the IC's are being interconnected on the card – there is an increasing probability that these changes can no longer be made simply by altering the wiring. Consequently, changing read only stores is becoming a more and more attractive alternative. To any individual who has ever spent 8 hours installing and checking out a 100 wire field change order, it represents a technological breakthrough.
- Macro and special instructions. Read only storage programs in microprogrammable devices are frequently used to tailor a processor to an application. For example, the Micro 800 is offered with special instruction options to handle a communications environment.
- Economy of expanding performance. Since new instructions and new options can be added by increasing the size of the read only store, it is relatively simple to add new features to the system.
- Late definition of final system configuration. In a system organization one of the most frequent complaints of logic designers is that someone changed the specifications. By using microprogramming techniques it is easier to make last minute changes.
- Lower documentation and service engineering training costs. Since one only changes the microprogram in order to change the device characteristics in a microprogrammable system, both documentation and maintenance training costs can be reduced. For example, in a conventional computer organization, the addition of floating point instructions will require the insertion of a great deal of random logic. Special documentation and field training is required to support the option. In the case of a microprogrammed device only the new microprogram need be documented.

CACHE TYPE SCRATCHPAD APPROACH IMPROVES CPU THROUGHPUT

Recent developemnts in bipolar semiconductors permit innovation in several areas of CPU design. Figure 1 shows a block diagram of a portion of CPU hardware and firmware, which utilizes new MS1 functions to improve throughput rate. The block diagram represents a 4K X 32 main memory, ALU with 32 X 2 scratchpad, 32 X 12 CAM, and microprogrammed control. The CAM allows the scratchpad to increase instruction rate when operating on recently addressed data. This approach may result in effective speedup on the CPU by a factor of 3 or more depending on the nature of the programs being run, the relative speeds of main memory and scratchpad, and the type of "overwrite" algorithm used.

FLOWCHART OF CACHE TYPE SCRATCHPAD

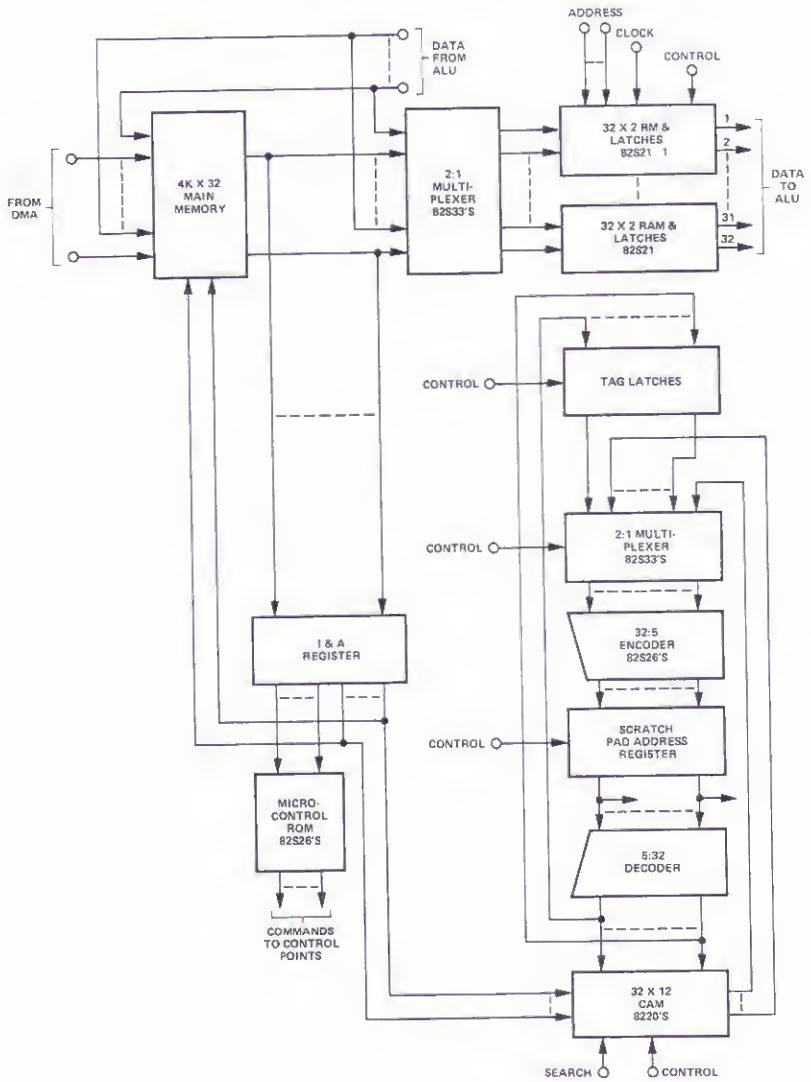


FIGURE 1

The flowchart of figure 2 clarifies operation of the block diagram. Initially, the next instruction word to be performed is loaded into the I and A register. Programmable read-only memories decode the commands that control the CPU and cause the following sequence of events. The address portion of the instruction is compared to CAM contents to determined whether the data to be manipulated has been stored in the scratchpad at a prior program step. If "yes", the CAM indicates the scratchpad location containing the data, and the instruction is performed without having to wait for a main memory read cycle to occur. If data has not been previously stored in the scratchpad, main memory is accessed. Data is then moved to an empty scratchpad location, the main memory address of that data is stored in the CAM, the corresponding tag latch is set and operation proceeds. If the scratchpad is full, overwriting is performed and the program then operates on the scratchpad data. The "overwrite" or "forgetting" algorithm must be tailored to the needs of the particular machine being developed.

Implementation of the cache-type scratchpad of Figure 1 may be accomplished using the following device types:

FUNCTION	DEVICE TYPE
Scratchpad and Output Latches	82S21 (32 X 2 RAM with latches).
Content Addressable Memory	8220 (4 X 2 CAM)
Decoder	82S50 (8:3 Decoder), 8XXX/74XX SSI Gates
Encoder	82S26 (256 X 4 FROM), 8808/7430 Gates
Micro-control	82S26 (256 X 4 FROM), 8XXX/74XX Gates and FF
Scratchpad Address Register (SPAR)	82S70 (Shift Register) or 82S91 (Counter)*
Tag Latches	8275 (Quad Latch)
Multiplexers	82S33 (Quad 2:1 Multiplexer)

*Device type dependent on choice of "overwrite" algorithm.

FLOWCHART OF CACHE TYPE SCRATCHPAD

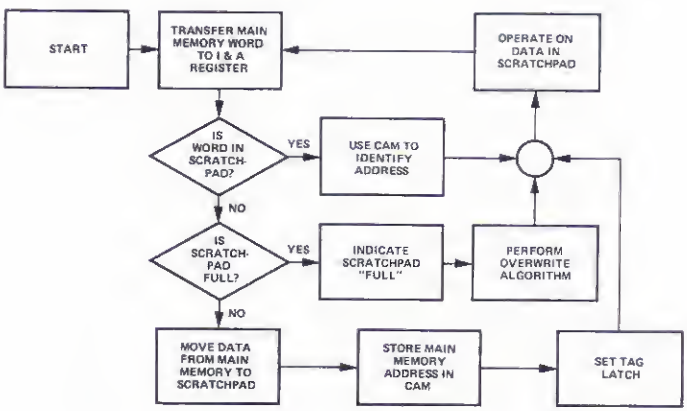


FIGURE 2

1 Wilkes, M. V., "The Best Way to Design an Automatic Calculating Machine," report of the Manchester University Computer Inaugural Conference, July 1951, pg. 16.

2 "Design of Microprogrammable Systems," Signetics Memory Systems Application Note SMS0052AN.

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4 Rosin, R. F., "Contemporary Concepts of Microprogramming and Emulation," Computing Surveys, Vol. 1, No. 4, Dec. 1969, Pg. 197.

5 Bartow, Neil and McGuire, Robert, "System/360 Model 85 Microdiagnostics," AFIPS, Vol. 36, 1970, Pg. 191.

6 Wilkes, M. V., "The Growth of Interest in Microprogramming," Computing Surveys, Vol. 1, No. 3, Sept. 1969, Pg. 139.

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8 Gerace, G. B., "Microprogramming Control for Computing Systems," IRE Transactions, EC-12, 1963, Pg. 733.

9 "Model 4 Microinstruction Reference Manual," Interdata Pub. No., 29-023.

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11 C. V. Ramamorthy and M. Tsuchiva. "A Study of User Microprogrammable Computers," AFIPS, Vol. 36, Pg. 165.

12 G. M. Amdahl, G. A. Bloauw, F. P. Brooks, Jr., "Architecture of the IBM System/360," IBM Journal of Research and Development, Vo. 8, No. 2, April 1964, Pg. 87.

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signetics

LINEAR
APPLICATIONS

6

Linear Functional Index

LINEAR

INTRODUCTION

Phase Locked Loops (PLLs) are a new class of monolithic circuits developed by Signetics, but they are based on frequency feedback technology which dates back 40 years.

A phase locked loop is basically an electronic servo loop consisting of a phase detector, a low pass filter and a voltage controlled oscillator. Its controlled oscillator phase makes it capable of locking or synchronizing with an incoming signal. If the phase changes, indicating the incoming frequency is changing, the phase detector output voltage increases or decreases just enough to keep the oscillator frequency the same as the incoming frequency, preserving the locked condition. Thus, the average voltage applied to the controlled oscillator is a function of the frequency of the incoming signal. In fact, the low pass filter voltage *is* the demodulated output when the incoming signal is frequency modulated (provided the controlled oscillator has a linear voltage-to-frequency transfer characteristic). The synchronous reception of radio signals using PLL techniques was described (Ref. 1) in the early thirties. You may have heard of the "homodyne" receiver.

The first widespread use of phase lock, however, was in TV receivers to synchronize the horizontal and vertical sweep oscillators to the transmitted sync pulses. Lately, narrow-band phase locked receivers have proved to be of considerable benefit in tracking weak satellite signals because of their superior noise immunity. Applications such as these were implemented primarily in discrete component form and involved considerable complexity even after the advent of transistors. This complexity made PLL techniques impractical or uneconomical in the majority of systems.

The development of complete, single-chip phase locked loops has changed this situation considerably. Now, a single packaged device with a few external components will offer the user all the benefits of phase locked loop operation, including independent center frequency and bandwidth adjustment, high noise immunity, high selectivity, high frequency operation and center frequency tuning by means of a single external component.

Signetics makes three basic classes of single-chip PLL circuits: the general purpose PLL, the PLL with an added multiplier and the PLL tone decoder.

The 560B, 562B and 565 are general purpose phase locked loops containing an oscillator, phase detector and amplifier. When locked to an incoming signal, they provide two outputs: a voltage proportional to the frequency of the incoming signal (FM output) and the square wave oscillator output which, during lock, is equal to the incoming frequency. All general purpose devices are optimized to provide a linear frequency-to-voltage transfer characteristic.

The 561B contains a complete PLL as those above, plus the additional multiplier or quadrature phase detector required for AM demodulation. In addition to the standard FM and oscillator outputs, it also provides an output voltage which is proportional to the amplitude of the incoming signal (AM output). The 561B is optimized for highly linear FM and AM demodulation.

The 567 is a special purpose phase locked loop intended solely for use as a tone decoder. It contains a complete PLL including oscillator, phase detector and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the locked frequency is above a minimal value, the driver amplifier turns on, driving a load as much as 200mA. It, thus, gives an output whenever an in-band tone is present. The 567 is optimized for both center frequency and bandwidth stability.

The 566 is not a phase locked loop, but a precision voltage-controllable waveform generator derived from the oscillator of the 565 general purpose loop. Because of its similarity to the 565 and because it lends itself well to use in, and in conjunction with, phase locked loops, it has been included in this section.

Table 8–1 summarizes the characteristics of Signetics phase locked loop products.

USER'S QUICK-LOOK GUIDE TO SIGNETICS PLLs

	Upper Frequency (MHz)	Maximum Lock Range (% f_o)	FM Distortion	Output Swing ±5% Deviation (volts p.p.)	Center Frequency Stability (ppm/°C)	Frequency Drift with Supply Voltage (%/volt)	Input Resistance	AM Output Available	Typical Supply Current (mA)	Supply Voltage Range (volts)
NE560	30	40%	.3%	1	±600	.3	2K**	No	9	+16 to +26
NE561	30	40%	.3%	1	±600	.3	2K**	Yes	10	+16 to +26
NE562	30	40%	.5%	1	±600	.3	2K**	No	12	+16 to +30
NE565	.5	120%	.2%	.15	±200	.16	5K	No	8	±6 to ±12
SE565	.5	120%	.2%	.15	±100	.08	5K	No	8	±6 to ±12
NE567	.5	14%	5%*	.20	35±60	.7	20K**	Yes*	7	+ 4.5 to +9
SE567	.5	14%	5%*	.20	35±60	.5	20K**	Yes*	6	+ 4.5 to +9
NE566	.5		.2%	30%/V***	±200	.16			7	+10 to +26
SE566	.5		.2%	30%/V***	±100	.08			7	+10 to +26

* The 567 AM and FM outputs are available, but are not optimized for linear demodulation.

** Input biased internally.

*** Figure shown is VCO gain in percent deviation per volt.

A considerable quantity of detailed specifications and publications information for these products is included in the Linear Spec. Handbook. Because many readers are likely to be unfamiliar with the terminology and operating characteristics of phase locked loops, a glossary of terms and a general explanation of PLL principles are included here with a detailed discussion of the action of the individual loop elements.

The tradeoff and setup section will assist the read in some of the considerations involved in selecting and applying these products to meet system requirements. A brief summary of measurement techniques has been presented to aid the user in achieving his performance goals.

Detailed descriptions have been provided for each of the products. The user can supplement the suggested connection diagrams with his own schemes.

Perhaps the best way to become familiar with the many uses of phase locked loops is to actually study the various application circuits provided. These circuits have been drawn from many sources – textbooks, users, Signetics' applications engineers and the 1970 Signetics–EDN Phase Locked Loop contest. Every effort has been made to provide usable, workable circuits which may be copied directly or used as jumping-off points for other imaginative applications.

The section on interfacing will aid the user in driving different forms of logic from PLL outputs and the section on expanding loop capabilities will show how to achieve improved performance in certain difficult applications.

PHASE LOCKED LOOP TERMINOLOGY

The following is a brief glossary of terms encountered in PLL literature.

CAPTURE RANGE ($2 \cdot \omega_C$) – Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes. The range over which the loop *can* acquire lock is termed capture range. The capture range is sometimes called the LOCK-IN RANGE. (The latter refers to how close a signal must be to the center frequency before acquisition can occur. It is thus one-half the capture range or ω_C.)

CURRENT CONTROLLED OSCILLATOR (CCO) – An oscillator similar to a VCO in which the frequency is determined by an applied current.

DAMPING FACTOR (ζ) – The standard damping constant of a second order feedback system. In the case of the PLL, it refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

FREE-RUNNING FREQUENCY (f_o, ω_o) – Also called the CENTER FREQUENCY, this is the frequency at which the loop VCO operates when not locked to an input signal. The same symbols (f_o, ω_o) used for the free-running frequency are commonly used for the general oscillator frequency. It is usually clear which is meant from the context.

LOCK RANGE ($2 \cdot \omega_L$) – The range of input frequencies over which the loop will remain in lock. It is also called the TRACKING RANGE or HOLD-IN RANGE. (The latter refers to how far the loop frequency can be deviated from the center frequency and is one-half the lock range or ω_L.)

LOOP GAIN (K_v) – The product of the dc gains of all the loop elements, in units of $(sec)^{-1}$.

LOOP NOISE BANDWIDTH (B_L) – A loop property related to damping and natural frequency which describes the effective bandwidth of the received signal. Noise and signal components outside this band are greatly attenuated.

LOW PASS FILTER (LPF) – A low pass filter in the loop which permits only dc and low frequency voltages to travel around the loop. It controls the capture range and the noise and out-band signal rejection characteristics.

NATURAL FREQUENCY (ω_n) – The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane. May be determined experimentally as the modulation frequency for which an underdamped loop gives the maximum output and at which phase error swing is the greatest.

PHASE DETECTOR GAIN FACTOR (K_d) – The conversion factor between the phase detector output voltage and the phase difference between input and VCO signals in volts/radian. At low input signal amplitudes, the gain is also a function of input level.

PHASE DETECTOR (PD) – A circuit which compares the input and VCO signals and produces an error voltage which is dependent upon their relative phase difference. This error signal corrects the VCO frequency during tracking. Also called PHASE COMPARATOR. A MULTIPLIER or MIXER is often used as a phase detector.

QUADRATURE PHASE DETECTOR (QPD) – A phase detector operated in quadrature (90^o out of phase) with the loop phase detector. It is used primarily for AM demodulation and lock detection.

VCO CONVERSION GAIN (K_o) – The conversion factor between VCO frequency and control voltage in radians/second/volt.

VOLTAGE CONTROLLED OSCILLATOR (VCO) – An oscillator whose frequency is determined by an applied control voltage.

THE PHASE LOCKED LOOP PRINCIPLE

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 8–1. Detailed analysis of the PLL as a feedback control system has been discussed in the literature (Ref. 2). Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. The parameters in the equations are somewhat different, however, since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

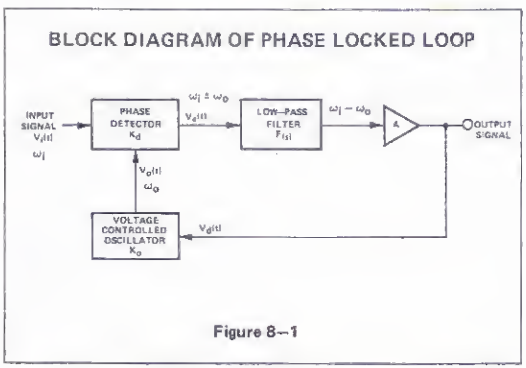


Figure 8–1

LOOP OPERATION

A rigorous mathematical analysis of the system is quite cumbersome and will not be repeated here. However, from a qualitative point of view, the basic principle of PLL operation can be briefly explained as follows: With no signal input applied to the system, the error voltage V_d is equal to zero. The VCO operates at a set frequency ω_o, which is known as the free-running frequency. If an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between f_o and the input signal. If the input frequency ω_i is sufficiently close to ω_o, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference. This net phase difference θ_o is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_i and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the "lock range."

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_o$ shown in Figure 8–1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component $(\omega_i - \omega_o)$ is zero; hence, the output of the phase comparator contains a dc component. The low pass filter removes the sum frequency component $(\omega_i + \omega_o)$ but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. Now, however, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as *the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal.* The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as *the frequency range usually centered about the VCO initial free-running frequency over which the loop can track the input signal once lock has been achieved.*

When the loop is in lock, the difference frequency component on the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

THE CAPTURE TRANSIENT

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows: Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\theta_o}{d_t}$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_o is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL was opened, say between the low pass filter and the VCO control input, then for a given condition of ω_o and ω_i the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_i and ω_o were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation. Now suppose that the feedback loop is closed by connecting the low pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to ω_i (i.e., decreasing $\Delta\omega$), then $\frac{d\theta_o}{d_t}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_i, $\frac{d\theta_o}{d_t}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 8–2a. Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward ω_i, thus decreasing $\Delta\omega$. In this manner, the beat note frequency rapidly decreases toward zero, the VCO frequency drifts toward ω_i and the lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state dc error voltage remains.

ASYNCHRONOUS ERROR BEAT FREQUENCY DURING THE CAPTURE PROCESS

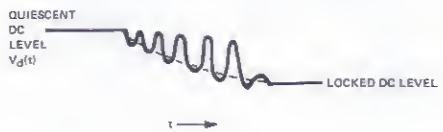


Figure 8–2a

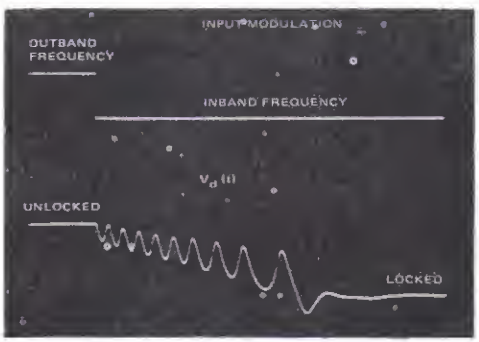


Figure 8–2b

Figure 8–2b displays an oscillogram of the loop error voltage V_d in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low pass filter attenuation becomes less and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the pull-in time. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 8–3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input tone-burst frequency was within its lock and capture range.

FAST CAPTURE EXHIBITED BY FIRST ORDER LOOP

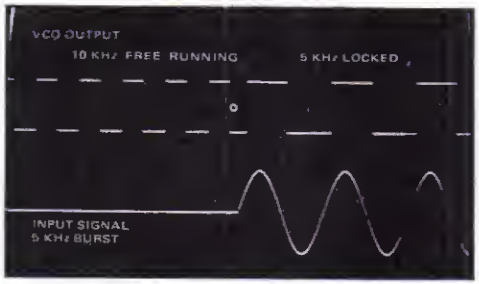


Figure 8–3

EFFECT OF THE LOW PASS FILTER

In the operation of the loop, the low pass filter serves a dual function: First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. The low pass filter bandwidth has the following effects on system performance:

a.) The capture process becomes slower, and the pull-in time increases.
b.) The capture range decreases.
c.) Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.
d.) The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

LINEARIZED MODEL OF THE PLL AS A NEGATIVE FEEDBACK SYSTEM

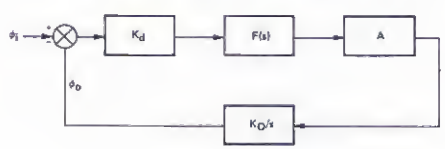


Figure 8–4

LINEAR ANALYSIS FOR LOCK CONDITION – FREQUENCY TRACKING

When the PLL is in lock, the non-linear capture transients are no longer present. Therefore, under lock condition, the PLL can often be approximated as a linear control system (see Figure 8–4) and can be analyzed using Laplace transform techniques. In this case, it is convenient to use the net phase error in the loop ($\theta_s - \theta_o$) as the system variable. Each of the gain terms associated with the blocks can be defined as follows:

K_d = conversion gain of phase detector (volt/rad)
F(s) = transfer characteristic of low pass filter
A = amplifier voltage gain
K_θ = VCO conversion gain (rad/sec/volt)

Note that, since the VCO converts a voltage to a frequency and since phase is the integral of frequency, the VCO functions as an integrator in the feedback loop.

The open loop transfer function for the PLL can be written as

$$T(s) = \frac{K_v F(s)}{s}$$

where K_v is the total loop gain, i.e., $K_v = K_o K_d A$. Using linear feedback analysis techniques, the closed loop transfer characteristics H(s) can be related to the open loop performance as

$$H(s) = \frac{T(s)}{1 + T(s)}$$

and the roots of the characteristic system polynominal can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

The simplest case is that of the first order loop where F(s) = 1 (no filter). The closed loop transfer function then becomes

$$T(s) = \frac{K_v}{s + K_v}$$

This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 8–5a. The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present on the phase detector output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

ROOT LOCUS AND FREQUENCY RESPONSE PLOTS OF FIRST AND SECOND ORDER LOOPS

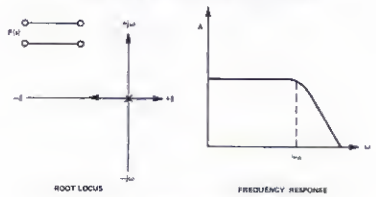


Figure 8–5a

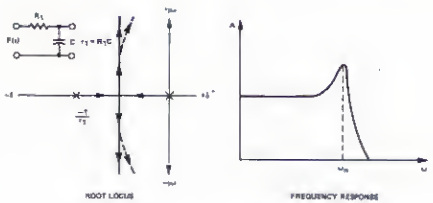


Figure 8–5b

With the addition of a single pole low pass filter F(s) of the form

$$F(s) = \frac{1}{1+\tau_1 s}$$

where $\tau_1 = R_1C$, the PLL becomes a second order system with the root locus shown in Figure 8–5b. Here, we again have an open loop pole at the origin because of the integrating action of the VCO and another open loop pole at a position equal to $\frac{-1}{\tau_1}$ where τ_1 is the time constant of the low pass filter.

One can make the following observations from the root locus characteristics of Figure 8–5b.

a.) As the loop gain K_v increases for a given choice of τ_1, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more underdamped.

b.) If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 8–5b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 8–5c. This type of a filter has the transfer function

$$F(s) = \frac{1+\tau_2 s}{1+(\tau_1+\tau_2)s}$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. By proper choice of R_2, this type of filter confines the root locus to the left half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second order loop and if $R_2 = \infty$, the loop behaves as a first order loop due to a pole-zero cancellation. Note, however, that as first order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

SECOND ORDER PLL RESPONSE WITH SIMPLE LAG FILTER

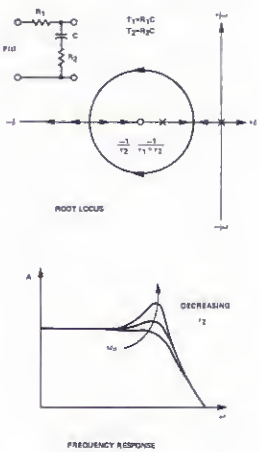


Figure 8–5c

In terms of the basic gain expressions in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the dc loop gain

$$2\omega_L = 4\pi f_L = 2K_v.$$

Since the capture range ω_L denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as:

$$2\omega_c = 4\pi f_c \simeq 2K_v \quad F(j\omega_c)$$

where $F(j\omega_c)$ is the low pass filter amplitude response at $\omega = \omega_L$. Note that at all times the capture range is smaller than the lock range. If the simple lag filter of Figure 8–5b is used, the capture range equation can be approximated as

$$2\omega_c \simeq 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_v}{\tau_1}}$$

Thus, the capture range decreases as the low pass filter time constant is increased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 8–6 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 8–6a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO gain ($1/K_o$) and goes through zero as $\omega_i = \omega_o$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back now, the cycle repeats itself, but it is inverted, as shown in Figure 8–6b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_c = \omega_3 - \omega_1 \text{ and } 2\omega_L = \omega_2 - \omega_4$$

TYPICAL PLL FREQUENCY-TO-VOLTAGE TRANSFER CHARACTERISTICS FOR INPUT FREQUENCY INCREASING AND DECREASING

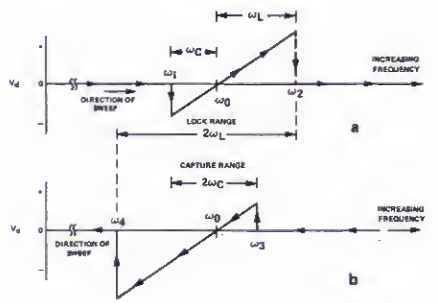


Figure 8–6

Note that, as indicated by the transfer characteristics of Figure 8–6, the PLL system has an inherent selectivity about the center frequency set by the VCO free-running frequency ω_o; it will respond only to the input signal frequencies that are separated from ω_o by less than ω_c or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

PHASE LOCKED LOOP BUILDING BLOCKS

VOLTAGE CONTROLLED OSCILLATOR

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_o (in radian/sec/volt).

$$K_o = \frac{\Delta\omega_o}{\Delta V_o}$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_o = \frac{\Delta\omega_o}{K_o}$$

The gain K_o can be found from the data sheet by taking the change in VCO control voltage for a given percentage frequency deviation and multiplying by the center frequency. When the VCO voltage is changed, the frequency change is virtually instantaneous.

All Signetics phase locked loops use the same form of phase detector—often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 8–7.

INTEGRATED PHASE DETECTOR

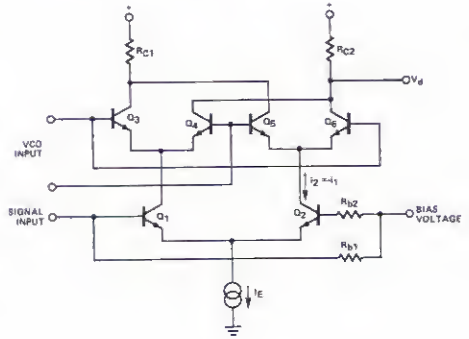


Figure 8–7

The input stage formed by transistors Q_1 and Q_2 may be viewed as a differential amplifier which has a collector resistance R_C and whose differential gain at balance is the ratio of R_C to the emitter resistance r_e of Q_1 and Q_2.

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_e/2}} = \frac{R_C}{0.013\, I_e}$$

The switching stage formed by $Q_3 - Q_6$ is switched on and off by the VCO square wave. Since the collector current swing of Q_2 is the negative of the collector current swing of Q_1, the switching action has the effect of multiplying the differential stage output first by +1 and then by −1. That is, when the base of Q_4 is positive, R_{C2} receives I_1 and when the base of Q_6 is positive, R_{C2} receives $I_2 = -I_1$. Since we have called this a multiplier, let us perform the multiplication to gain further insight into the action of the phase detector.

Suppose we have an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

$$V_i + V_k = V_i \sin(\omega_i t + \theta_i) + V_k \sin(\omega_k t + \theta_k)$$

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$\frac{4}{\pi(2n+1)} \sin[(2n+1)\,\omega_o t]$$

where ω_o is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationship and inserting the differential stage gain A_d, we get

$$V_d = \frac{2A_d}{\pi}\left[\sum_{n=0}^{\infty}\frac{V_i}{(2n+1)}\cos\left[(2n+1)\,\omega_o t - \omega_i t - \theta_i\right]\right.$$

$$-\sum_{n=0}^{\infty}\frac{V_i}{(2n+1)}\cos\left[(2n+1)\,\omega_o t + \omega_i t + \theta_i\right]$$

$$+\sum_{n=0}^{\infty}\frac{V_k}{(2n+1)}\cos\left[(2n+1)\omega_o t - \omega_k t - \theta_k\right]$$

$$\left.-\sum_{n=0}^{\infty}\frac{V_k}{(2n+1)}\cos\left[(2n+1)\omega_o t + \omega_k t + \theta_k\right]\right]$$

Assuming the V_k is zero, temporarily, if ω_i is close to ω_o, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As ω_o is driven closer to ω_i, this difference component becomes lower and lower in frequency until $\omega_o = \omega_i$ and lock is achieved. The first term then becomes

$$\frac{2A_d V_i}{\pi}\cos\theta_i$$

which is the usual phase detector formula showing the dc component of the phase detector during lock. This component must equal the voltage necessary to keep the VCO at ω_o. It is possible for ω_o to equal ω_i momentarily during the lock up process and, yet, for the phase to be incorrect so that ω_o passes through ω_i without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_i = \omega_o$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_i = (2n + 1)\ \omega_o$, giving the dc phase detector component

$$\frac{2A_dV_i}{\pi(2n+1)} \quad \cos\ \theta_i$$

showing that the loop can lock to odd harmonics of the center frequency. The (2n + 1) term in the denominator shows that the phase detector output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase detector output during lock is (assuming A_d is constant) also a function of the input amplitude V_i. Thus, for a given dc phase detector output V_d, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_i becomes, the more reduced is the lock range.

Going to the second term, we note that during lock the lowest possible frequency is $\omega_o + \omega_i = 2\omega_i$. A sum frequency component is always present at the phase detector output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase detector output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that we have other frequencies represented by V_k present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_i, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. Suppose lock has been achieved, however, so that $\omega_o = \omega_i$. In order for lock to be maintained, the average phase detector output must be constant. If $\omega_o = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_i. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. We can reduce this effect by decreasing the cutoff frequency of the low pass filter so that the $\omega_o - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_o - \omega_i$ is likewise attenuated) when the low pass filter capacitor is large.

The third term can have a dc component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)$ $(\omega_o - \omega_i)$ is zero and θ_k makes its appearance. This will have an effect on θ_i which will change the θ_i versus frequency ω_i. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_i is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase detector output will have a component at the locked frequency ω_o at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental ω_o at the phase detector output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, we need only worry about those close to the locked frequency.

The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by:

$$V_q = \frac{2A_qV_i}{\pi} \quad \sin\ \theta_i$$

where V_i is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

$$V_q = \frac{2A_qV_i}{\pi}$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

FUNCTIONAL APPLICATIONS

LOW PASS FILTER

The simplest type of low pass filter for the second order loop is a single pole RC type shown in Figure 8–5b. In all Signetics' loops, the resistor is internal and the capacitor is external. The inside resistor greatly improves the center frequency stability of the loop with temperature variations. Fortunately, the capture range and loop damping are related to the square root of this internal resistor value, so variations in its absolute value have little effect on loop performance. The nominal value of the internal resistor for each loop is given in the circuit diagrams of the detailed circuit descriptions in this chapter. The typical tolerance on these integrated resistors is ±20%.

As a functional building block, the phase locked loop is suitable for a wide variety of frequency related applications. These applications generally fall into one or more of the following categories:

a.) FM Demodulation
b.) Frequency Synthesizing
c.) Frequency Synchronization
d.) Signal Conditioning
e.) AM Demodulation

FM DEMODULATION

If the PLL is locked to a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage, which forces the VCO to maintain lock with the input signal then becomes the demodulated FM output. The linearity of this demodulated signal depends solely on the linearity of the VCO control-voltage-to-frequency transfer characteristic.

It should be noted that since the PLL is in lock during the FM demodulation process, the response is linear and can be readily predicted from a root locus plot.

FM demodulation applications are numerous; however, some of the more popular are:

Broadcast FM Detection

Here, the PLL can be used as a complete IF strip, limiter and FM detector which may be used for detecting either wide or narrow band FM signals with greater linearity than can be obtained by other means. For frequencies within the range of the VCO, the PLL functions as a self contained receiver since it combines the functions of frequency selectivity and demodulation. One increasingly popular use of the PLL is in scanning-receivers where a number of broadcast channels may be sequentially monitored by simply varying the VCO free-running frequency.

FM Telemetry

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 8–8 to a point between the FM discrimator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

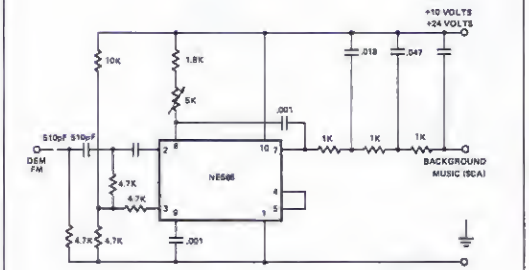


Figure 8–8

Frequency Shift Keying (FSK)

This refers to what is essentially digital frequency modulation. FSK is a means for transmitting digital information by a carrier which is shifted between two discrete frequencies. In this case, the two discrete frequencies correspond to a digital "1" and a digital "0," respectively. When the PLL is locked to a FSK signal, the demodulated output (error voltage) shifts between two discrete voltage levels, corresponding to the demodulated binary output. FSK techniques are often used in modems (modulator-demodulators), intended for transmitting data over telephone lines.

FREQUENCY SYNTHESIS

Frequency Multiplication can be achieved with the PLL in two ways:

a.) Locking to a harmonic of the input signal
b.) Insertion of a counter (digital frequency divider) in the loop

Harmonic locking is the simplest and can usually be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. A limitation on this scheme, however, is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 8–9. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the *divided* VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property, is the use of the PLL in wide range frequency synthesizers.

BLOCK DIAGRAM OF FREQUENCY SYNTHESIZER USING FREQUENCY DIVIDER

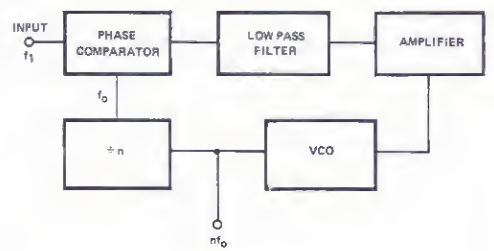


Figure 8–9

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.

For the case of frequency fractionalization, both harmonic locking and frequency countdown could be used to generate, for instance, a frequency exactly 16/3 the input. In this case, the circuit of Figure 8–10 could be used with the initial VCO frequency set to approximately 16/3 the expected input frequency. The counter then divides the VCO frequency by 16, and the input is locked to the 3rd harmonic of the counter output. Now the output can be taken as the VCO output and it will be exactly 16/3 of the input frequency as long as the loop is in lock.

IMPLEMENTATION OF FREQUENCY SYNTHESIZER (565)

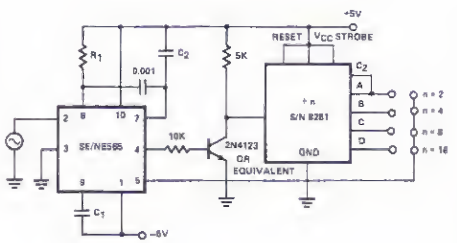


Figure 8–10

Frequency translation can be achieved by adding a mixer and a low pass filter stage to the basic PLL as shown in Figure 8–11. With this system the PLL can be used to translate the frequency of a highly stable but fixed-frequency reference oscillator by a small amount in frequency.

In this case, the reference input f_R and the VCO output f_o are applied to the inputs of the mixer stage. The mixer output is made up of the sum and the difference components of f_R and f_o. The sum component is filtered by the first low pass filter. The translation or offset frequency f_1 is applied to the phase comparator along with the $f_R - f_o$ component of the mixer output. When the system is in lock, the two inputs of the phase comparator are at identical frequency, that is,

$$f_o - f_R = f_1 \quad \text{or} \quad f_o = f_R + f_1$$

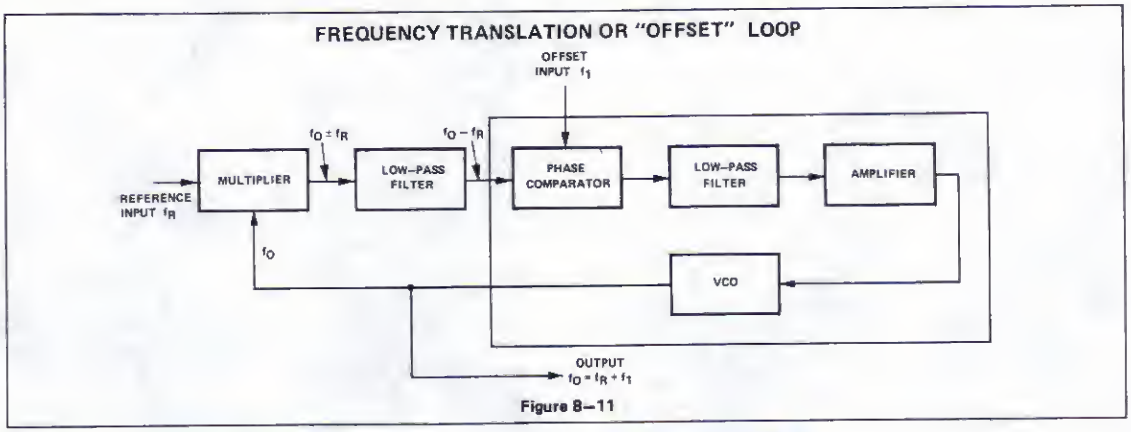


Figure 8–11

FREQUENCY SYNCHRONIZATION

Using the phase locked loop system, the frequency of the less precise VCO can be phase locked with a low level but highly stable reference signal. Thus, the VCO output reproduces the reference signal frequency at the same per-unit accuracy, but at a much higher power level. In some applications, the synchronizing signal can be in the form of a low duty cycle burst at a specific frequency. Then, the PLL can be used to regenerate a coherent CW reference frequency locking onto this short synchronizing pulse. A typical example of such an application is seen in the phase locked chroma-reference generators of color television receivers.

In digital systems, the PLL can be used for a variety of synchronization functions. For example, two system clocks can be phase locked to each other such that one can function as a back up for the other; or PLLs can be used in synchronizing disk or tape drive mechanisms in information storage and retrieval systems. In pulse-code modulation (PCM) telemetry receivers or in repeater systems, the PLL is used for bit synchronization.

Other popular applications include locking to WWVB to generate an inexpensive laboratory frequency standard and synchronizing tape speed for playback of a tape recorded at an irregular speed.

SIGNAL CONDITIONING

By proper choice of the VCO free-running frequency, the PLL can be made to lock to any one of a number of signals present at the input. Hence, the VCO output reproduces the frequency of the desired signal, while greatly attenuating the undesired frequencies of sidebands present at the input.

If the loop bandwidth is sufficiently narrow, the signal-to-noise ratio at the VCO output can be much better than that at the input. Thus, the PLL can be used as a noise filter for regenerating weak signals buried in noise.

AM DEMODULATION

AM demodulation may be achieved with PLL by the scheme shown in Figure 8–12. In this mode of operation, the PLL functions as a synchronous AM detector. The PLL locks on the carrier of the AM signal so that the VCO output has the same frequency as that of the carrier but no amplitude modulation. The demodulated AM is then obtained by multiplying the VCO signal with the modulated input signal and filtering the output to remove all but the difference frequency component. It may be recalled from the initial discussion that when the frequency of the input signal is identical to the free-running frequency of the VCO, the loop goes into lock with these signals 90^{o} out of phase. If the input is now shifted 90^{o} so that it is in phase with the VCO signal and the two signals are mixed in a second phase comparator, the average dc value (difference frequency component) of the phase comparator output will be directly proportional to the amplitude of the input signal.

The PLL still exhibits the same capture range phenomena discussed earlier so that the loop has an inherent high degree of selectivity centered about the free-running VCO frequency. Because this method is essentially a coherent detection technique which involves averaging of the two compared signals, it offers a higher degree of noise immunity than can be obtained with conventional peak-detector-type AM demodulators.

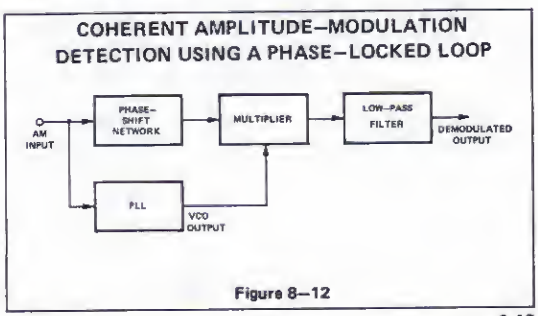


Figure 8–12

GENERAL LOOP SETUP AND TRADEOFFS

In a given application, maximum PLL effectiveness can be achieved if the user understands the tradeoffs which can be made. Generally speaking, the user is free to select the frequency, tracking or lock range, capture range and input amplitude.

CENTER FREQUENCY SELECTION

Setting the center frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming so that detection or tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow band operation (reduced tracking speed).

All of Signetics' loops use a multiplier in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase detector discussion would suggest that the PLL cannot lock to subharmonics because the phase detector cannot produce a dc component if ω_i is less than ω_o.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at f_o. For example, a square wave of fundamental $f_o/3$ will have a substantial component at f_o to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven (the resultant internal limiting generates harmonic frequencies). Locking to even harmonics or subharmonics is the least satisfactory since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial even harmonic content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest f_o. This magnitude can be used to estimate the capture and lock range.

All of Signetics' loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature compensated over the entire military temperature range (−55 to +125°C). To benefit from this inherent stability, however, the user must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the user may wish to trade some stability for lower cost external components.

TRACKING OR LOCK RANGE CONTROL

Two things limit the lock or tracking range. First, any VCO can only swing so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase detector is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. It often happens with low input amplitudes that even the full ±90° phase range of the phase detector cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. We must, therefore, give up some tracking capability and accept greater phase errors if the input signal is weak. Conversely, a strong input signal will allow us to use the entire VCO swing capability and keep the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that tracking range does not depend on the low pass filter. However, if a low pass filter *is* in the loop, it will have the effect of limiting the maximum *rate* at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0 or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that our output contains a significant and often bothersome signal

at twice the input frequency. (Remember that the multiplier forms both the sum and difference frequencies. During lock. the difference frequency is zero, but the sum frequency of twice the locked frequency is still present.) This sum frequency component can then be filtered out with an external low pass filter.

CAPTURE RANGE CONTROL

There are two main reasons for making the low pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase detector output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase detector to drive the VCO towards the input frequency. If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

CHOICE OF INPUT LEVEL

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the tracking (lock) and capture range becomes independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase detector gain and will result in a lock range which becomes constant with amplitude as the phase detector gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speed.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a.) Input phase
b.) Low pass filter characteristic
c.) Loop damping
d.) Deviation of input frequency from center frequency
e.) In-band input amplitude
f.) Out-band signals and noise
g.) Center frequency

Fortunately, it is usually sufficient to know how we can improve the lock-up time and what we must tradeoff to get faster lock-up. Suppose we have set up a loop or tone decoder and find that occasionally the lock-up transient is too long. What can be done to improve the situation—keeping in mind the factors that influence lock?

a.) Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 8—13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at $t = 0$. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of pulse train and the transmitted tone phase-related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b.) Low pass filter — The larger the low pass filter time constant, the longer will be the lock-up time. We can reduce lock-up time by decreasing the filter time constant, but in doing so, we sacrifice some of the noise immunity and out-band signal rejection which caused us to use a large filter in the first place. We must also accept a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low pass capacitor automatically increases the bandwidth. We gain speed only at the expense of added bandwidth.

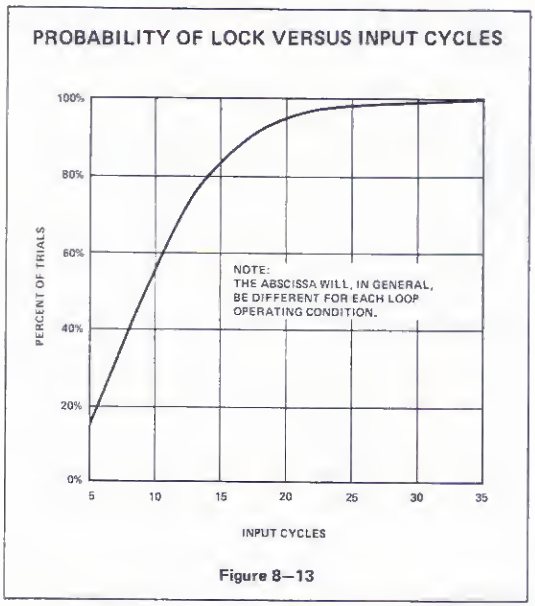


Figure 8–13

c.) Loop damping -- Loop damping for a simple time constant low pass filter is:

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{\tau K_v}}$$

Damping can be increased not only by reducing τ, as discussed above, but also by reducing the loop gain K_v. By using the loop gain reduction to control bandwidth or capture and lock range, we achieve better damping for narrow bandwidth operation. The penalty for this damping is that more phase detector output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d.) Input frequency deviation from free-running frequency — Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e.) In-band input amplitude — Since input amplitude is one factor in the phase detector gain K_d and since K_d is a factor in the loop gain K_v, damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low pass capacitor can charge with the reduced phase detector output (see d above).

f.) Out-band signals and noise — Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g.) Center frequency — Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies *on the average* will be detected before the lower frequencies. However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with user measurements of PLL operation. The techniques suggested are meant to help the user in evaluating the performance of his PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the user's test equipment may be limited, we have stressed the techniques which require a minimum of standard test items.

CENTER FREQUENCY

Center frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass and low pass filter capacitors. No input signal should be present. As the center frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor unless the capacity added by the measurement probe is much less than the timing capacitor value since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a dc voltage for production readout or automated testing, a calibrated phase locked loop can be used as a frequency meter (see Applications Section).

CAPTURE AND LOCK RANGE

Figure 8–14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X–Y recorder. The sweep voltage is applied to the X axis.

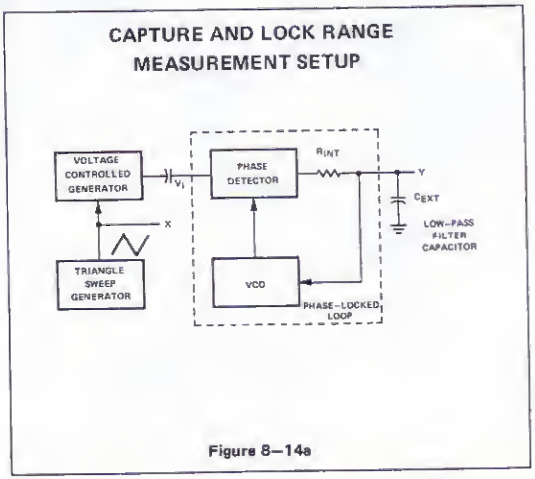


Figure 8–14a

Figure 8–14b shows the type of trace which results. The lock range (also called hold-in or tracking range) is given by the outer lines on the trace, which are formed as the incoming frequency sweeps *away* from the center frequency. The inner trace, formed as the frequency sweeps *toward* the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta t/\Delta V$) is the gain or conversion factor for the VCO.

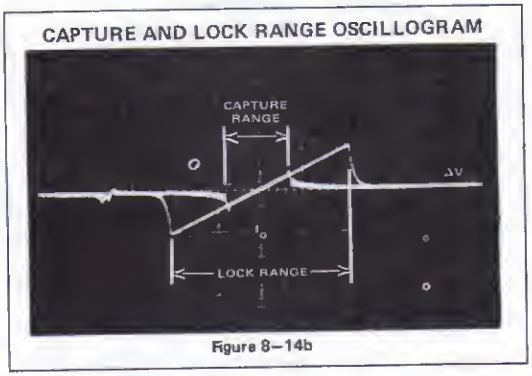


Figure 8–14b

By using the sweep technique, the effect on center frequency, capture range and lock range of the input amplitude, supply voltage, low pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be very much lower than the center frequency, especially when the capture range is below 10% of center frequency. Otherwise, the *apparent* capture and lock range will be a function of sweep frequency. It is best to start sweeping as slow as possible and, if desired, increase the rate until capture range begins to show an apparent reduction—indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the center frequency. In the case of the 561 and 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 8–15, showing the output level versus frequency for one value of input amplitude.

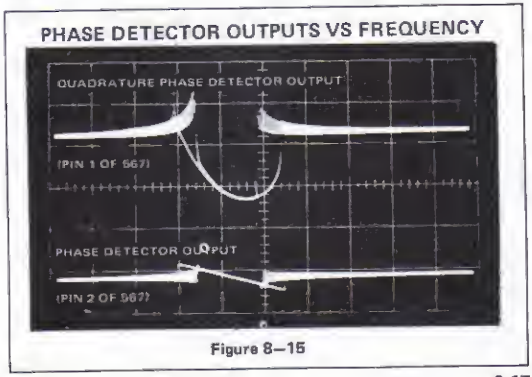


Figure 8–15

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the dc voltage at the low pass filter or the ac beat frequency components at the low pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straightforward. The loop is simply setup for FM or AM (561 or 567) detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP 333 A) can be used to measure distortion at the FM or AM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase detector output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured. The same comment applies to the measurement of AM distortion on the 561.

When AM distortion is being measured, the carrier frequency offset becomes more important. The lowest absolute value of carrier voltage at the modulation valleys must be high enough to maintain lock at the frequency deviation present. Otherwise, lock will periodically be lost and the distortion will be unreasonable. For example, the typical tracking range as a function of input signal graph in the 561 data sheet gives a total 3% tracking range at 0.3mV rms input. Thus, for a carrier deviation of 1.5%, the carrier must not drop below 0.3V rms in the modulation valleys. Naturally, the AM amplitude must not be too high or the AM information will be suppressed.

NATURAL FREQUENCY (ω_n)

Expressions for the natural frequency in terms of the loop gains and filter parameters are given in Table 8–2.

EXPRESSIONS FOR ω_n AND ζ IN SECOND ORDER LOOP

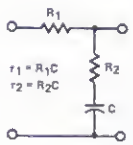
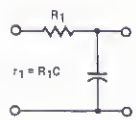
LOOP FILTER TYPE	NATURAL FREQUENCY ω_n	DAMPING ζ
	$\sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}}$	$1/2\ \omega_n\ (\tau_2 + \frac{1}{K_o K_d})$
	$\sqrt{\frac{K_o K_d}{\tau_1}}$	$\frac{\omega_n}{2 K_O K_D}$

Table 8–2

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency modulated signal of the desired amplitude to the loop (Table 8–2 shows that the natural frequency is a function of K_d, in turn a function of input amplitude). As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $S_m = \omega_n$ and the output amplitude will peak.

DAMPING (ζ)

As shown in Table 8–2 in the discussion on low pass filter, damping is a function of K_o, K_d and the low pass filter. Since K_o and K_d are functions of center frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency modulated within the lock range by a square wave. The low pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 8–16. Figure 8–17 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 8–18, which gives the transient phase error due to a step in input frequency.

MEASUREMENT SETUP FOR DISPLAY OF LOOP TRANSIENT RESPONSE

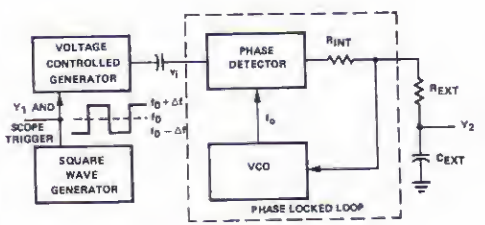


Figure 8–16

UNDERDAMPED $\zeta \approx 0.3$

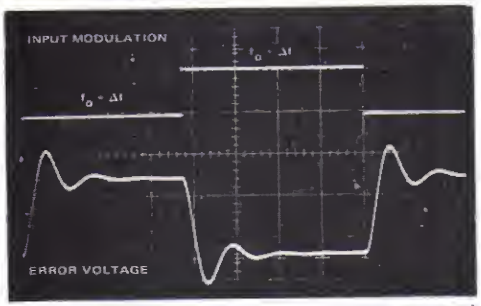


Figure 8–17a $[C_{ext} > C_{crit}, R_{ext} = 0]$

CRITICALLY DAMPED $\zeta \approx 1$

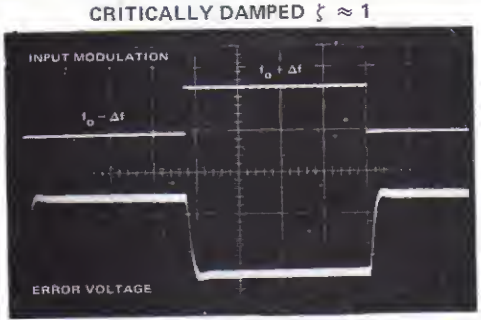


Figure 8–17b $[C_{ext} = C_{crit}, R_{ext} = 0]$

OVERDAMPED $\zeta \approx 10$

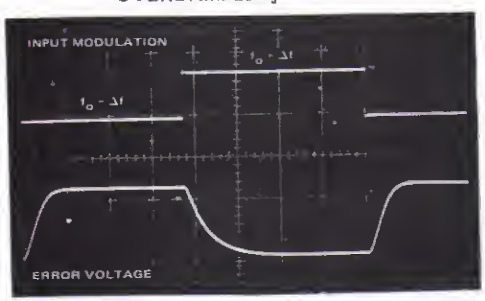


Figure 8–17c $[C < C_{crit}, R_{ext} > 0]$

HIGHLY OVERDAMPED $\zeta > 10$

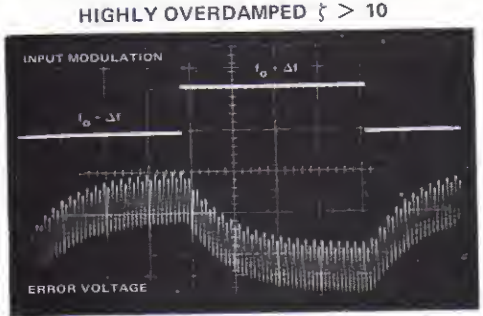


Figure 8–17d $[C << C_{crit}, R_{ext} = 0]$

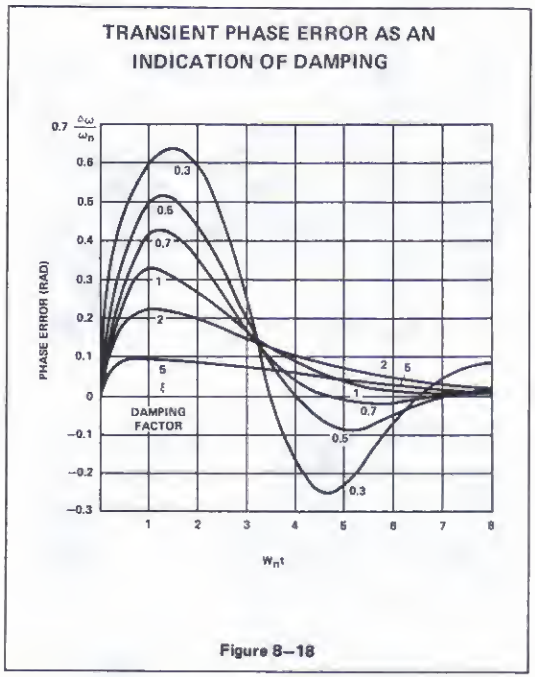


Figure 8–18

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB-down point will give the damping. Table 8–3 gives the approximate relationship.

ESTIMATING DAMPING FROM MODULATING FREQUENCY (ω_m) RESPONSE

ζ	PEAK AMPLITUDE / LOW FREQUENCY AMPLITUDE	$\frac{\omega_{-3dB}}{\omega_n}$
.3	6.0dB	1.8
.5	3.2dB	2.1
.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	.5dB	10

NOISE EFFECTS

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the ±90° permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

SIMPLIFIED MEASUREMENT EQUIPMENT

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low-cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. (See the applications in this section.) Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to dc, the calibration may be done in steps. Moreover, Gardner* shows how loop measurements may be made by applying a *constant* frequency to the loop input and the modulating signal to the low pass filter terminal to simulate the effect of a FM input so that a FM generator may be omitted for many measurements.

*see references

SIGNETICS MONOLITHIC PHASE LOCKED LOOPS

DETAILED DESCRIPTION OF 560B, 561B AND 562B

The 560B, 561B and 562B phase locked loops are all derived from the same monolithic die with different metal interconnections. Each device contains the same VCO, phase detector and voltage regulator stage and, hence, the basic loop parameters are the same for all three circuits.

The 560B is the most fundamental of the three circuits, having a block diagram equivalent to that shown in Figure 8–1. The actual circuit diagram is shown in Figure 8–19.

SCHEMATIC DIAGRAM OF 560B

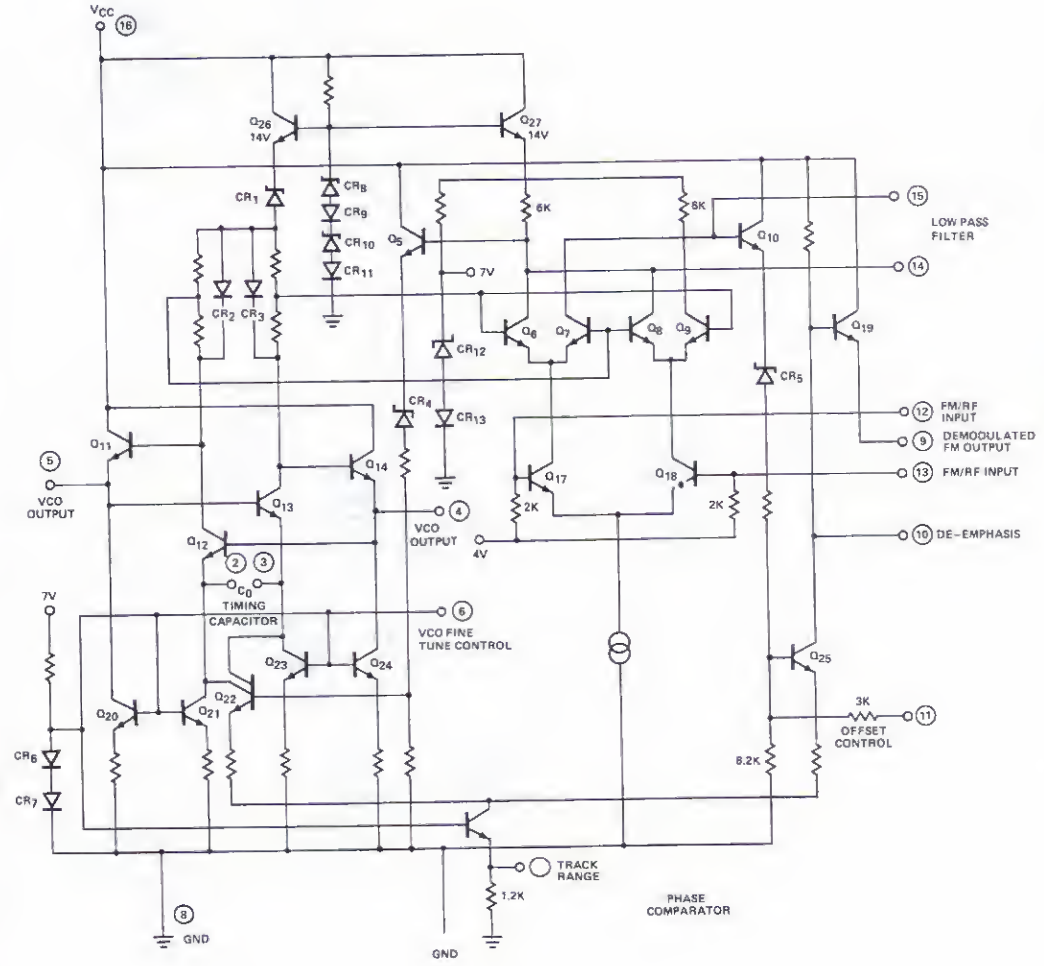


Figure 8–19

The VCO is a high frequency emitter-coupled multivibrator formed by transistors Q_{11}–Q_{14}. It operates from a regulated 7.7V supply formed by 6.3V supply formed by Zener diode CR_1 (a reverse-biased base-emitter junction) in series with the 14V regulated supply. The VCO frequency is thus immune from supply voltage variations. Four constant current sources formed by Q_{20}, Q_{21}, Q_{23}, Q_{24}, and biased by CR_6 and CR_7 supply operating current for the VCO. Voltage control of the frequency is achieved by a differential amplifier, Q_{22} and Q_{25}. As the base voltage of Q_{22} increases with respect to the base voltage of Q_{25}, additional current is supplied to the emitters of Q_{12} and Q_{13}, increasing the charge and discharge current of the timing capacitor C_o, increasing the VCO frequency. Reducing the base voltage of Q_{22} with respect to Q_{25} similarly reduces the VCO frequency. Two Zener diodes and two transistors, CR_4, CR_5, Q_5 and Q_{10}, respectively, provide level shifting which allows the VCO to be driven by the outputs of the phase detector.

The phase detector is a doubly-balanced multiplier formed by transistors Q_6–Q_9, Q_{17} and Q_{18}. Signal input is made to the lower stage, biased at about 4V by means of 2kΩ base resistors. The upper stage is biased and driven directly by the VCO output taken from the collector resistors of Q_{12} and Q_{13}. A differential output signal is available between the collectors of Q_6 (and Q_8) and Q_7 (and Q_9). An external network, together with the 6K collector resistors, comprises the low pass filter. The phase detector is operated from regulated 14V appearing at the emitter of Q_{27}. A resistor in the collector of Q_{25} can be shunted with an external capacitor to form a de-emphasis filter. The de-emphasized signal is buffered by emitter follower Q_{19} before being brought out.

The TRACK RANGE input, pin 7 on all three loops, allows the user to control the total current flowing through the frequency controlling differential amplifier Q_{22}, Q_{25}. This is done by controlling the effective emitter resistance of Q_{29}, the current source for Q_{22}, Q_{25}. Current may be added or subtracted at pin 7 to, respectively, reduce or increase the tracking range.

SCHEMATIC DIAGRAM OF 561B

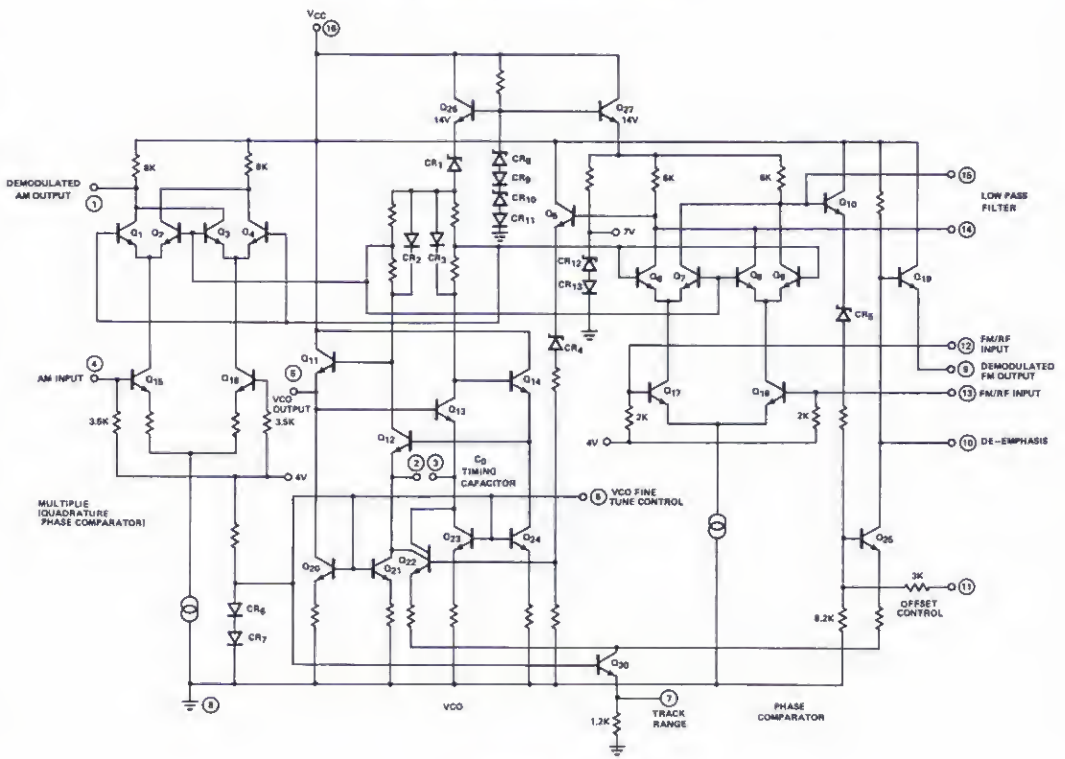


Figure 8–20

The 561, shown in Figure 8–20, contains all of the circuitry of the 560 and in addition, has a quadrature phase comparator. This enables it to be used as a synchronous AM detector. The quadrature phase detector consists of transistors Q_1–Q_4 and Q_{15}, Q_{16} which are biased and driven in the same manner as the loop phase detector. However, the quadrature detector input is single ended rather than differential (as the loop phase detector input) and an external 90° phase shift network is required to provide the proper phase relations. The demodulated AM output is brought out at pin 1.

The 562, shown in Figure 8–21, is basically the same as the 560 except that the loop is broken between the VCO and phase comparator. This allows a counter to be inserted in the loop for frequency multiplication applications. Transistors Q_1–Q_4 provide low impedance differential VCO outputs (pins 3 and 4), and the upper stage phase detector inputs are brought out of the package (pins 2 and 15). A bias voltage is brought out through pin 1 to provide a convenient bias level for the upper stage of the phase detector.

SCHEMATIC DIAGRAM OF 562B

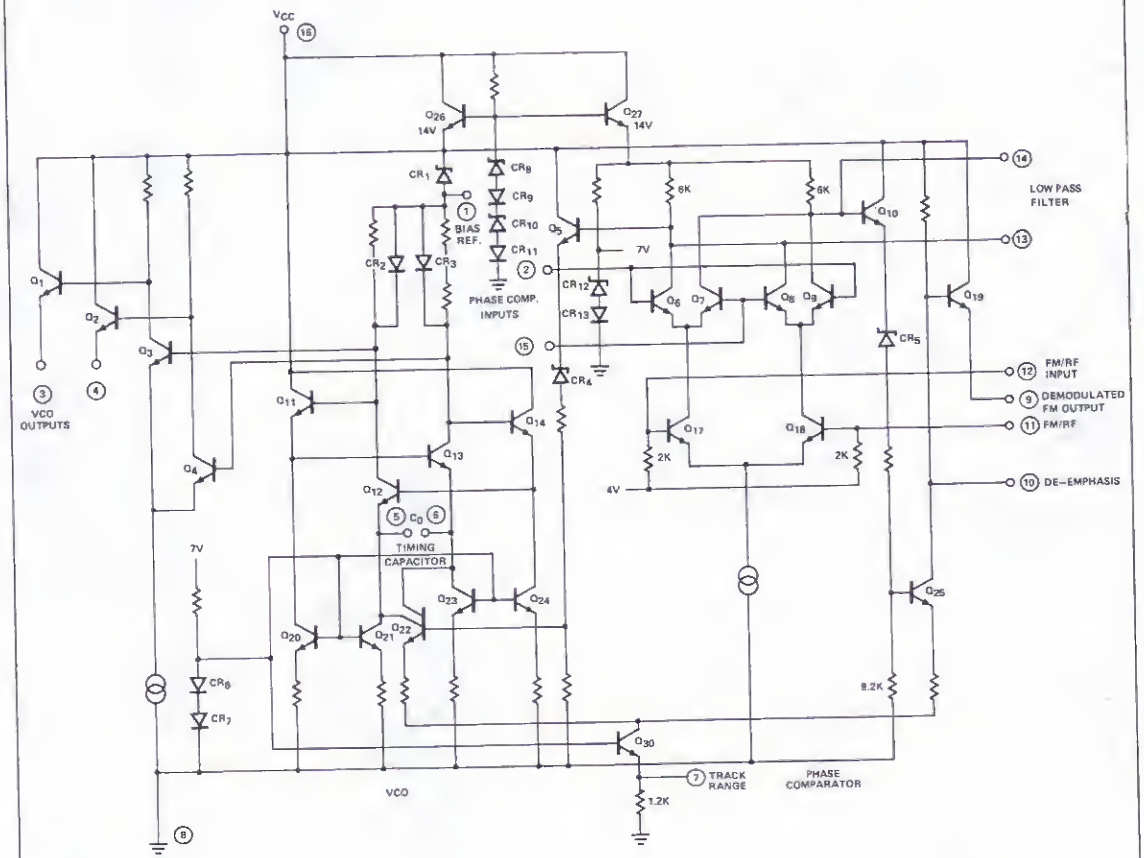


Figure 8–21

INTERFACING

Connection of the Signetics 560B and 561B phase locked loops to external input and output circuitry is readily accomplished; however, as with any electrical system, there are voltage, current and impedance limitations that must be considered.

The inputs of the phase comparators in the 560B, 561B and 562B and the AM detector in the 561B are biased internally from a +4 volt supply; therefore, the input signals must be capacitively coupled to the PLL to avoid interfering with this bias. These coupling capacitors should be selected to give negligible phase shift at the input frequency and impedance of the PLL. (The capacitive impedance at the operating frequency should be as small as possible, compared to the input resistance of the PLL.)

The input resistance of the phase comparator is 2000Ω single-ended, and 4000Ω when differentially connected. The input resistance of the AM detector is 3000Ω. The signal input to the phase comparator may be applied differentially if there is a common mode noise problem; however, in most applications, a single-ended input will be satisfactory. When inputs are not used differentially, the unused input may be ac-coupled to ground to double the phase detector gain at low input amplitudes.

The amplitude of the input signal should be adjusted to give optimum results with the PLL. Signals of less than 0.2mV rms may have an unsatisfactory signal-to-noise ratio; signals exceeding 25mV rms will have reduced AM rejection (less than 30dB). The AM detector will handle input signals up to 200mV peak-to-peak without excessive distortion, and will handle up to 2V peak-to-peak where distortion is not a factor.

Interfacing of the available outputs is best described by referring to the following diagrams. Figure 8–22 shows the PLL VCO output as a clock circuit for logic pulse synchronization. Figures 8–22a and 8–22b show the 560B and 561B, respectively, connected directly to the clock circuit; however, this configuration may be limited by low voltage and the possibility of too large a capacitive load swamping the oscillator. Figures 8–22c and 8–22d show the PLL clock output for the 560B and 561B, respectively, using the 5710 Voltage Comparator as a buffer amplifier to provide an output voltage swing suitable for driving logic circuits. The power supply for circuits utilizing the 5710 is split (+12 and −6V dc).

VCO OUTPUT INTERFACING

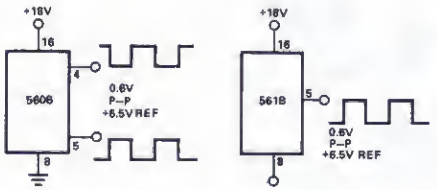


Figure 8–22a Figure 8–22b

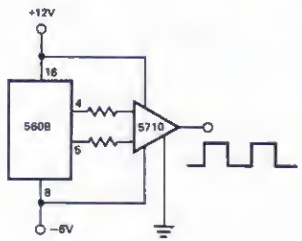


Figure 8–22c

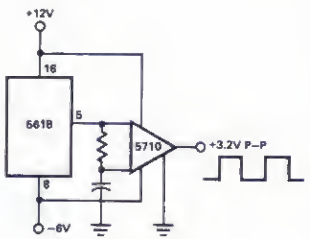


Figure 8–22d

In Figure 8–23a the 560B is a FM demodulator used for the detection of audio information on frequency modulated carriers. Since the lower frequency limit of this type of information is approximately 1Hz, capacitive coupling may be used. However, in some applications where carrier shifts occur at an extremely slow rate, direct coupling from the output to load is necessary. Figure 8–23b shows an alternate FM detector output configuration which should be used if a different output is desirable. In this case, the output is removed at pins 14 and 15. These pins are the terminals of the low pass filter and are in the line containing the demodulated signal. The signal level (single-ended) is about one-sixth of that at pin 9 so that additional amplification may be required.

FM DETECTOR INTERFACING

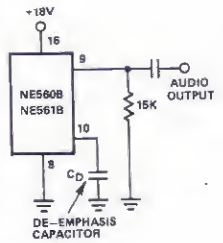


Figure 8–23a

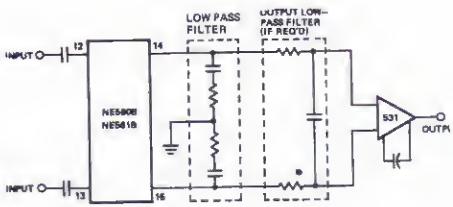


Figure 8–23b

DETECTOR INTERFACING (NE561B ONLY)

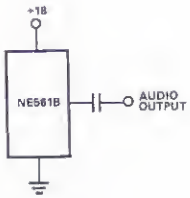


Figure 8–24a

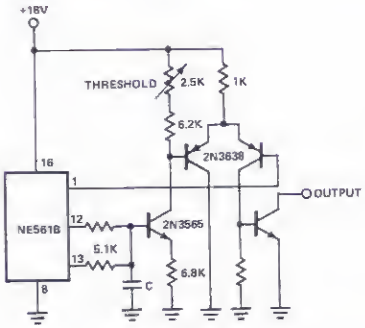


Figure 8–24b

Additional receiving modes are illustrated in Figure 8–24 for the 561B only. Figure 8–24a shows the 561B output when used as an AM detector; note the straight capacitive coupling. Figure 8–24b shows the 561B used as a continuous wave detector. Since this version of the circuit is for the detection of CW or AM signals, external circuitry must be incorporated for use with CW inputs. With a CW input applied, there will be a dc shift at the output of the AM detector, pin 1. This shift is small compared to the no-signal dc level and may be difficult to detect in relation to power supply voltage changes. Therefore, a reference must be generated to track any power supply voltage variations and to compensate for internal PLL thermal drift. This is best accomplished by simulating a portion of the PLL internal structure. The 2N3565 npn transistor is used as a constant-current source. Its reference voltage is obtained from an internal PLL bias source at pins 12 and 13, with the current level established by the 6.8K resistor. The 6.2K resistor and the 2.5K potentiometer simulate the PLL output resistance. The differential amplifier, composed of two 2N3638 pnp transistors, amplifies the dc output and allows it to drive a npn transistor referenced to ground. This type of circuit may also be used as a tone detector or to sense that the PLL is locked to an incoming signal.

The 562 phase locked loop is especially designed for utilizing the output of the VCO. In this configuration, an amplifier-buffer has been added to the VCO to provide differential square wave outputs with a 4.5V amplitude (see block diagram Figure 8–25). This facilitates the utilization of the frequency stabilized VCO as a timing or clocking signal. The outputs (pins 3 and 4) are emitter-followers and have no internal load resistors; therefore, external 3K to 12K Ω load resistors are required.

BLOCK DIAGRAM OF 562B

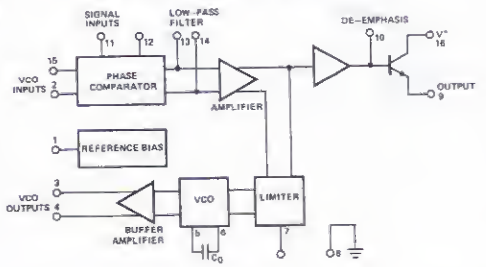


Figure 8–25

It is essential that the resistance from each pin to ground be equal in order to maintain output waveform symmetry and to minimize frequency drift. When locking the VCO output to the phase comparator (pins 3 to 2 for single-ended connection), capacitive coupling should be used. If a signal exceeding 2V is to be applied, a 1K Ω resistor should be placed in series with the coupling capacitor. This resistor may be part of the load resistance of 12K Ω, by using two resistors (1K and 11K) to form the VCO load, as shown in Figure 8–26.

ATTENUATING INPUT TO 562B PHASE DETECTOR

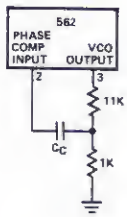


Figure 8–26

The output from the VCO is a minimum of 3V peak-to-peak, but has an average level of 12V dc; that is, it oscillates from 10.5 to 13.5V. To utilize this output with logic circuits, some means of voltage level shifting must be used. Figures 8–27 and 8–28 show two methods of accomplishing level shifting. These circuits will operate satisfactorily to 20MHz.

The phase comparator inputs of the 562B (pins 2 and 15) must be biased by connecting a 1K Ω resistor from each pin to the 8V bias supply available at pin 1. Pin 1 should be capacitively bypassed to ground. The inputs to the phase comparator should be capacitively coupled.

LEVEL SHIFTING 562B VCO OUTPUT FOR DRIVING LOGIC

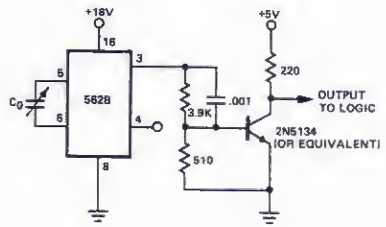


Figure 8–27

LEVEL SHIFTING 562B VCO OUTPUT FOR DRIVING LOGIC

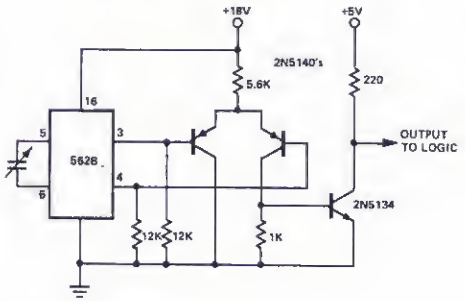


Figure 8–28

DETAILED DESCRIPTION OF 565

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. Functionally, the circuit is similar to the 562 in that the loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 8–29. I_1 is the charging current created by the application of the control voltage V_c. In the initial state, Q_3 is off and the current I_1 charges capacitor C_1 through the diode D_2. When the voltage on C_1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q_3. This provides a current sink and essentially grounds the emitters of Q_1 and Q_2 to become reverse biased. The charging current I_1 now flows through D_1, Q_1 and Q_3 to ground. Since the base-emitter voltage of Q_2 is the same as that of Q_1, an equal current flows through Q_2. This discharges the capacitor C_1 until the lower triggering threshold is reached at which point the cycle repeats itself. Because the capacitor C_1 is charged and discharged with the constant current I_1, the VCO produces a triangle wave form as well as the square wave output of the Schmitt trigger.

SIMPLIFIED DIAGRAM OF 565 VCO

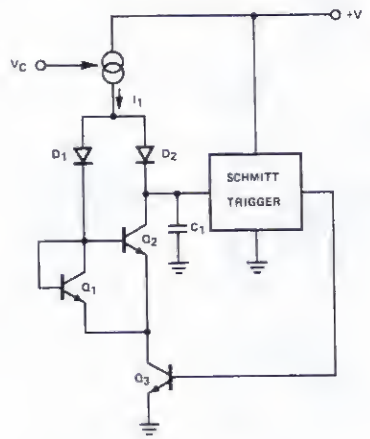


Figure 8–29

The actual circuit is shown in Figure 8–30. Transistors Q_1–Q_7 and diodes D_1–D_3 form the precision current source. The base of Q_1 is the control voltage input to the VCO. This voltage is transferred to pin 8 where it is applied across the external resistor R_1. This develops a current through R_1 which enters pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q_1 base current, all the current that enters pin 8, appears at the anodes of diodes D_2 and D_3. When Q_8 (controlled by the Schmitt trigger) is on, D_3 is reverse biased and all the current flows through D_2 to the duplicating current source Q_5–Q_7, R_2–R_3 and appears as the capacitor discharge current at the collector of Q_5. When Q_8 is off, the duplicating current source Q_5–Q_7, R_2–R_3 floats and the charging current passes through D_3 to charge C_1.

The Schmitt trigger (Q_{11}, Q_{12}) is driven from the capacitor triangle wave form by the emitter follower Q_9. Diodes D_6–D_9 prevent saturation of Q_{11} and Q_{12}, enhancing the switching speed. The Schmitt trigger output is buffered by emitter follower Q_{13} and is brought out to pin 4, and is also connected back to the current source by the differential amplifier (Q_{14}–Q_{16}).

SCHEMATIC DIAGRAM OF 565

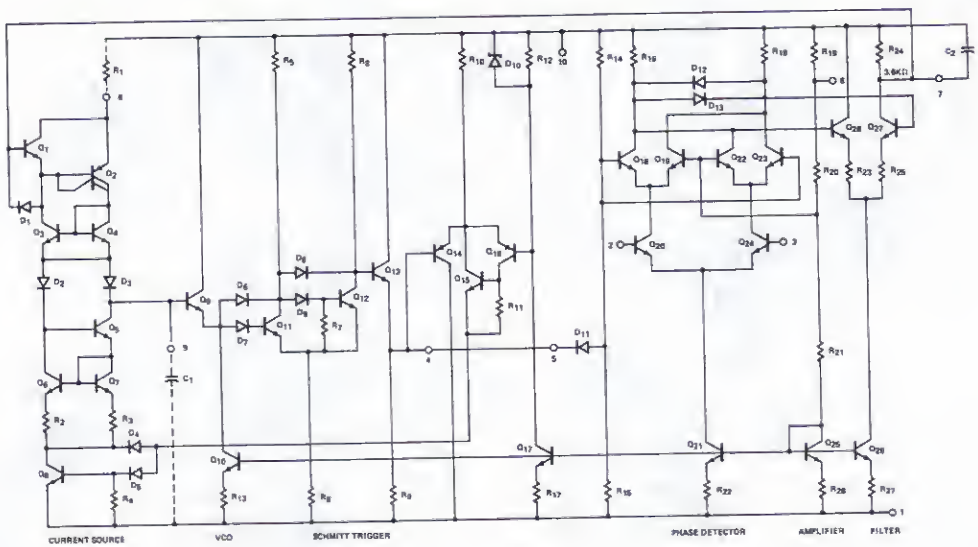


Figure 8–30

When operated from dual symmetrical supplies, the square wave on pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below positive supply. The triangle wave form on pin 9 is approximately centered between positive and negative supply and has an amplitude of 2V with supply voltages of ±5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase detector is again of the doubly-balanced modulator type. Transistors Q_{20} and Q_{24} form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q_{20} and Q_{24} through external resistors to ground. The switching stage Q_{18}, Q_{19}, Q_{22} and Q_{23} is driven from the Schmitt trigger via pin 5 and D_{11}. Diodes D_{12} and D_{13} limit the phase detector output, and differential amplifier Q_{26} and Q_{27} provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to pin 7) and the collector resistance R_{24} (typically 3.6K Ω). The voltage on pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q_1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is nominally equal to the output voltage on pin 7. This allows differential stages to be both biased and driven by connecting them to pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R_1 and C_1 and is given approximately by

$$f_o \simeq \frac{1.2}{4R_1C_1}$$

When the phase comparator is in the limiting mode (Vin ⩾ 200mV p-p), the lock range can be calculated from the expression:

$$2\omega_L = 2K_oK_dA\theta_d$$

where K_o is the VCO conversion gain, K_d is the phase detector gain factor, A is the amplifier gain and θ_d is the maximum phase error over which the loop can remain in lock.

For the 565: $K_o = \frac{50f_o}{V_{cc}}$ radians/sec/volt

(where f_o is the free-running frequency of the VCO and V_{cc} is the total supply voltage applied to the circuit.)

$$K_d = \frac{1.4}{\pi} \text{ volts/radian}$$

$$A = 1.4$$

$$\theta_d = \frac{\pi}{2} \text{ radians}$$

The lock range for the 565 then becomes:

$$f_L \cong \frac{\omega_L}{2\pi} \cong \frac{8f_o}{V_{cc}} \text{ Hz}$$

to each side of the center frequency, or a total range of:

$$2f_L \cong \frac{16f_o}{V_{cc}} \text{ Hz}$$

The capture range, over which the loop can acquire lock with the input signal is given approximately by:

$$2\omega_c \cong 2\sqrt{\frac{\omega_L}{\tau}}$$

where ω_L is the one-sided lock range

$$\omega_L = 2\pi f_L$$

and τ is the time constant of the loop filter

$$\tau = RC_2$$

with R = 3.6kΩ.

This can be written as:

$$f_c \cong \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}} = \pm\frac{1}{2\pi}\sqrt{\frac{32\pi f_o}{V_{cc}\tau}}$$

to each side of the center frequency or a total capture range of:

$$f_c \cong \frac{1}{\pi}\sqrt{\frac{32\pi f_o}{\tau V_{cc}}}$$

This approximation works well for narrow capture ranges ($f_c = 1/3f_L$) but becomes too large as the limiting case is approached ($f_c = f_L$).

DETAILED DESCRIPTION OF 566

The 566 is the voltage controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 8–31. Transistor Q_{18} has been a buffered triangle waveform output. (The triangle waveform is available at capacitor C_1 also, but any current drawn from pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q_{19} by pin 4. The circuit will operate at frequencies up to 1MHz and may be programmed by the voltage applied on the control terminal (pin 5), current injected into pin 6 or the value of the external resistor and capacitor (R_1 and C_1).

SCHEMATIC DIAGRAM OF 566

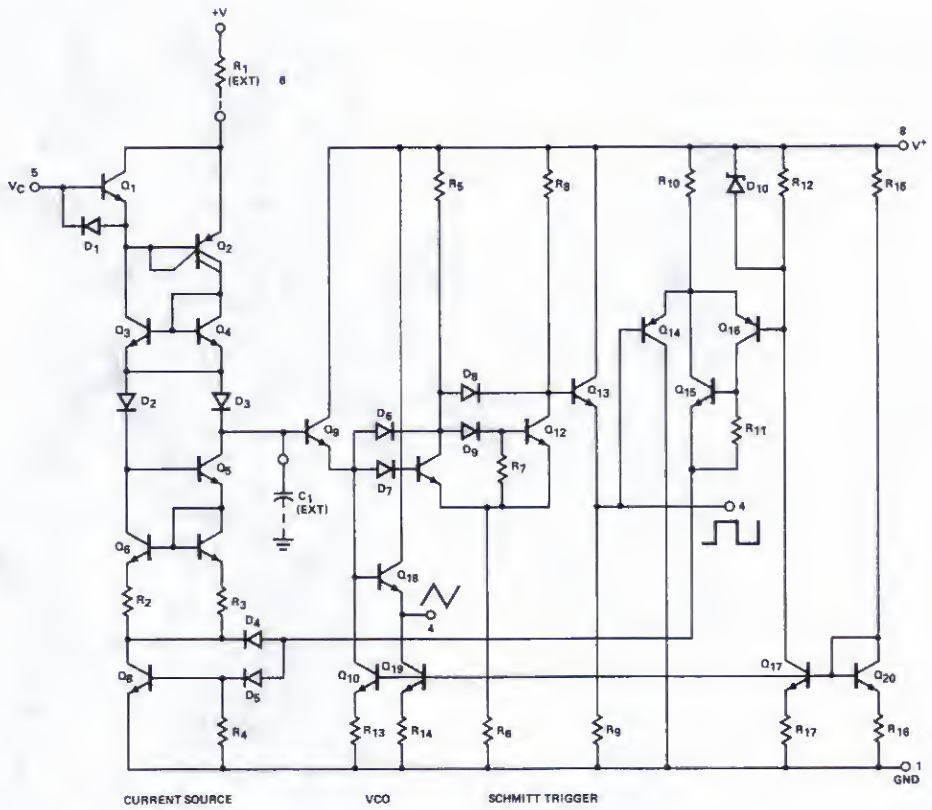


Figure 8–31

DETAILED DESCRIPTION OF 567

The 567 is a PLL designed specifically for frequency sensing or tone decoding. Like the 561, the 567 has a controlled oscillator, a phase detector and a second auxiliary or quadrature phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature phase detector output. During lock, the quadrature phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder center frequency and bandwidth are specified by the center frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range.

The current controlled oscillator is shown in simplified form in Figure 8–32. It provides both a square wave output and a quadrature output. The control current I_c sweeps the oscillator ±7% of the center frequency, which is set by external components R_1 and C_1. It operates as follows:

Transistors Q_1 through Q_6 form a flip-flop which can switch pin 5 between V_{be} and $V^+ - V_{be}$. Thus, the R_1C_1 network is driven from a square wave of $V^+ - 2V_{be}$ peak-to-peak volts. On the positive portion of the square wave, C_1 is charged through R_1 until V_1 is reached. A comparator circuit driven from C_1 at pin 6 then supplies a pulse which resets the flip-flop so that pin 5 switches to V_{be} and C_1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop and C_1 resumes charging.

SIMPLIFIED DIAGRAM OF 567 TONE DECODER CCO

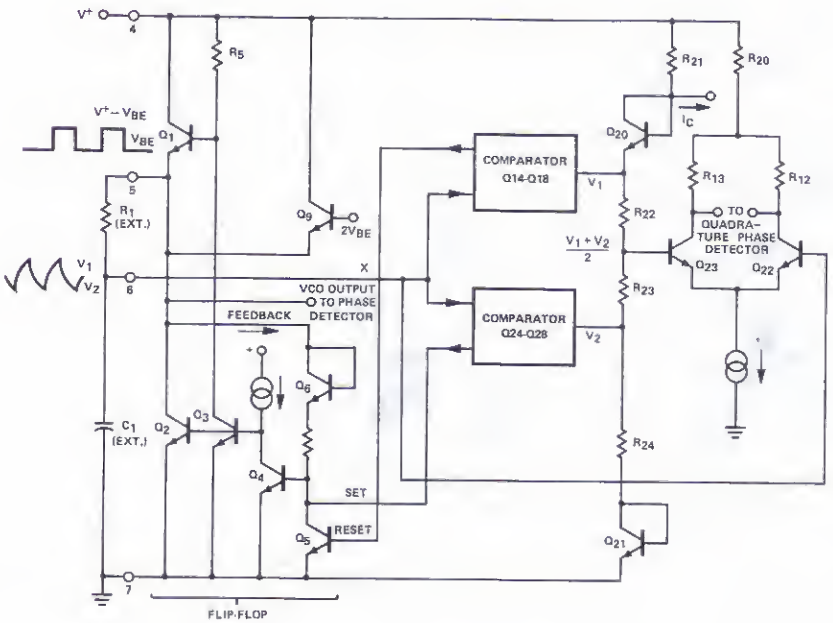


Figure 8–32

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

$$V_1 - V_2 = (V^+ - 2V_{be}) \frac{R_{22} + R_{23}}{R_{21} + R_{22} + R_{23} + R_{24}}$$

$$= K\,(V^+ - 2V_{be})$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 8–33 shows the pin 5 and pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of V^+ and dependent only on the time constant R_1C_1 of the external components. Moreover, if $(V_1 + V_2)/2 = V^+/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase shifted from the square wave. A differential stage (Q_{22} and Q_{23}) amplifies the triangular wave with respect to $(V_1 + V_2)/2$ to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase shifted about 80°, but no operating compromises result from this slight deviation from true quadrature.)

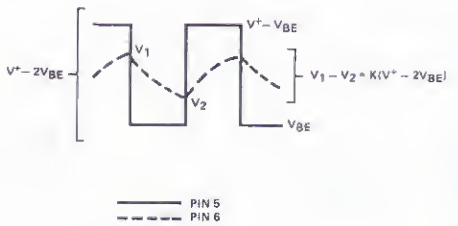


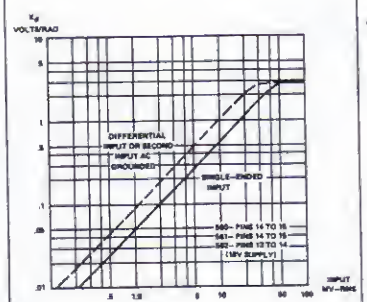
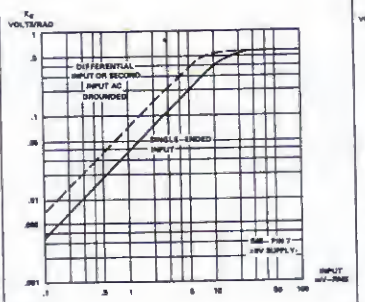
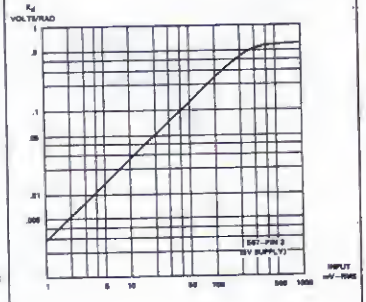
Figure 8–33

One source of error in this oscillator scheme is current drawn by the comparators from the R_1C_1 mode. An emitter follower, therefore, is inserted at X to minimize this drain and Q_{21} placed in series with Q_{20} to drop the comparator sensing voltage one V_{be} to compensate for the V_{be} drop in the emitter follower.

LOOP GAIN CONSTANTS (K_o, K_d)

Table 8–4 gives the gain constants (K_o, K_d) for the Signetics' loops. The values given are for the standard connection with no gain reduction or tracking adjustment components connected. The dc amplifier gain A has been included in either the K_o or K_d value, depending on which side of the low pass filter terminals the gain is present. This causes no hardship in calculations since the loop gain K_v becomes simply K_oK_d.

PLL GAIN CONSTANTS* K_oK_d ($K_v = K_oK_d$)

	560B, 561B, 562B	565	567
K_o	$0.32\ \omega_o \frac{\text{rad.}}{\text{sec-volt}}$ Single-Ended Input to VCO $0.64\ \omega_o \frac{\text{rad.}}{\text{sec-volt}}$ Differential Input to VCO	$\frac{8.0\ \omega_o}{\text{Total Supply Voltage}}$ $= 0.67\ \omega_o \frac{\text{rad.}}{\text{sec-volt}}$ at ±6 volts	$0.44\ \omega_o \frac{\text{rad.}}{\text{sec-volt}}$
K_d			

*The dc amplifier gain A has been included in K_o or K_d, depending on which side of the LPF terminals the amplifier is located.

Table 8–4

In order to insure that the square wave drops quickly and accurately to V_{be}, an active clamp scheme is applied to the collector of Q_2. The base of Q_9 is held at 2 V_{be} so that as Q_2 is turned on by its base current, its collector is held at V_{be}. Because Q_2 and Q_3 have the same geometry and their base-emitter voltages are the same, the maximum Q_2 current when clamped is essentially the same as the collector current of Q_3 (as limited by R_5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making R_{21} somewhat less than R_{24} and restoring the proper voltage for 50% duty cycle by drawing I_c of 100μA for the R_{21}, Q_{20} junction. When I_c is then varied between 0 and 200μA, the frequency changes by ±7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_c, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of center frequency with temperature and supply voltage changes when $I_c \neq 0$, I_c is also made a function of $V^+ - 2V_{be}$.

The CCO circuit is shown in the tone decoder schematic diagram, Figure 8–34.

SCHEMATIC DIAGRAM OF 567

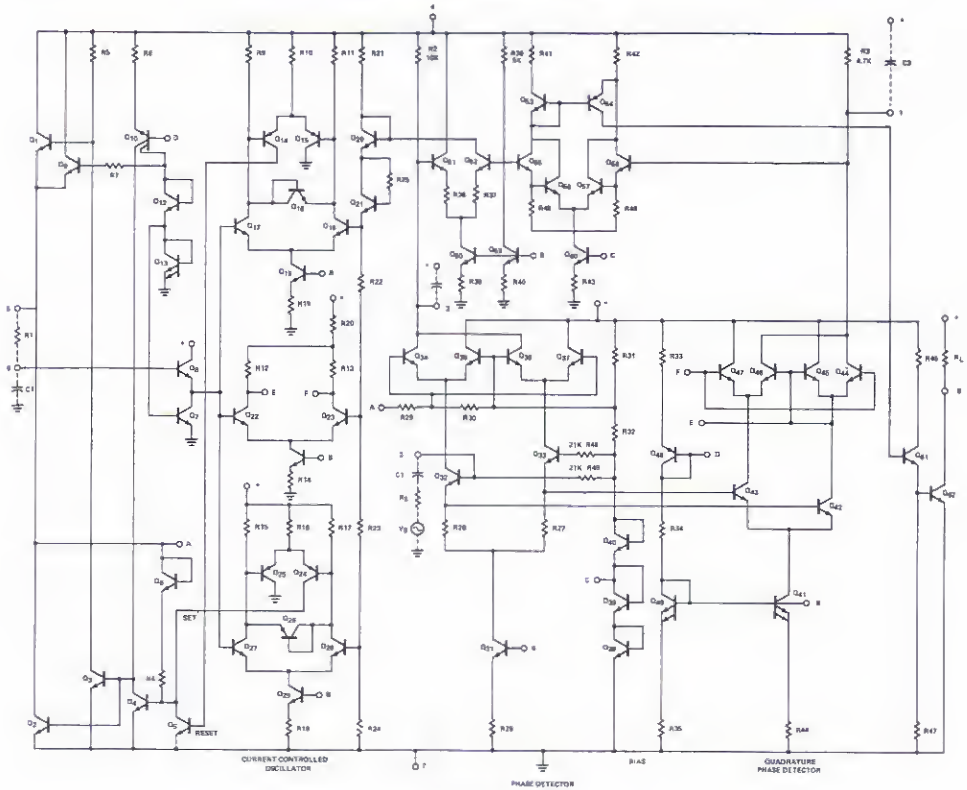


Figure 8–34

A doubly-balanced multiplier formed by Q_{32} through Q_{37} (Figure 8–34) functions as the phase detector. The input signal is applied to the base of Q_{32}. Transistors Q_{34} – Q_{37} are driven by a square wave taken from the CCO at the collector of Q_2. Phase detector input bias is provided by three diodes, Q_{38} through Q_{40}, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R_{26} and R_{27}, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop dc amplifier is formed by Q_{51} and Q_{52}. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full ±7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mV rms. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels since this greatly facilitates operation of the quadrature lock detector. Emitter resistors R_{36} and R_{37} help stabilize the gain over the required temperature range. Another function of the dc amplifier is to allow a higher impedance level at the low pass filter terminal (pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter resistors help stabilize the loop gain over the temperature range.

The quadrature phase detector (QPD), formed by a second doubly-balanced multiplier Q_{42} – Q_{47}, is driven from the quadrature output (E, F, in Figure 8–34) of the CCO. The signal input comes from the emitters of the input transistors Q_{32} and Q_{33}.

The output stage, Q_{53} through Q_{62}, compares the average QPD current in the low pass output filter R_3C_3 with a temperature compensated current in R_{39} (forming the threshold voltage V_t).

Since R_3 is slightly lower in value than R_{39}, the output stage is normally off. When the lock and the QPD current I_q occurs, pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (pin 8) of the power npn output transistor can drive both 100 – 200mA loads and logic elements, including TTL.

EXPANDING LOOP CAPABILITY

LOW PASS FILTER CIRCUITS (560B, 561B and 562B)

The low pass filters used with the 560B, 561B and 562B are externally adjusted to provide the desired operational characteristics. To select the most appropriate type of filter and component values, a basic understanding of filter operation is required.

A FM signal to be demodulated is matched in the phase comparator with the voltage controlled oscillator signal, which is tuned to the FM center frequency. Any resulting phase difference between these two signals is the demodulated FM signal. This demodulated signal is normally at frequencies between dc and upper audio frequencies.

The choice of low pass filter response gives a degree of design freedom in determining the capture range or selectivity of the loop. The attenuation of the high frequency error components at the output of the phase detector enhances the interference rejection characteristics of the loop. The filter also provides a short-term memory for the PLL that ensures rapid recapture of the signal if the system is thrown out of lock due to a noise transient.

To ensure absolute closed loop stability at all signal levels within the dynamic range of the loop, the open loop PLL is required to have no more than 12dB per octave high frequency roll-off.

The capacitor in each filter circuit shown in Figure 8–35 will provide 6dB per octave roll-off at the first break point–the desired bandwidth frequency. The resistance Rx shown in filters (c) and (d) is used to break the response up at high frequencies to ensure 6dB per octave roll-off at the loop unity gain frequency. Rx is typically between 50 and 200Ω.

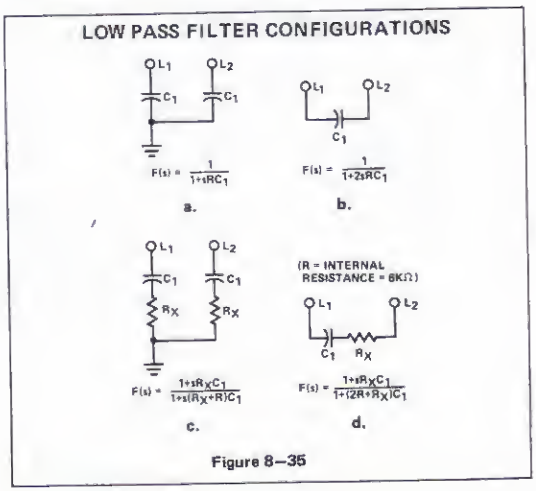


Figure 8–35

Calculation of values for low pass filters shown can be made using the complex second-degree transfer function equations given, or approximated using the equation: $C_1 = \frac{26.60}{f}$ mfd for filters (a) and (c), and the equation: $C_1 = \frac{13.30}{f}$ mfd for filters (b) and (d) where f is the desired first break frequency in Hz.

At frequencies greater than 5MHz where the loop may be prone to instability, filters (a) and (c) should be used. For operation at low frequencies, a simple type (b) lag filter with no added resistance is usually sufficient.

OPERATING FREQUENCY EXTENSION TO 60MHz (560B, 561B, 562B)

The frequency range of the 560B, 561B and 562B phase locked loops may be extended to 60MHz by the addition of two 10K Ω resistors from the timing capacitor terminals to the negative power supply as shown in Figure 8–36. The inclusion of a 5K Ω potentiometer between these 10K Ω resistors and the negative supply provides a simple method of fine tuning.

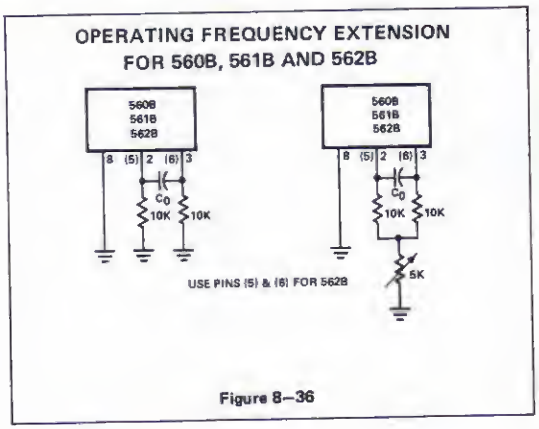


Figure 8–36

INCREASED LOOP OUTPUT VOLTAGE FOR SMALL FREQUENCY DEVIATIONS (565)

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into pin 8 and increase the value of R_1. One scheme for this is shown in Figure 8–37. The basis for this scheme is the fact that the output voltage controls only the current through R_1 while the current through Q_1 remains constant. Thus, if most of the charging current is due to Q_1, the total current can be varied only a small amount due to the small change in current through R_1. Consequently, the VCO can track the input signal over a small frequency range yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

NARROW BANDWIDTH FM DEMODULATOR

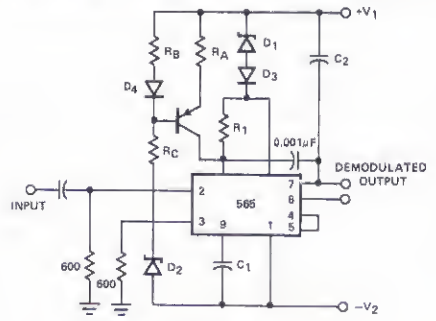


Figure 8–37

Diode D_1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available. D_4 is a diode which should be matched to the emitter-base junction of Q_1 for temperature stability. In addition, D_1 and D_2 should have the same breakdown voltages and D_3 and D_4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across pins 10 and 1 of the phase locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The center frequency can be found by:

$$f_o \simeq \frac{2R_B}{(R_B + R_C)\, R_A C_1} \div \frac{1}{4R_1 C_1} \text{ Hz}$$

and the total lock range is given by:

$$2\Delta f_L \simeq \frac{22.4 V_D (R_B+R_C) R_A f_o}{(|V_1|+|V_2|-V_z-V_D)(8R_B R_1 + R_A[R_B+R_C])} \text{ Hz}$$

where:
- V_D = forward biased diode voltage $\simeq$ 0.7V
- V_z = Zener diode breakdown voltage
- V_1 = positive supply voltage
- V_2 = negative supply voltage
- f_o = free-running VCO center frequency

When the output excursion at pin 7 need be only a volt or so, diodes D_1, D_2 and D_3 may be replaced by short circuits.

The value of R_1 can be selected to give a prescribed output voltage for a given frequency deviation.

$$R_1 = \frac{R_A(R_B+R_C)\, f_o}{R_B(|V_1|+|V_2|-0.7)\, \Delta f}$$

where f_o is the center frequency and Δf is the desired frequency deviation per volt of output.

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For best temperature stability, diode D_1 should be a base-collector shorted transistor of the same type as Q_1.

EXPANDED LOCK RANGE (565)

When the 565 is connected normally, feedback to the VCO from the phase detector is internal. That is, an amplifier makes the pin 8 voltage track the pin 7 (phase detector output) voltage. Since the capacitor C_1 charge current is determined by the current through resistance R_1, the frequency is a function of the voltage at pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into pin 8 is no longer a function of the pin 8 voltage but only of the pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 8–38 shows such a circuit in which the 5741 operational amplifier is set for a differential gain of 5, feeding current to pin 8 through the 33K resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the user should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500μA which also specifies the pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

EXPANDED LOCK RANGE CONFIGURATION FOR 565

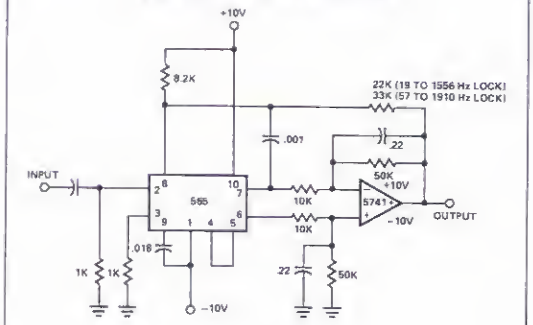


Figure 8–38

BREAKING THE INTERNAL FEEDBACK LOOP (565)

Many times it would be advantageous to be able to break the feedback connection between the output (pin 7) and the control voltage terminal (Q_1) of the VCO. This can be easily done once it is seen that it is the *current* into pin 8 which controls the VCO frequency. If the external resistor R_1 is replaced with a current source, such as in Figure 8–39, we have effectively broken the internal voltage feedback connection. The current flowing into pin 8 is now independent of the voltage on pin 8. The output voltage (on pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 8–39. This scheme allows the addition of enough

gain for the loop to stay in lock over a 100:1 frequency range, or conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0^o and 180^o. In addition, it is now possible to do special filtering to improve the performance in certain applications. For instance, in frequency multiplication applications it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

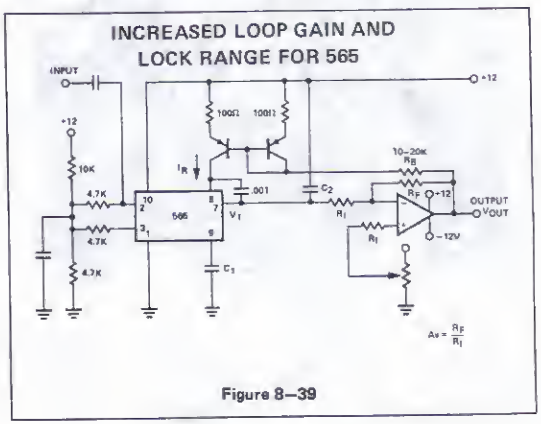


Figure 8–39

BREAKING THE INTERNAL FEEDBACK LOOP (560, 561, 562)

The internal control voltage feedback loop can also be easily broken on the 560, 561 and 562. The key in this case is to bias the range control terminal (pin 7) to +2V which turns off the controlled current source. Now the phase comparator output voltage will have no effect on the charging current which sets the VCO frequency. Now an external feedback loop can be built with the desired transfer function. Figure 8–40 shows a practical application of this principle. The control voltage is taken from across the low pass filter terminals, amplified, and used to add or subtract current into the timing capacitor nodes.

MINIMIZING TONE DECODER RESPONSE TIME (567)

The 567 Tone Decoder is a specialized loop which can be set up to respond to a given tone (constant frequency) within its bandwidth. The center frequency is set by a resistor R_1 and capacitor C_1 which determine the free-running frequency. The bandwidth is controlled by the low pass filter capacitor C_2. A third capacitor C_3 integrates the output of the quadrature phase detector (QPD) so that the dc lock-indicating component can switch the power output stage on when lock is present. The 567 is optimized for stability and predictability of center frequency and bandwidth.

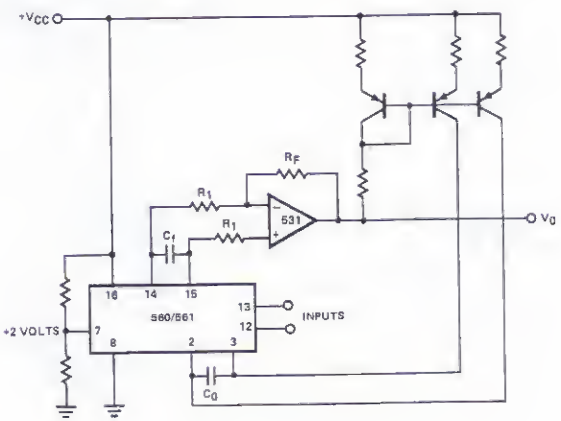


Figure 8–40

Two events must occur before an output is given. First, the loop portion of the 567 must achieve lock. Second, the output capacitor C_3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low pass filter. Thus, C_2 must be as small as possible. However, C_2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 8–41, reprinted from the 567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C_2 and the input amplitude is 200mV rms or greater. The response time is given in cycles of center frequency. For example, a 2% bandwidth at a center frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 8–42 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only 30/180 = 1/6 of the time will the lock-up time be longer than half the worst case lock-up time. Figure 8–43 shows some actual measurements of lock-up time for a set-up having a worst case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

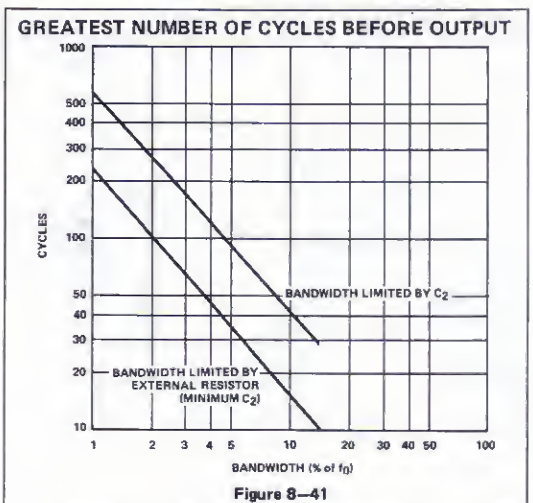


Figure 8–41

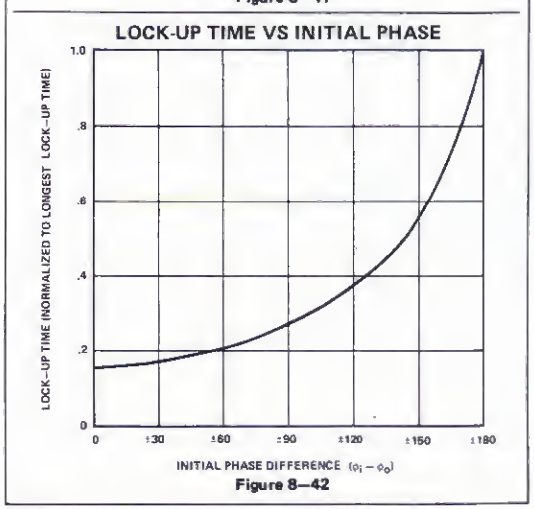


Figure 8–42

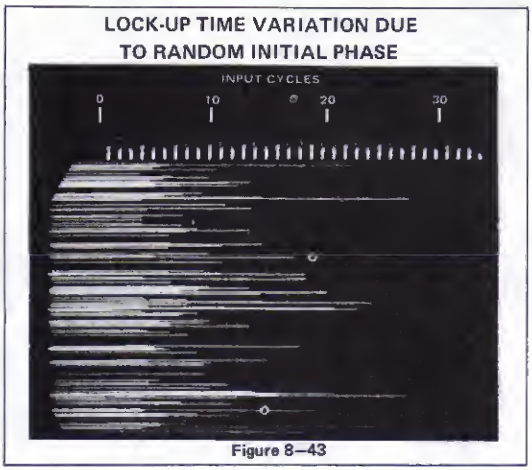


Figure 8–43

The lower curve on the graph shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C_2 required for this minimum response time is

$$C_2' = \frac{130}{f_o}\left[\frac{10K + R_A}{R_A}\right] \quad \mu F$$

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value (C_2') of C_2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect on the lock-up time—usually negligible in comparison to the variation caused by input phase.

Lock-up transients can be displayed on a two-channel scope with ease. Figure 8–44 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at pin 2, the low pass filter voltage. The input frequency is offset slightly from the center frequency so that the locked and unlocked voltage are different. It is apparent that, while the C_2 decay during unlock is always the same, the lock transient is different each time. This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing a favorable initial phase is created that is

not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C_2 or input amplitude is seen. However, *the repetition rate must be readjusted for worst-case lock-up after each such change.*

TONE DECODER LOCK-UP TRANSIENT

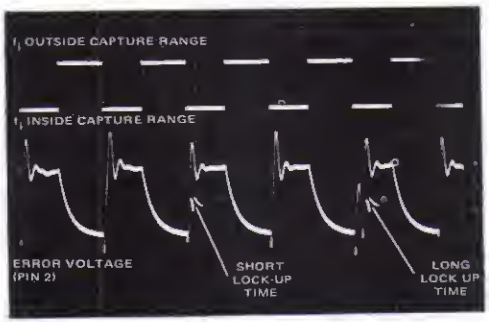


Figure 8–44

EFFECT OF THRESHOLD VOLTAGE (V_t) ADJUSTMENT ON TONE DECODER TURN-ON AND TURN-OFF DELAY

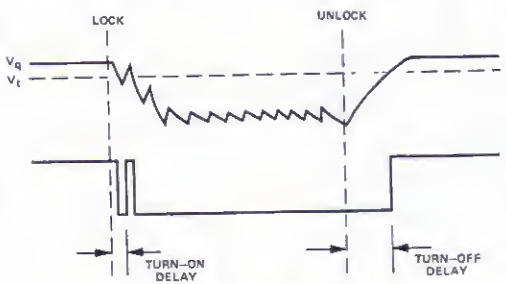


Figure 8–45a

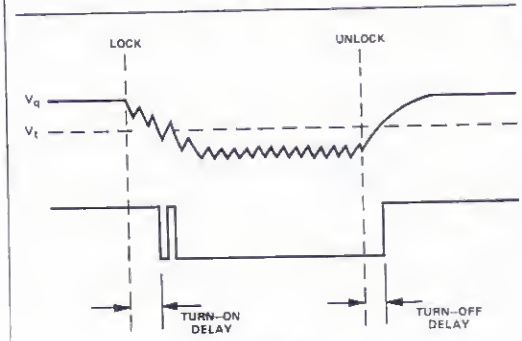


Figure 8–45b

Once lock is achieved, the quadrature phase detector output at pin 1 is integrated by C_3 to extract the dc component. As C_3 charges from its quiescent value V_q (see Figure 8–45) to its final value ($V_q - \Delta V$), it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant ($\tau = 4700C_3$) expires before V_t is crossed so that C_3 does not greatly influence the response time. However, as shown in Figure 8–45a, the turn-off delay time can be quite long when C_3 is large. Figure 8–45b shows how desensitizing the output stage by connecting a high-value resistor between pin 1 and pin 4 (plus supply) can equalize the turn-on and turn-off time. If turn-off delay is important in the overall response time, then desensitizing can reduce the total delay.

But why not make C_3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large twice-center-frequency component that must be filtered out. Also, noise, outband signals and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C_3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C_3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C_3. What must be done, then, is to make C_3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a.) After the center frequency has been set, adjust C_2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 8–43) suggests that worst case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction. (See data sheet.)

b.) Check lock-up time by observing the waveform at pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.

c.) Starting with a large value of C_3 (say 10 C_2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.

d.) Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.

e.) Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a.) Relax the bandwidth requirement.

b.) Operate the entire system at higher frequency when this option is available.

c.) Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurance of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.

d.) Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.

e.) If the system design permits, send the tone to be detected continuously at a low level (say 25mV rms) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing The signal amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as 1/3 to 1/2 the center frequency when C_3 is small. This is equivalent to ASK (amplitude shift keying).

FM IF AMPLIFIER/DEMODULATOR WITH MUTING (561B)

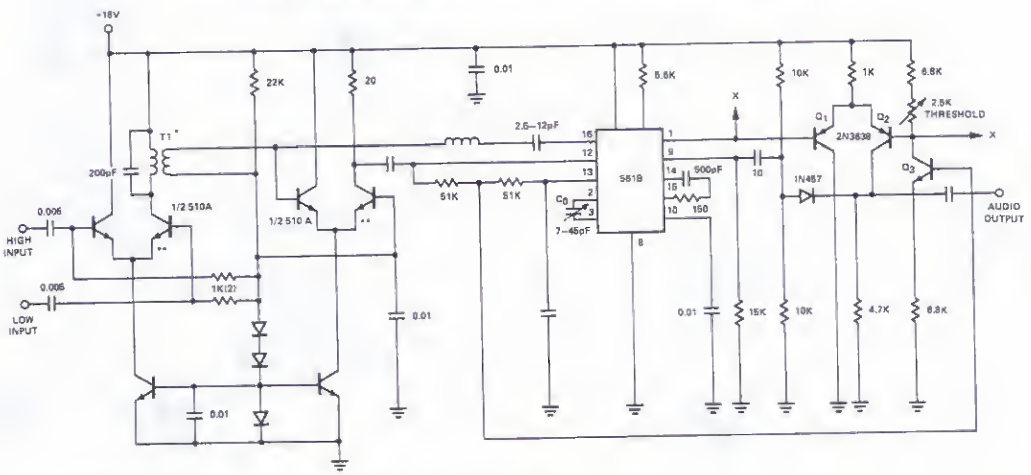
In this application, the loop portion of the 561B operates in the usual manner for FM demodulation. To introduce muting (squelch) the synchronous AM detector portion of the PLL is used to detect the presence of an input signal and to open a muting gate. Figure 8–46 shows a typical circuit incorporating the muting feature.

The input section of the circuit is a broad-band, amplifier-limiter. The tuned LC network at the AM input, pin 4, is adjusted to provide a 90° phase shift at the IF frequency. This network is adjusted for maximum output at pin 1, demodulated AM output, with a carrier applied at the IF frequency.

Three transistors at the right of the diagram (Q_1, Q_2 and Q_3) and the 1N457 diode form the muting gate. Gating is accomplished by applying the demodulated FM output through the 1N457 diode and by biasing the diode on and off as follows: During periods with no input applied, Q_1 is shut off and Q_2 conducts. Therefore, the diode is effectively back biased since its anode potential developed by the two 10K resistors across the power supply is approximately +13.5V. When an input is applied to the circuit, Q_1 is turned on and Q_2 shuts off, reducing its collector potential below 9V. Thus, the diode is forward biased and the demodulated IF output is gated through to the circuit output.

Muting threshold adjustment is accomplished using the 2.5K potentiometer. Transistor Q_3 is used as a bias generator for the differential pair, Q_1 and Q_2. In turn, the bias of Q_3 is obtained from internal PLL bias points at pins 12 and 13. Thus, the muting gate will track the PLL over wide temperature variations.

TYPICAL FM IF AMPLIFIER/DEMODULATOR WITH MUTING



* T1: 20 TURNS BIFILAR NO. 36 WIRE ON 1/2 –WATT RESISTOR BODY (FOR 10.7 MHz)
** PART OF NE510A

Figure 8–46

FM DEMODULATOR (560B)

When used as a FM demodulator, the 560B phase locked loop requires selection of external components and/or circuits to create the desired response. The areas to be considered are:

a.) Input Signal Conditioning
b.) Tuning – VCO Frequency
c.) Low Pass Filter Selection/Gain Adjustment
d.) Output Swing
e.) Tracking Range Adjustment
f.) De-emphasis Network Selection

Figure 8–47 illustrates schematically a typical FM demodulator with IF amplifier and limiter using the 560B PLL. The amplitude of the input signal has a pronounced effect on the operation. For the tracking range to be constant, the input signal level should be greater than 2mV rms. In addition, AM rejection diminishes at higher signal levels and drops to less than 20dB for signals greater than 30mV. If either the tracking range or AM rejection is critical, the input signal should be conditioned to be in the 2 to 10mV range, using either a limiter or a combination limiter-amplifier. This circuit should limit at the smallest input voltage that is expected.

TYPICAL FM DEMODULATOR WITH IF AMPLIFIER AND LIMITER USING THE 560B

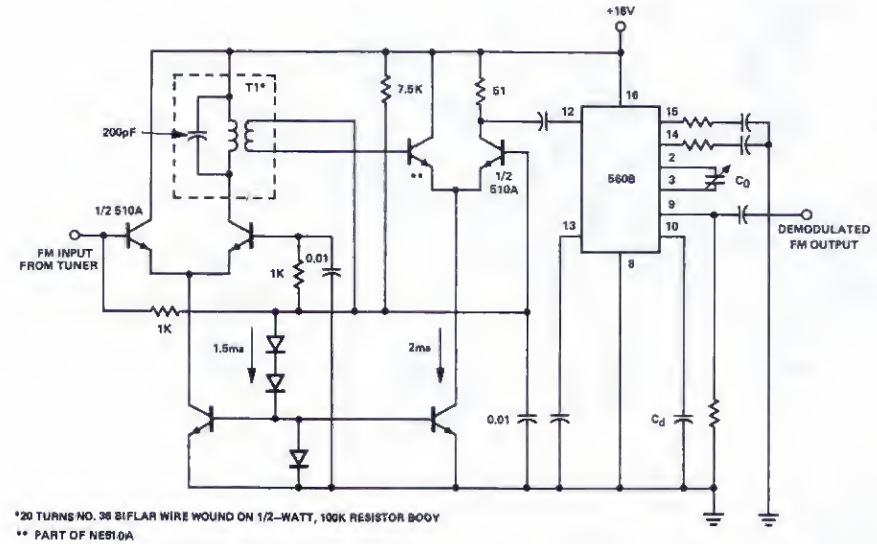


Figure 8–47

The PLL is tuned by adjusting the VCO to the center frequency of the FM signal. This is accomplished by connecting a capacitor across pins 2 and 3. The capacitor value is determined using the equation $C_0 \cong 300/f_0$, pF where f_0, the free-running VCO frequency, is in MHz. The exact value is not important as the internal resistors are only within ±10% of nominal value and fine tuning is normally required. Fine tuning may be accomplished by using a trimmer capacitor in parallel with C_0 or by using a potentiometer connected across the power supply with the rotor connected to pin 6 through a 200Ω current limiting resistor.

The dc gain of the loop, which sets the lock range and threshold sensitivity, can be controlled by the placement of a resistance between pins 14 and 15, the low pass filter terminals. A low pass filter connected to these terminals controls the capture range or selectivity of the loop. In basic terms, it may be said that the low pass filter sets the bandwidth of the demodulated information which will be obtained. For most applications, a single capacitor connected between pins 14 and 15 will provide the required filtering. The capacitance value required can be approximated as follows:

$$C \approx \frac{13.30}{f} \text{ mfd}$$

where f is the desired bandwidth in Hz. For example, if the desired information bandwidth is 15kHz, the required low pass filter capacitance will be:

$$C \approx \frac{13.30}{15000} = 885 \text{ pf}$$

The output swing is a function of the frequency deviation of the incoming signal, and is approximately 0.3V p-p for ±1% deviation. For example, a standard 10.7MHz IF frequency has a deviation of ±75kHz; therefore, the percentage deviation equals $\frac{\pm 0.75 \times 100}{10.7} = \pm 0.7\%$ and the output voltage will be 0.3V p-p x $\frac{.7\%}{1\%}$ = .21V p-p, or 74mV rms for 100% modulation.

The de-emphasis network requires an external capacitor from pin 10 to ground. This capacitor C_d and the 8000Ω internal resistance should produce a time constant of approximately 75μsec for standard FM broadcast demodulation. The value of the de-emphasis capacitor for this application is determined by the following formula:

$$C_d = \frac{75 \times 10^{-6}}{8000} = 0.0094 \text{ mfd}$$

For most applications, a 0.01mfd value would be satisfactory since the manufacturing tolerance of the resistor is on the order of 20%.

PHASE LOCKED AM RECEIVER (561B)

The Signetics 561B can be used as an AM detector/receiver. AM detection is accomplished as illustrated in the block diagram of Figure 8–48a. The phase locked loop is locked to the signal carrier frequency and its VCO output is used to provide the local oscillator signal for the product detector or synchronous demodulator. The PLL locks to its input signal with a constant 90^0 phase error. The amplitude of the signal at the output of the product detector is a function of the phase relationship of the carrier of the incoming signal and the local oscillator; it will be a maximum when the carrier and local oscillator are in phase or 180^0 out of phase and a minimum when they are in quadrature. It is, therefore, necessary to add a 90^0 phase shift network in the system to compensate for the normal PLL phase shift. The 561 is designed for this to be incorporated between the signal input and the input to the phase comparator input, pin 12 or pin 13.

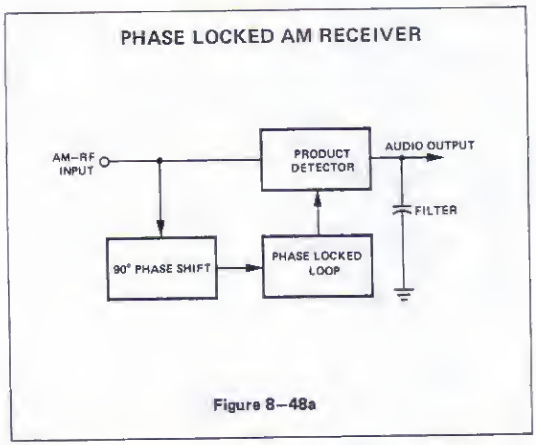


Figure 8–48a

Connection as an AM detector/receiver is given in Figure 8–48b. The bypass and coupling capacitors should be selected for low impedance at the operating frequency. C_o is selected to make the VCO oscillate at the frequency to be received and C_x is selected, in conjunction with the output resistance (8000Ω) and the load resistance, to roll off the audio output for the desired bandwidth. The phase shift network may be determined from the following equations:

$$C_y = \frac{1.3 \times 10^{-4}}{f_c} \text{ pF}$$

where f_c is the carrier frequency of the signal to be received and R_y = 3000Ω. A receiver for standard AM reception is easily constructed using the circuit of Figure 8-48b. Its operating range will be from 550kHz to 1.6MHz. All bypass and coupling capacitors are 0.1mfd. C_y is selected using a frequency which is the geometric mean of the limits of the frequencies which are to be received.

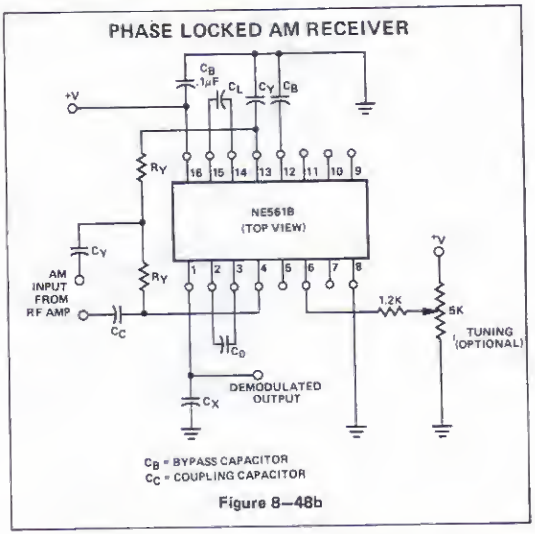


Figure 8–48b

$$f_c = \sqrt{f_{hi} f_{lo}} = \quad 1.6 \times 0.55 = .94\text{MHz then:}$$

$$C_y = \frac{1.3 \times 10^{-4}}{.94 \times 10^{-6}} = 135\text{pF}$$

The low pass filter for the loop, C_L, is not critical for no information is being derived directly from the loop error signal and one need only be assured of stable loop operation. A .01mfd capacitor was found to be adequate.

Tuning may be accomplished in several ways. The simplest method uses a variable capacitor as C_o. It should be trimmed so that when set for minimum capacitance, the VCO frequency is approximately 1.6MHz. The capacitance used may be obtained from the following formula: $C_o \approx \frac{300\text{pF}}{f_o}$ where f_o is in MHz.

Application of this formula shows that the minimum capacitance should be about 180pF and the maximum capacitance should be 550pF. A second tuning method utilizes the fine tuning input, pin 6. When current is inserted or removed from this pin, the VCO frequency will change, thereby tuning the receiver. Select C_o, when the current at pin 6 is zero, to make the VCO operate at the mean frequency used in the phase shift network calculation (940kHz). The complete standard AM broadcast band may now be tuned with one potentiometer. The resistor in series with the arm of the potentiometer is selected to give the desired tuning range and will be about 1200Ω when an 18V power supply is used.

For operation, this receiver requires an antenna and a good grounding system. Operation may be improved by including a broadband untuned RF amplifier, but care should be used to ensure that the phase locked loop is not overdriven, e.g. input signals should be kept less than 0.5V rms.

IF STAGE WITH AGC AND AM/FM DETECTION (561B)

The circuit shown in Figure 8–49 is basically an IF strip at 10.7MHz employing a buffer amplifier, two stages of gain, two ganged stages of AGC and an AGC summing amplifier. A single 561B PLL serves as both the AM and FM detector. Input sensitivity to insure lockup for either AM or FM demodulation is approximately 10μV. The input level to the 561B is held level at 305mV p-p during input amplitude excursion from 10μV to 120mV p-p. Potentiometer R_{AGC} is adjusted at no input for a quiescent dc voltage (pin 6 of amplifier 5741) of −90mV. This presets the 5596 multipliers at a maximum gain condition. The gain is slowly reduced as the RF input level rises and full AGC action begins.

The bandwidth of linear demodulation of AM is 1Hz to 4.5kHz and of FM is 1Hz to 36kHz.

IF gain adjustment can be provided with the installation of a potentiometer between pins 4 and 9 of either (or both) of the 5733, a zero ohm setting insuring maximum gain.

The addition of a conventional converter front-end and audio driver stages completes the circuitry for a receiver.

IF GAIN STAGE WITH AGC AND AM/FM DETECTION

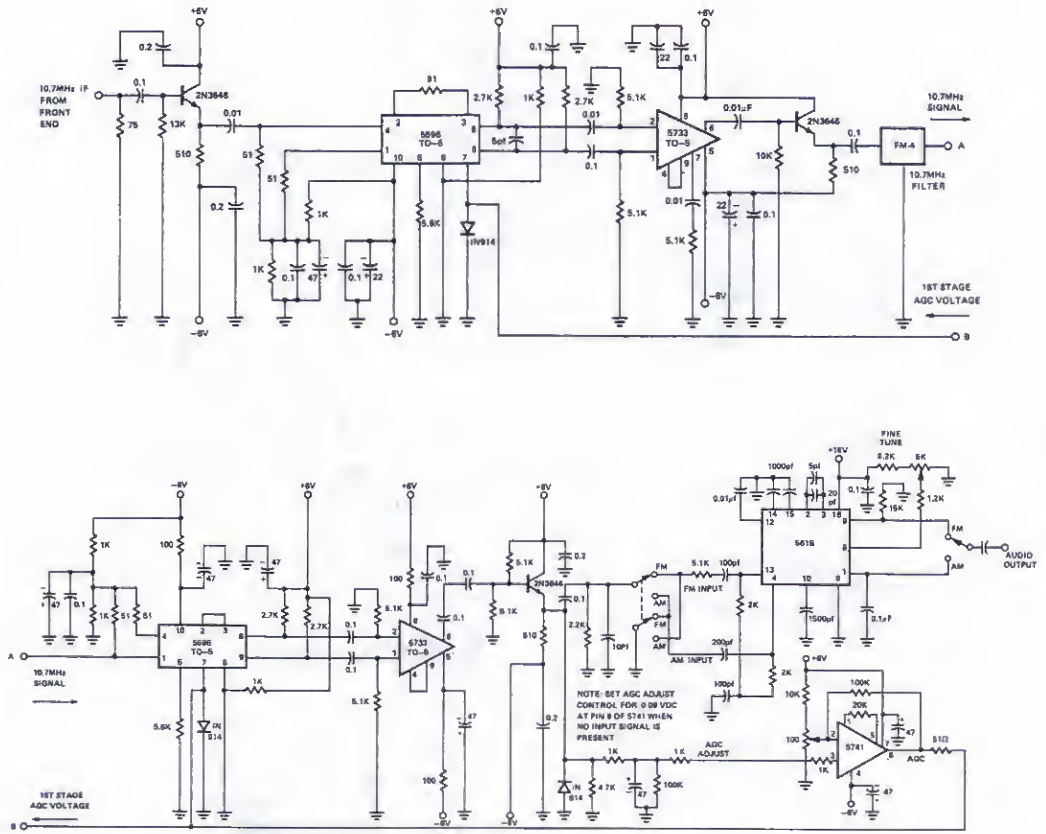


Figure 8–49

TRANSLATION LOOP FOR PRECISE FM (561B, 562B)

A translation loop mixes the output of two oscillators and produces a signal whose frequency is equal to the sum or difference of the two. In the most useful application of this circuit, one oscillator is a precise crystal-controlled oscillator and the second is a low frequency voltage-controlled oscillator so that the loop output is a FM signal whose center frequency is slightly offset from the crystal oscillator frequency. Since the offset oscillator supplies only a small percentage of the final output frequency, it need not be as precise as the crystal oscillator.

Such a loop is shown in Figure 8–50a. The VCO is driven until the filtered low frequency component of the PD2 output is equal to the offset frequency f_m. When this occurs, lockup is achieved and the VCO output is either $f_R + f_m$ or $f_R - f_m$. By adjusting the VCO free-running slightly above f_m, the latter case can be eliminated. If f_m is frequency modulated, then the output will also be frequency modulated since it has the same absolute deviation.

TRANSLATION LOOP FOR PRECISION TV INTERMEDIATE–FREQUENCY FM GENERATOR

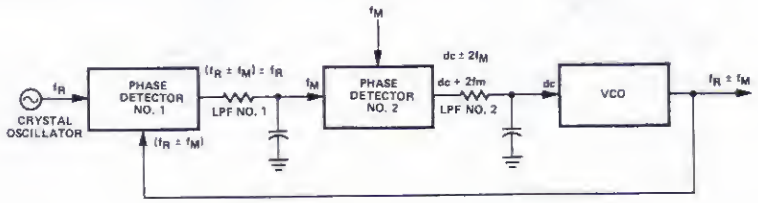


Figure 8–50a

Figure 8–50b shows a translation loop made from a 561B and 562B. It is designed to produce a 4.5MHz signal with a deviation of ±25kHz. The 561B serves as the VCO and PD1; the 562B serves as the crystal oscillator and PD2. A 4.400MHz crystal controls the reference frequency f_R. The offset frequency f_m is 100kHz frequency modulated ±25kHz at a modulation frequency of 400Hz. The accuracy of the output frequency is that of the reference oscillator plus that of the offset oscillator; since f_m is a small percentage (2%) of f_R, its stability can be considerably less than that of the crystal oscillator. In this case, f_m can be provided by a 566 VCO modulated, if desired, by a second 566. (The triangle wave 566 output results in a constant df/dt.)

TRANSLATION LOOP FOR PRECISION TV INTERMEDIATE – FREQUENCY FM GENERATOR

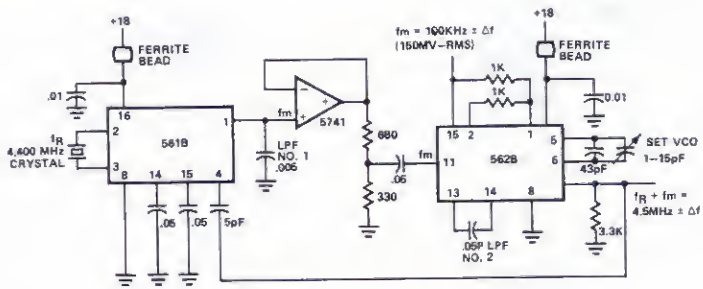


Figure 8–50b

Special layout precautions are required to be sure that no high frequency coupling occurs via grounds or power supply lines. The circuit is adjusted by trimming the 562 VCO trimmer capacitor until the beat note present at test point 1 has the same frequency as f_m throughout the deviation range (f_m can be deviated by hand or very slowly, say, at a 1Hz rate, to observe that the beat note does not break up during sweep. If the beat note is lost at either extreme, adjust the VCO trimmer. If the full deviation cannot be obtained, decrease the 562 low pass filter capacitor slightly. Connect a counter to the output to be sure the loop is locked to $f_R + f_m$ and not $f_R - f_m$ (unless the latter is desired).

Naturally, the component values given may be altered for other applications. Note that as f_m is made a smaller and smaller percentage of the total output frequency, it becomes difficult to prevent locking in the $f_R - f_m$ mode since the 562 lock range will likely include both $f_R - f_m$ and $f_R + f_m$. However, if f_m is made too large a portion of the output frequency, then overall stability suffers unless f_m is also quite precise.

PHASE LOCKED FSK DEMODULATORS (560B, 565)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

The 560B phase locked loop can be used as a receiving converter to demodulate FSK audio tones and to provide a shifting dc voltage to initiate mark or space code elements. The PLL can replace the bulky audio filters and undependable relay circuits previously used for this application. Connection of the 560B PLL as a FSK demodulator is illustrated in Figure 8–51.

FSK DEMODULATOR USING 560B

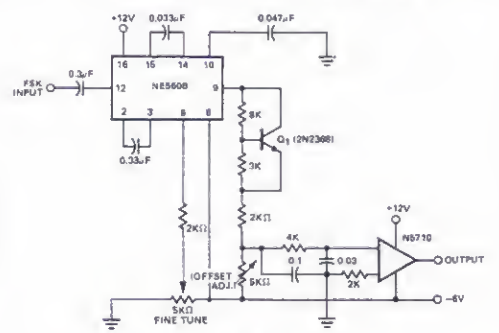


Figure 8–51

The system functions by locking-on and tracking the output frequency of the receiver. The demodulator frequency shift appears at pin 9 as a direct-current voltage of about 60mV amplitude and must be amplified and signal-conditioned to interface with the printer. The input voltage at pin 12 should be from 30mV to 2V peak-to-peak, square or sine wave. Pin 10, the de-emphasis terminal, is used for bandshaping. The capacitor connected between this terminal and ground bypasses unwanted high frequency noise to ground. Pin 9 is the output (approximately 60mV dc) which is amplified, conditioned and fed to a voltage comparator amplifier (N5710) to provide the proper voltages for interfacing with the printer. This specific circuit was designed to match the Bell 103C and 103D Data Phones. When modifying this circuit to accommodate other systems, maintain the resistance to ground from pin 9 at approximately 15Ω. Pins 3 and 2 are the connections for the external capacitor that determine the free-running frequency of the VCO. The 0.33μF value indicated provides a VCO frequency, f_o, of approximately 1060Hz. The value of the timing capacitor can be calculated by use of the following equation: $C_o = \frac{300pF}{f_o}$

where f_o is in Hertz.

The output has a swing of 2V peak-to-peak, over a 0 to 600 baud input FSK rate, with less than 10% jitter at the comparator output. The circuit is operative over a temperature range of 0° to 75°C with a total drift of approximately 100mV over the temperature range.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 8–52. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

FSK DECODER USING THE 565

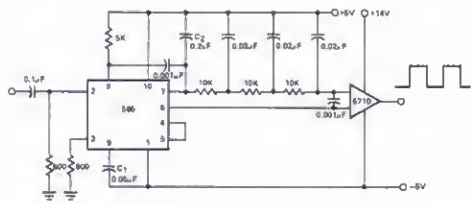


Figure 8–52

The loop filter capacitor C_2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency component. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300

baud or bits per second, or 150Hz) and twice the input frequency (about 2200Hz). The free-running frequency should be adjusted (with R_1) so that the dc voltage level at the output is the same as that at pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6.

The input connection is typical for cases where a dc voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance.)

FSK DECODER WITH EXPANDED 565 OUTPUT VOLTAGE RANGE

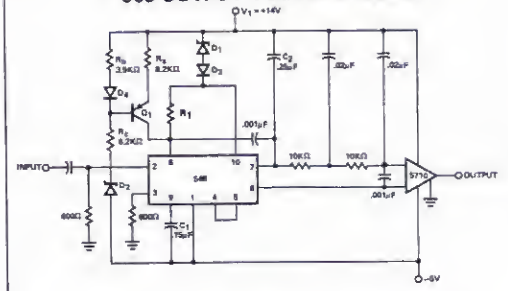


Figure 8–53

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 8–53. Here, a constant current is injected into pin 8 by means of transistor Q_1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for VCO) controls only the current through R_1, while the current through Q_1 remains constant. Thus, if most of the capacitor charging current is due to Q_1, the current variation due to R_1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25mfd loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs.

The output is then filtered with a two-stage RC ladder filter with a band edge chosen to be approximately 800Hz (approximately half-way between the maximum keying rate of 150Hz and twice the carrier frequency). The number of stages on the filter can be more or less depending on the degree of uncertainty allowable in the comparator output pulse. Two small capacitors (typically 0.001mfd) are connected between pins 8 and 7 of the 565 and across the input of the comparator to avoid possible oscillation problems.

For best operation, the free-running VCO frequency should be adjusted so that the output voltage (corresponding to the input frequencies of 1070Hz and 1270Hz swings equally to both sides of the reference voltage at pin 6. This can be easily done by adjusting the center frequency of the VCO so that the output signal of the 5710 comparator has a 50% duty cycle. It is usually necessary to decouple pin 6 with a large capacitor connected to the positive supply in order to obtain a stable reference voltage for the 5710 comparator.

Figure 8–54 shows the output of the 5710 comparator and the output of the 565 phase locked loop after the filter at rates of 100, 200 and 300 baud, respectively.

100 BAUD FSK DECODING

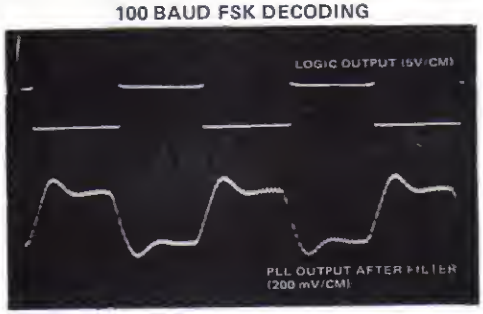


Figure 8–54a

200 BAUD FSK DECODING

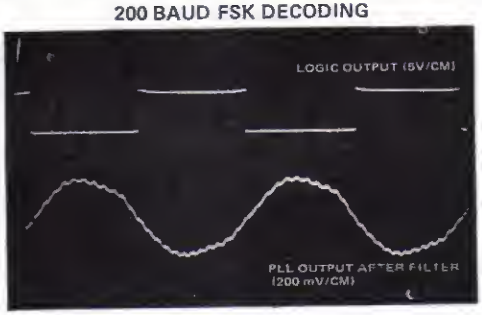


Figure 8–54b

300 BAUD FSK DECODING

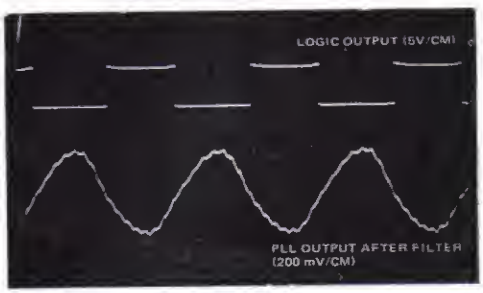


Figure 8–54c

ANALOG LIGHT COUPLED ISOLATORS (565, 567)

The analog isolator shown in Figure 8–55a is basically a FM transmission system with light as the transmission medium. Because of the high degree of electrical isolation achieved, low-level signals may be transmitted without interference by great potential difference between the sending and receiving circuits. The transmitter is a 565 used as a VCO with the input applied to the VCO terminal 7. Since the light emitting diode is driven from the 565 VCO output, the LED flashes at a rate proportional to the input voltage. The receiver is a photo transistor which drives an amplifier having sufficient gain to apply a 200mV peak-to-peak signal to the input of the receiving 565, which then acts as a FM detector with the output appearing at pin 7. Since the output has a twice carrier frequency ripple, it is best to keep the carrier frequency as high as possible (say, 100 times the highest modulation frequency). Because of the excellent temperature stability of the 565, drift is minimal even when dc levels are being transmitted. If operation to dc is not required, the output of the receiver can be capacitively coupled to the next stage. Also, a 566 can be used as the transmitter.

LIGHT-COUPLED ANALOG ISOLATORS

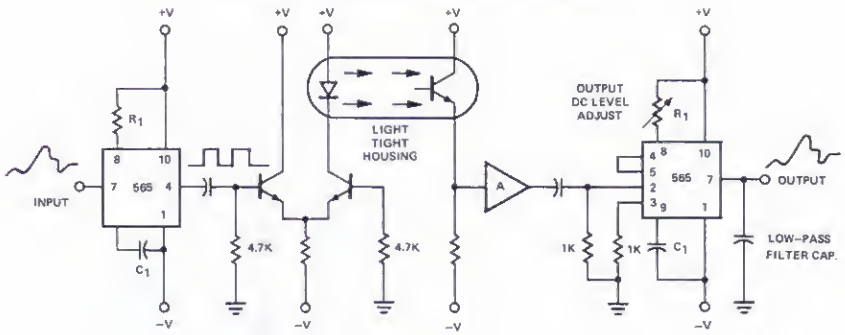


Figure 8–55a

Figure 8–55b shows that the 567 may be used in the same manner when operation from 5V supplies is required. Here, the output stage of the 567 is used to drive the LED directly. When the free-running frequency of the receiving 567 is the same as that of the transmitting 567, the non-linearity of the two controlled oscillator transfer functions cancel so that highly linear information transfer results.

LIGHT-COUPLED ANALOG ISOLATORS

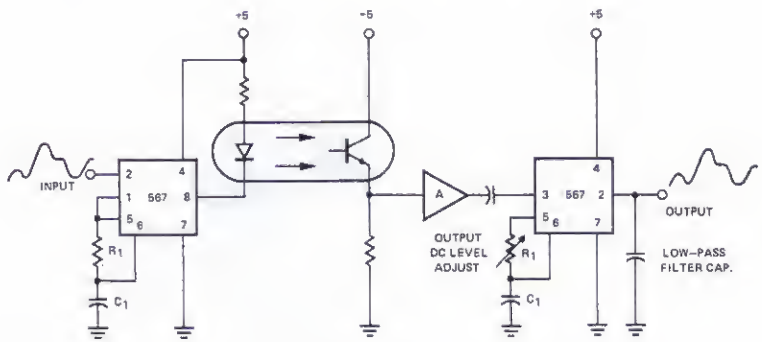
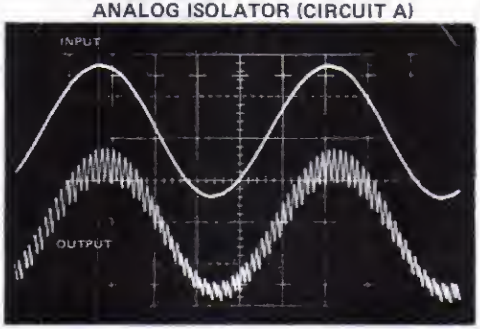


Figure 8–55b

Figure 8–56 is an oscillogram of the input and output of the Figure 8–55a circuit. The output can easily be filtered to remove the sum frequency component.

WAVEFORMS OF LIGHT-COUPLED ANALOG ISOLATOR (CIRCUIT A)



PHASE MODULATORS

If a phase locked loop is locked onto a signal at the center frequency, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase detector so that the VCO voltage is constant and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase detector output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 8–57a. The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 8–57b shows an implementation of this circuit using the 567.

PHASE MODULATION USING THE PLL

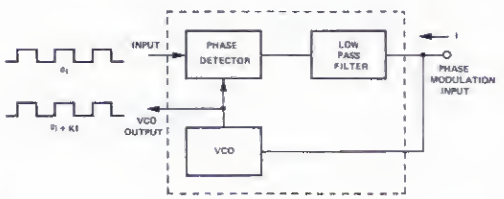


Figure 8–57a

PHASE MODULATION USING THE PLL

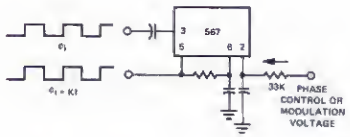


Figure 8–57b

DUAL TONE DECODERS (567)

Two integrated tone decoders can be connected (as shown in Figure 8–58a) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R_1'C_1'$ are chosen, respectively, for tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C_3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 8–58b shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_2 and CR_1 until activated by tone 1. A further variation is given in Figure 8–58c. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn-on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

HIGH SPEED, NARROW BAND TONE DECODER (567)

The circuit of Figure 8–58a may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_o$ and $1300/f_o$ mfd where f_o is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

DETECTION OF TWO SIMULTANEOUS OR SEQUENTIAL TONES

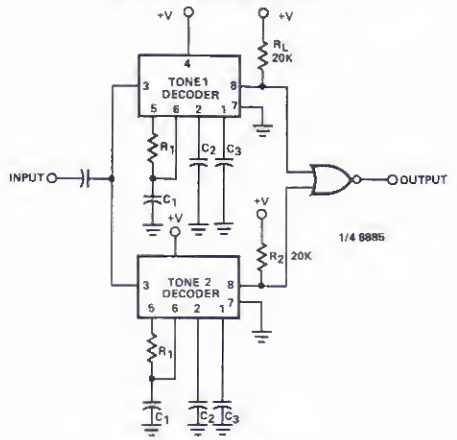


Figure 8–58a

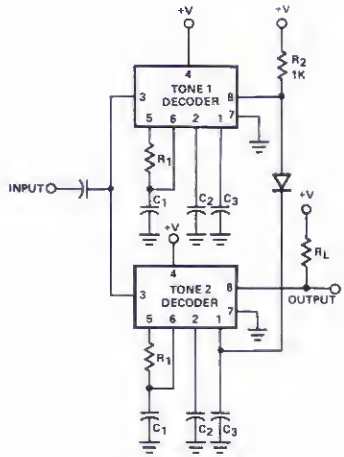


Figure 8–58b

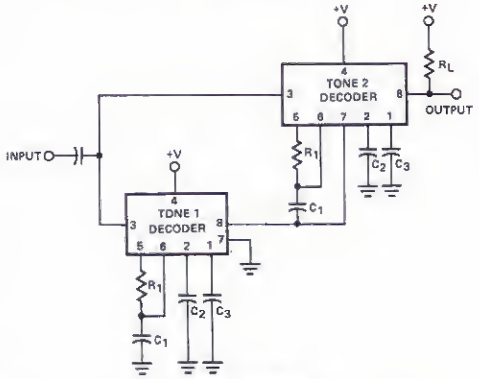


Figure 8–58c

TOUCH-TONE® DECODER (567)

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 8–59. Seven 567 tone decoders, their

LOW-COST TOUCH TONE® DECODER

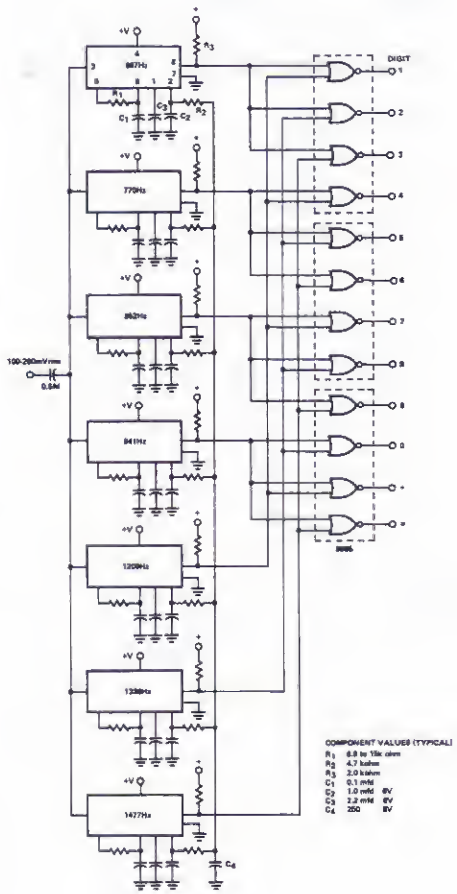


Figure 8–59

inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mV rms. Capacitor C_4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltages (50 to 100mV rms), the bandwidth can be controlled in the normal manner by selecting C_2, thereby eliminating the seven R_2 resistors and C_4. In this case, C_2 would be 4.7mfd for the three lower frequencies and 2.2mfd for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under Alternate Method of Bandwidth Reduction, an external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R_2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two 567s which are being activated. Capacitor C_4 decouples the ac currents at the common point.

FREQUENCY METER WITH LOW-COST LAMP READOUT

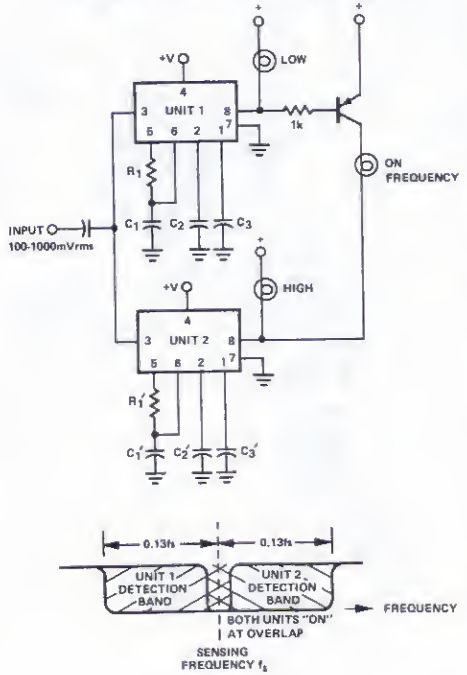


Figure 8–60

LOW COST FREQUENCY INDICATOR (567)

Figure 8–60 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

CRYSTAL-STABILIZED PHASE LOCKED LOOP (560B)

Figure 8–61a shows the 560B connected as a tracking filter for signals near 10MHz. The crystal keeps the free-running frequency at the desired value. Figure 8–61b gives the lock and capture range as a function of input amplitude. An emitter follower has been added to the normal VCO output to prevent pulling the loop off frequency.

CIRCUIT DIAGRAM

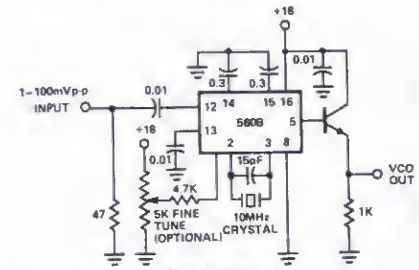


Figure 8–61a

LOCK RANGE VS INPUT AMPLITUDE

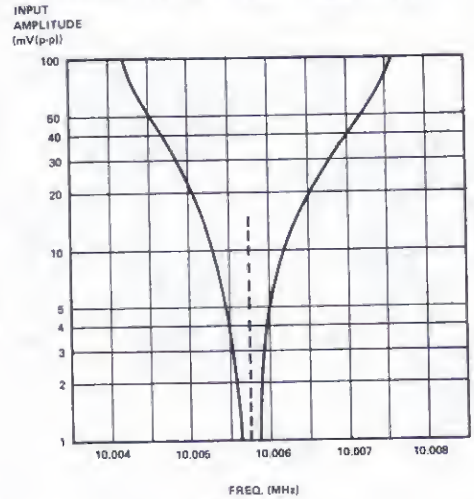


Figure 8–61b

RAMP GENERATORS (566)

Figure 8–62 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the pin 3 output rapidly discharges C_1 at the end of the charging period so that charging can resume instantaneously. The pnp transistor likewise rapidly charges the timing capacitor C_1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period τ is $1/2f_o$ where f_o is the 566 free-running frequency in normal operation. Therefore,

$$\tau = \frac{1}{2f_o} = \frac{R_T C_1 V^+}{5(V^+ - V_C)}$$

where V_C is the bias voltage τ pin 5 and R_T is the total resistance between pin 6 and V^+. Note that a short pulse is available at pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

NEGATIVE RAMP GENERATOR

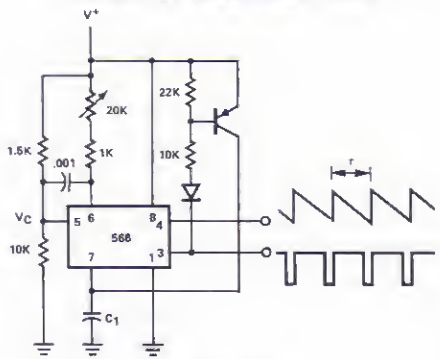


Figure 8–62a

POSITIVE RAMP GENERATOR

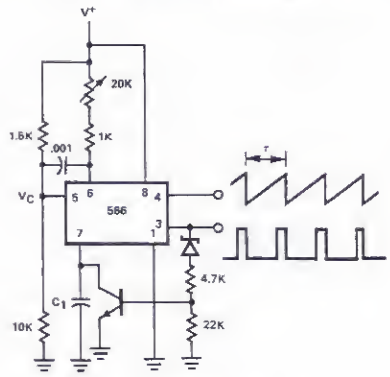


Figure 8–62b

SAWTOOTH AND PULSE GENERATOR (566)

Figure 8–63 shows how pin 3 output can be used to provide different charge and discharge currents for C_1 so that a sawtooth output is available at pin 4 and a pulse at pin 3. The pnp transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

$$\tau = \frac{R_T C_1 V^+}{5(V^+ - V_C)}$$

where R_T is the combined resistance between pin 6 and V^+ for the interval considered.

POSITIVE SAWTOOTH AND PULSE GENERATOR

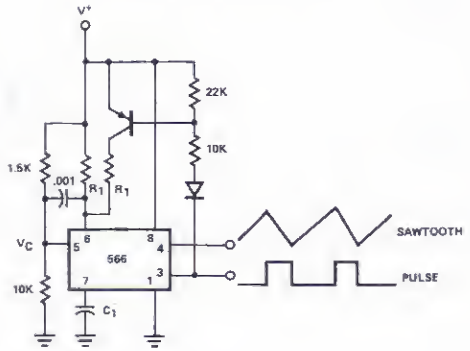


Figure 8–63a

NEGATIVE SAWTOOTH AND PULSE GENERATOR

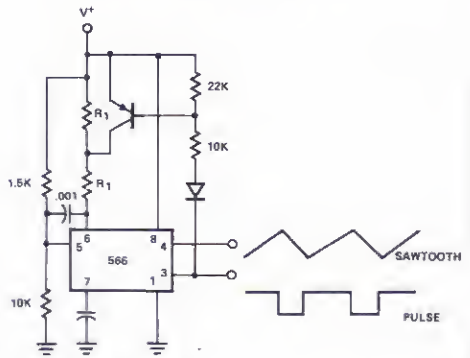


Figure 8–63b

TRIANGLE-TO-SINE CONVERTERS (566)

Conversion of triangular wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

The first scheme (Figure 8–64a) uses the non-linear $I_{DS} - V_{DS}$ transfer characteristic of a p-channel junction FET to shape the triangle waveform. The second scheme (Figure 8–64b) uses the non-linear emitter base junction characteristic of the 511B for shaping.

In both cases, the amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

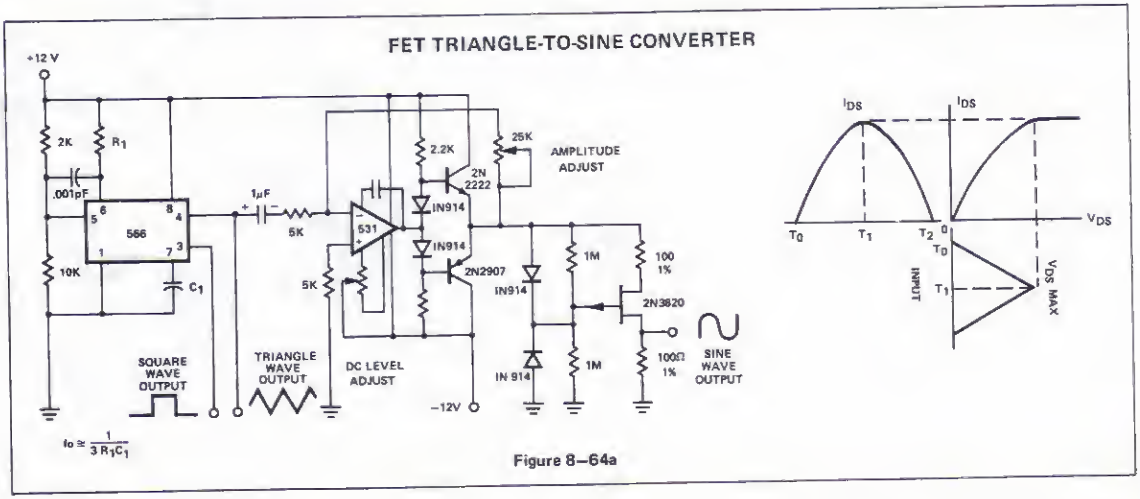


Figure 8–64a

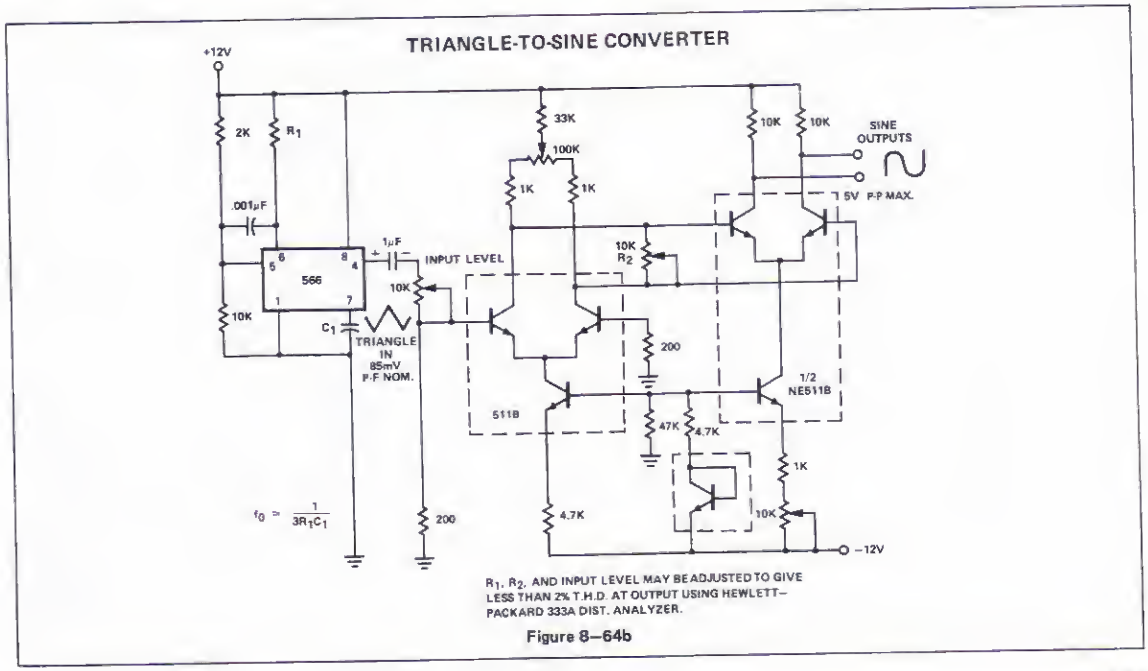


Figure 8–64b

SINGLE TONE BURST GENERATOR (566)

Figure 8–65 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is as a communications network alert signal. Cessation of the tone is accomplished by the SCR, which shunts the timing capacitor C_1 charge current when activated. The SCR is gated on when C_2 charges up to the gate voltage, which occurs in 0.5 seconds. Since only 70μA are available for triggering, the SCR must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R_2 (and increasing C_2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R_2, $R_2' = 82K$.

If the SCR is replaced by a npn transistor, the tone can be switched on and off at will at the transistor base terminal.

SINGLE BURST TONE GENERATOR

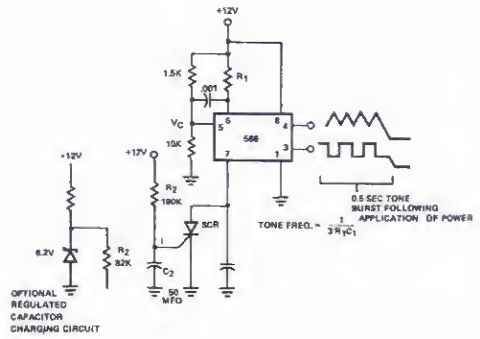


Figure 8–65

LOW FREQUENCY FM GENERATORS (566)

Figures 8–66 and 8–67 show FM generators for low frequency (less than 0.5MHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C_1 selects the modulation frequency adjustment range and C_1' selects the center frequency. Capacitor C_2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

FREQUENCY MODULATED GENERATOR FOR SMALL DEVIATIONS (TO ±20%)

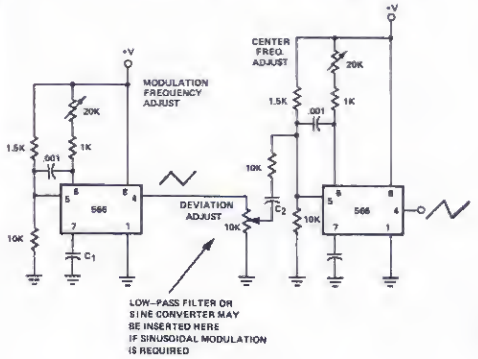


Figure 8–66

FREQUENCY MODULATED GENERATOR FOR LARGE DEVIATIONS (TO ±100%)

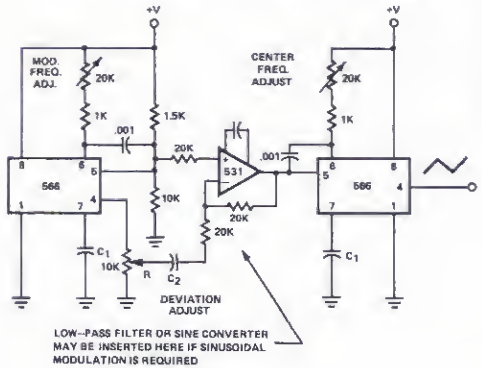


Figure 8–67

RADIO FREQUENCY FM GENERATORS (566, 560B)

Figure 8–68 shows how a 560B may be used as a FM generator with modulation supplied by a 566 function generator. Capacitor C_1 is chosen to give the desired modulation range, C_2 is large enough for undistorted coupling and C_3 with its trimmer specifies the center frequency. The VCO output may be taken differentially or single ended.

A 561B or 562B with appropriate pin numbering changes may also be used in this application. If a sweep generator is desired, the 566 may be connected as a ramp generator (described elsewhere in this chapter).

RF-FM GENERATOR

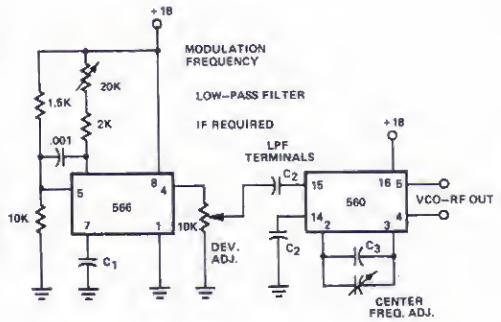


Figure 8–68

PRECISION POWER INVERTER (566, 540)

Figure 8–69 shows a precision 12 VDC to 115 VAC 100W inverter. Its triangular output is derived from the 566 function generator, providing a high degree of frequency stability (±.02%/°C). The 540 power driver is used to drive the power output stage. Because of third harmonic attenuation in the transformer, the output is very close to a pure 60Hz sine wave.

DESIGN IDEAS FOR USING PHASE LOCKED LOOPS

The following design ideas were drawn mainly from the Signetics-EDN Phase Locked Loop Contest. These circuits should be viewed as design suggestions only since Signetics has not verified their operating characteristics. In all cases, however, the principle of operation appears to be sound.

Quotation marks indicate quotes taken directly from the contest entry.

AIRCRAFT VHF OMNIDIRECTIONAL RANGE (VOR) RECEIVER

Herbert F. Kraemer of Minneapolis, Minnesota, submitted the winning contest entry which uses one phase locked loop (562) as an AM detector, a second loop (565) as an FM detector and a third loop (565) as a self-biased phase detector.

"The circuit is a new type of VOR (VHF omnidirectional range) receiver used in air navigation to determine an airplane's angular bearing with respect to a VOR transmitter located on the ground. The principles of the circuit allow any desired increase in accuracy, as compared to current units, with potential cost savings.

PRECISION 100 WATT POWER INVERTER

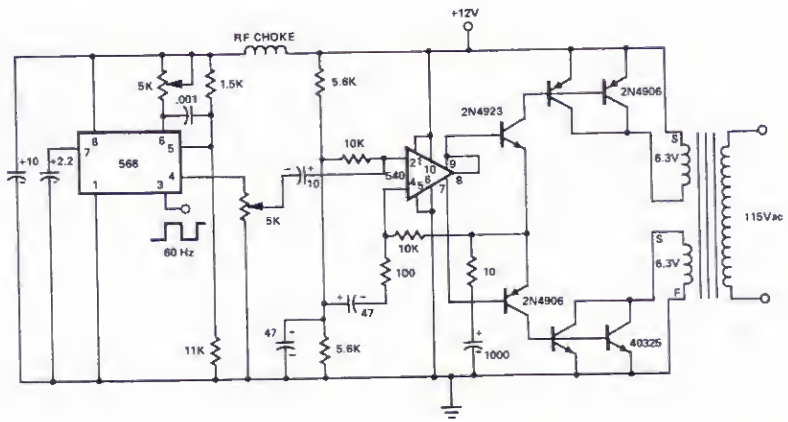


Figure 8–69

A VOR station transmits in the VHF band (108–117.9MHz). Two signals are transmitted on the same carrier, i.e.,

1) A 30Hz reference signal which frequency modulates an audio frequency subcarrier of 9960Hz. This subcarrier then amplitude modulates the VHF carrier.
2) A 30Hz directional signal which amplitude modulates the VHF carrier.

The latter signal varies in phase with respect to the reference, depending on the bearing of the VOR station and the receiver. Both signals are in phase when the receiver is north of the transmitter and 180 degrees out of phase when the receiver is south.

Current VOR receivers are specified to be accurate within a 1–2 degree bearing, but many pilots accept 4 degree errors. The major design problem is to produce a receiver which will measure phase differences to an accuracy of about 1 degree, throughout the entire 360 degree range."

Although analog quarter-square multipliers can be built to an accuracy of 0.01%, the simpler analog phase detectors are only accurate to 3–4°. This circuit uses the NE562 PLL to frequency multiply the two 30Hz signals, producing 60 and 120Hz signals. A digital method combines these signals, thereby dividing the entire range of bearings into eight 45° sectors. One of eight lights on the display will light, showing the pilot his approximate bearing. An analog method is then used to further determine the phase difference and the bearing within the given 45° sector. Extending the principle further, sectors of 22½° could be used for improved accuracy.

This VOR receiver does not have the conventional to-from switch since it indicates directly throughout the entire 360° range. Confusion of 180° in bearing (going the wrong way) is impossible with this receiver.

System Description (References to Block Number – Figure 8–70)

Block 1. This is a standard VHF tuner.
Block 2. The NE561 is used for IF and AM detection.
Block 3. A low pass filter removes the 9960Hz subcarrier. It appears that a zero crossing detector is not needed to shape the input signal to the NE562.
Block 4. Frequency multiplier.
Block 5. High pass filter.
Block 6. FM detection of 30Hz signal.
Block 7. A calibration adjustment to compensate for any phase shifts throughout the circuit. A gain may be needed since the FM detector output is low.
Block 8. Another frequency multiplier.
Block 9. Standard ripple flip-flops for divide-by-two.
Block 10. A null principle is normally used in a VOR receiver so that the pilot can fly along a predetermined course, nulling the needle by turning his plane. To insure that the needle always reacts in the same direction for a given direction of error, even sectors are treated differently than odd sectors." The phase comparison is made with respect to C for *odd* sectors, and with respect to $\overline{C}$ for *even* sectors.
Block 11. "At the desired null, the two signals must be 90 degrees out of phase to obtain a zero output from the phase detector. Some gain may be needed to compensate for the losses in Block 10.
Block 12. The phase detector portion of the NE565 only is used. The VCO part is unused but may be valuable in certain types of special displays.

An alternate form of analog phase detector might be an AND gate followed by a standard duty cycle integrator, such as used on dwell meters.

Block 13. The digital signals from the flip-flops are decoded with AND gates to indicate the sector corresponding to the phase lag between the two 30Hz signals."

SPEECH PRIVACY CIRCUIT (SPEECH SCRAMBLER)

The second place entry was that of David M. Alexander of Austin, Texas. His application for the loop was a voice scrambler-unscrambler for private communications.

"This circuit utilizes the principles of frequency inversion and masking to render speech unintelligible to listeners not possessing a similar unit. A synchronization signal is generated as part of the scrambled signal which phase locks the decoding carrier oscillator to the coding oscillator and thus guarantees minimum distortion in the unscrambled speech. This synch signal also increases the security close to the inversion point where they are displaced only slightly from their original values.

In operation, a single circuit serves as both scrambler and unscrambler at one end of a two-way communications link. It is switched from the receive mode to the transmit mode by a multipole relay controlled by the push-to-talk switch on the system microphone or handset.

As can be seen by the diagram (Figure 8–71), the major components of the system are the synch oscillator PLL-1 (NE560B), the carrier oscillator-modulator PLL-2 (NE561B) and the mixer-gain stage OA-1 (5709).

VHF OMNIDIRECTIONAL RANGE (VOR) RECEIVER

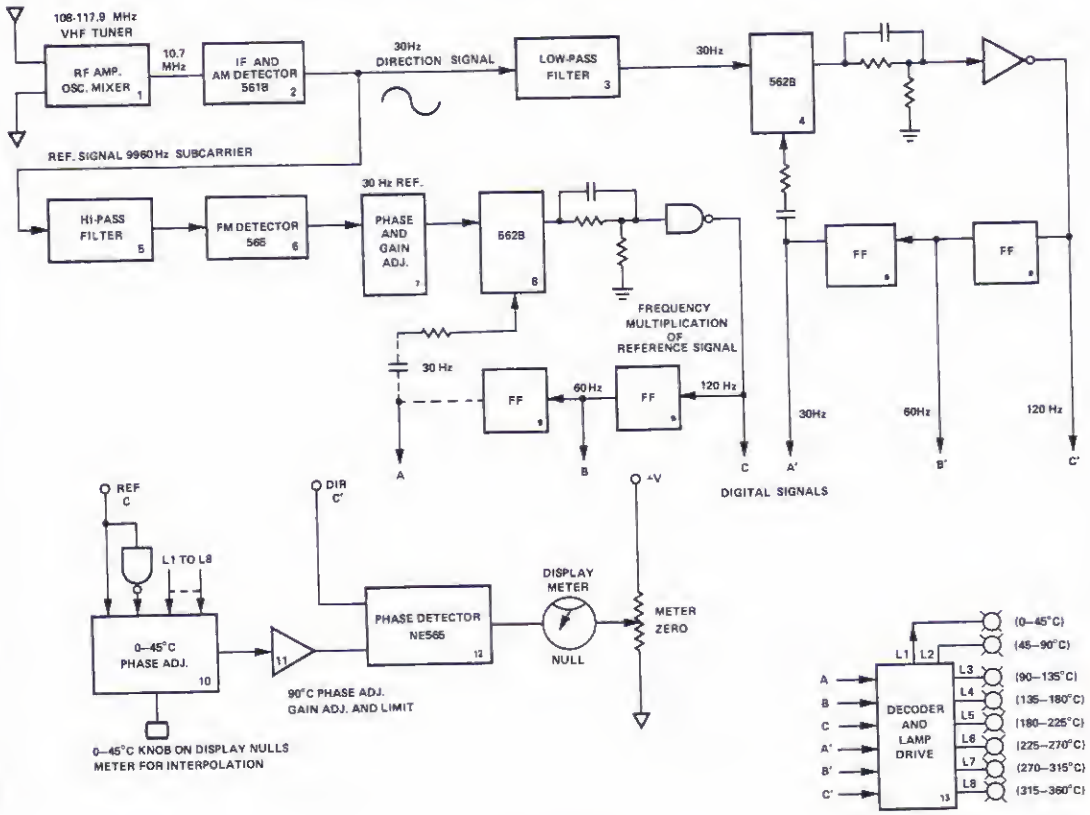


Figure 8–70

SIMPLIFIED DIAGRAM OF VOICE SCRAMBLER

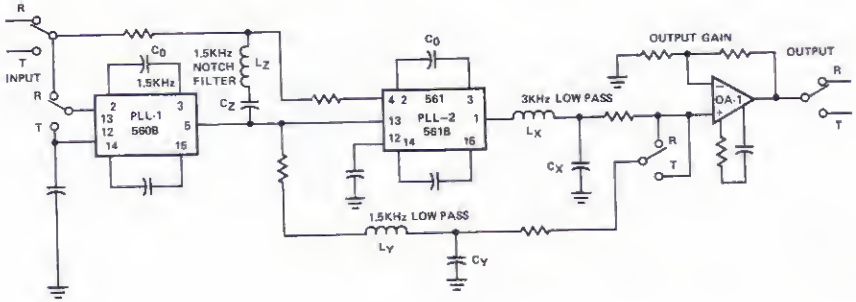


Figure 8–71

In the transmit mode, PLL-1 is adjusted to free-run at the inversion frequency (1.5kHz), or ½ the desired carrier frequency. PLL-2 is phase locked to this oscillator and operates on its second harmonic frequency (3kHz). The audio to be scrambled is applied to the input of the multiplier of PLL-2. This produces the sum and difference products of the input audio and the encoding carrier. The sum product is filtered out by the low pass filter (Lx-Cx), leaving only the difference product. This product consists of the original audio signal with the frequency components inverted about ½ the carrier frequency, or 1.5kHz. The square wave output of the oscillator of PLL-1 is low pass filtered by network Ly-Cy to produce a sine wave sync signal which is mixed with the inverted speech by OA-1 to produce the final scrambled signal.

In the receive mode, PLL-1 is phase locked to the 1.5kHz synch and masking signal and acts as a signal conditioner for this signal. PLL-2 doubles this frequency to produce the decoding carrier. The scrambled signal is notch-filtered by network Lz-Cz to remove the 1.5kHz sync and masking signal and the resultant inverted audio applied to the multiplier of PLL-2. Here it is re-inverted in a manner similar to that of the transmit mode. The resultant unscrambled audio is amplified in OA-1 for output to further system audio stages."

[Note: It is suggested that the 1.5kHz "sync and masking" signal be changed to 1.0kHz, since PLL-2 (free-running at 3kHz) will lock to the third harmonic of the 1kHz square wave from PLL-1 more readily than to the small second harmonic of the 1.5kHz signal. It may then be desirable to disconnect the notch filter during transmission. Of course, the filters may be implemented using active filter techniques.]

PRECISION PROGRAMMABLE TIME DELAY GENERATOR

Sam Butt of Gaithersburg, Maryland, submitted the third place entry. This circuit provides both a pulse and a high frequency output at some time t_d after an input pulse is received. The interval t_d is programmable in 10 steps by means of a digital output switch.

Figure 8–72 shows the circuit in simplified form. It works as follows:

The 562 VCO is set so that its center frequency is at a point slightly above (say 10.5MHz) the window of the 10MHz band pass filter (BPF). Thus, no rf appears at the output. When a pulse is received at the input, the flip-flop is set so as to actuate one input A of the N8880A NAND gate. The other side of the NAND gate B receives a signal which occurs at the rate of f_r/M where M is set by the binary-output switch. The output of the NAND gate begins to drive the N8291A binary ripple counter which is connected to the divide-by-N circuit in the loop feedback path. When 10 counts have been registered, the divide-by-N counter is putting out $f_o/10$ or (in the assumed case) 1.05MHz. Since the phase comparator now sees two frequencies very close together, the loop locks up and $f_o = 10\ f_r$. Since f_r is 1MHz, the VCO operates at 10MHz rf which the band pass filter passes to the output. This rf is detected and used to reset the input flip-flop and the counter in preparation for the next input pulse. The duration of the rf output is determined mainly by the detector time constant. The duration of the output pulse, which begins when the rf detector actuates the one-shot, is determined by the one-shot time constant.

The delay time is

$$t_d = \frac{NM}{f_r}$$

where M is settable between 1 and 10 using the digital switch.

METAL DETECTOR USING PLL AS A FREQUENCY METER (565)

The metal detector shown in Figure 8–73 was submitted to the Signetics-EDN Phase Locked Loop Contest by Jim Blecksmith of Irvine, California. It incorporates a 565 as a frequency meter which indicates the frequency change in a Colpitts oscillator whose tank coil approaches a metal object. The loop output voltage at pin 7 is compared with the reference voltage at pin 6 and the difference amplified by meter amplifier Q_4, Q_5.

To increase the loop output (pin 7) to about 0.5V per percent of frequency deviation, a current source (Q_2, Q_3) is used to supply most of the capacitor (2.5mA) charge and discharge current at pin 8. The 20K resistor connected to pin 8 changes the charge and discharge current by $\frac{0.5V}{20K\Omega} =$ .025mA or about 1% per 0.5V. Since the voltage at pins 8 and 7 track, the loop output voltage is also 0.5V per percent deviation. (This technique of increasing loop output swing for small frequency deviations is discussed in the Expanding Loop Capability section of this chapter.)

Increasing oscillator frequency, as indicated by a rising meter indication, results when the search coil is brought near a non-ferrous metal object. Reduced oscillator frequency, as indicated by a dropping meter reading, results from the search coil being brought near a ferrous object.

PRECISION PROGRAMMABLE TIME DELAY GENERATOR

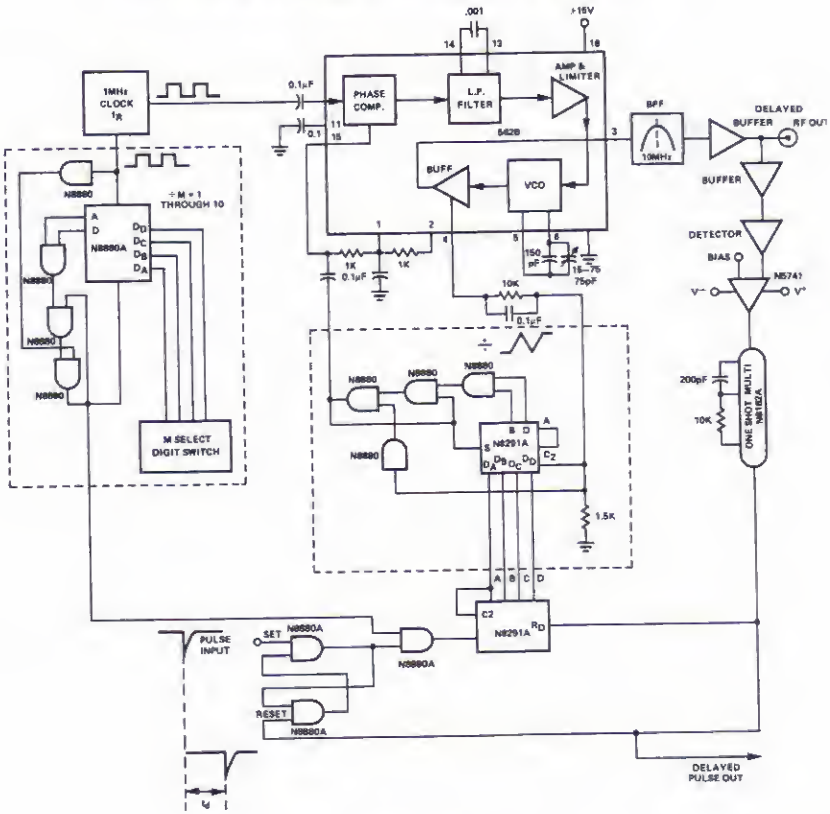


Figure 8–72

PHASE LOCKED LOOP METAL DETECTOR

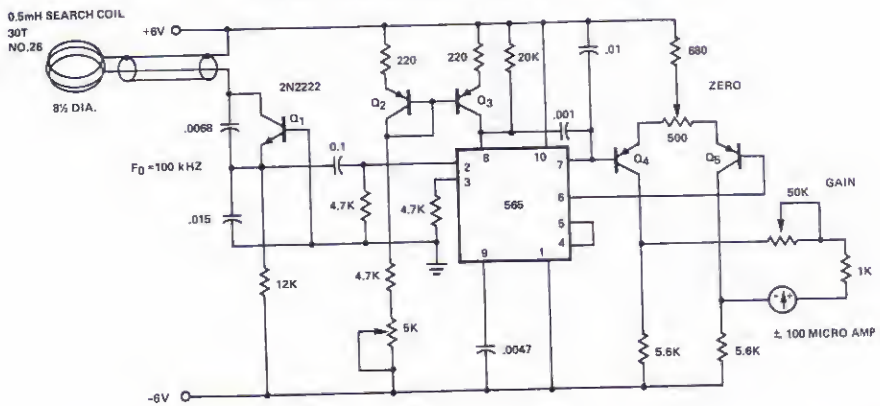


Figure 8–73

PROGRAMMED PHASE OR FREQUENCY SHIFT

Howard E. Clupper of Chadds Ford, Pennsylvania, submitted the following circuit in which "a digital phase shifter is inserted in the loop between the VCO and the phase comparator. The phase shift is programmed by sequentially selecting the ring counter outputs by means of the multiplexer and up-down counter.

"As shown in Figure 8–74, the eight ring counter outputs are separated by 45°, which is within the lock-in range of the loop. Output 1 is constrained to follow the phase shift introduced and may be used, for example, to drive a synchronous motor above or below its normal speed, while still maintaining reference with the input. This is accomplished by monitoring the contents of the up-down counter (which may be any length). As long as the counter does not overflow, the motor may be advanced or retarded in any manner and then returned to the original relationship with respect to the 60Hz reference input by running the U/D counter to the initial value.

For higher frequency outputs, a divide-by-N counter may be added in the normal manner and the output taken directly from the VCO at output 2. Operation in this mode would provide means to generate a precisely controlled FM signal of any arbitrary center frequency depending upon the frequency of the reference input and the value of N."

The 565 may be used in this circuit in place of the 562 for lower frequency applications (less than 500kHz).

PROGRAMMED PHASE OR FREQUENCY SHIFTER

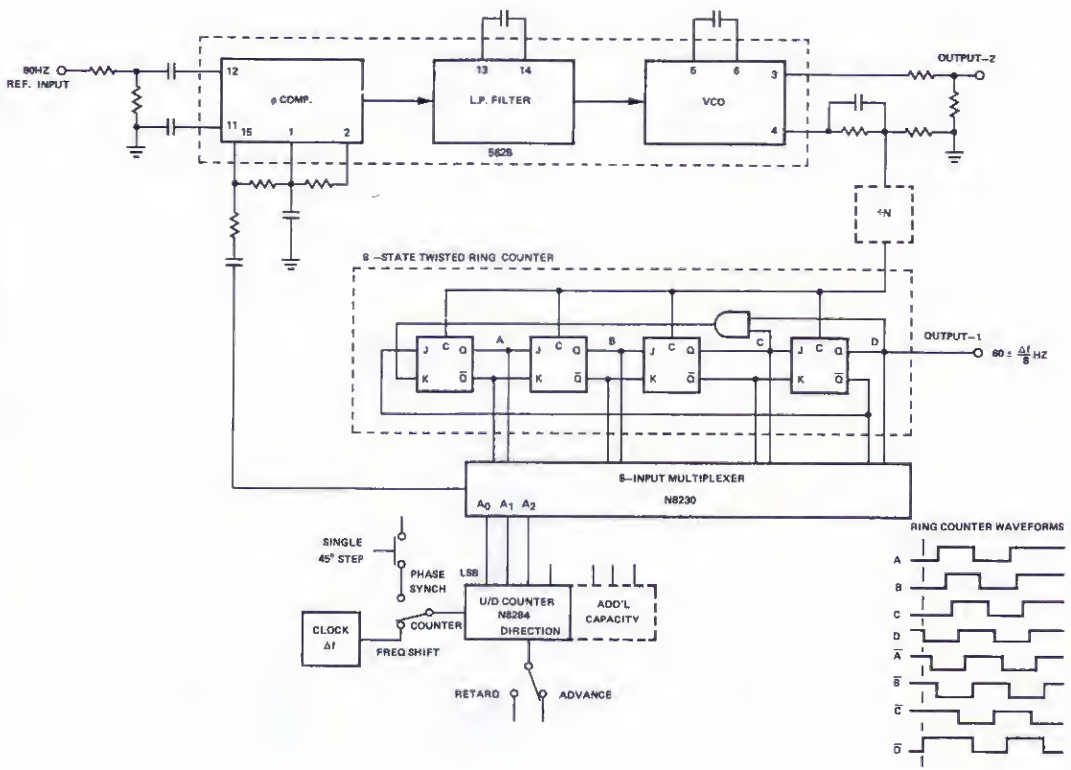


Figure 8–74

FSK DATA CONVERTER FOR CASSETTE RECORDER

A circuit scheme which allows an ordinary reel or cassette tape recorder to be used as a digital data recorder was submitted by Daniel Chin of Burlington, Massachusetts.

"The circuit design allows any single-track audio tape recorder with frequency response to 7kHz to be used as a digital recorder for many non-critical applications. This application provides a complete data recording system using two recorded frequencies on a single track. The two frequencies are obtained from two synchronized NE565s. Detection of the recorded frequencies requires a third NE565. A fourth circuit is used to generate and synchronize the system clock. The advantages obtained by using these techniques are elimination of the need for:

1. A timing channel to strobe off the data, or
2. A third frequency for null, while using the other two frequencies for 1 and 0.

This implementation, therefore, is one of the simplest ways to get a digital recording system on an audio recorder. It is shown in block diagram form in Figure 8–75.

The parameters chosen for the circuit design allow a digital recording bit rate of 800Hz or 100 8-bit characters per second. Though 100 characters per second is less than the 300-character-per-second speed of a high-speed paper tape reader, the low cost of this circuitry combined with the audio tape recorder should make this system very attractive from a cost performance viewpoint. This is especially true when compared with the normal Teletype speed of 10 characters per second.

BLOCK DIAGRAM OF
PLL CASSETTE RECORDER

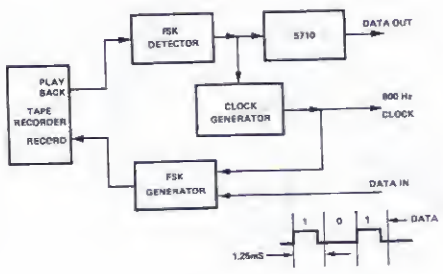


Figure 8–75

The circuits will also work with the readily available low cost cassette recorders now available, which make compact as well as low cost information storage. A FSK system of recording is used, which allows the voice recording and reproduction electronics of the recorder to be unmodified for use in recording digital information. The retained electronics may also be used to record voice message identification of the various sections of the tape.

The intended use of this circuit is to convert an audio recorder for minicomputer programs written for engineering design applications. Such an application requires good information storage and retrieval over a wide range of storage time. Redundancy may be incorporated by using a two-channel recorder (stereo) and a FSK detector per channel. The outputs of the two detectors could then be ORed digitally to recovered recorded 1s and, thus, give a safeguard against dropouts.

Circuit Description

Four NE565s are used in three circuits to achieve the design. These are:

The FSK detector (Figure 8–76a) is used to detect 6.4kHz for a 1 and 4.8kHz for a 0. The data output is taken from a 5711 connected to pins 7 and 6 of the NE565. The recording method used is RZ FSK, which means that a zero is recorded as 4.8kHz for the entire bit period and one is recorded as 6.4kHz for about 60 percent of the period and 4.8kHz for the remaining 40 percent of the period. This 60 percent bit duty cycle insures that the clock will synchronize with a negative transition during the time that a 1 should be detected.

CASSETTE RECORDER FSK DETECTOR,
CLOCK GENERATOR AND FSK GENERATOR

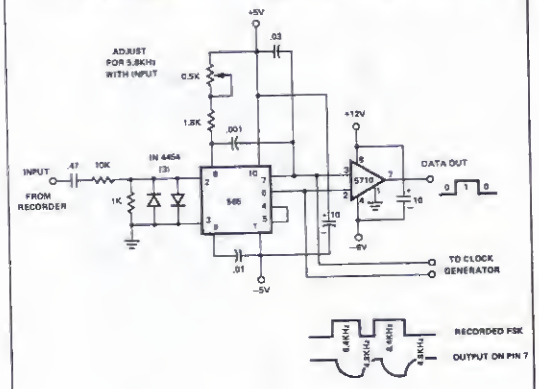


Figure 8–76a

The clock generator (Figure 8–76b) is used to derive the 800Hz with no input. When the data pulses are extracted from the recorded data, the clock is synchronized to the data. The design allows up to 7 zeros in succession without causing the clock to go out of synchronization. This condition is easily met if odd parity is used to record the 8-bit characters. (One of the 8 bits is a parity bit and, thus, one bit out of 8 is always a one.)

The FSK generator (Figure 8–76c) provides the FSK signal for recording on tape. It consists of 2 oscillators locked to the basic 800Hz system clock but oscillating at 6.4kHz and 4.8kHz. The incoming data to be recorded selects either oscillator as the frequency to be recorded. Harmonic suppression of the square wave output is taken care of automatically by the high frequency roll off characteristic of the tape recorder."

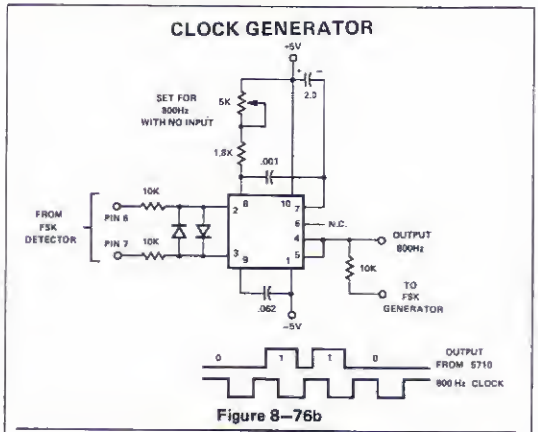


Figure 8–76b

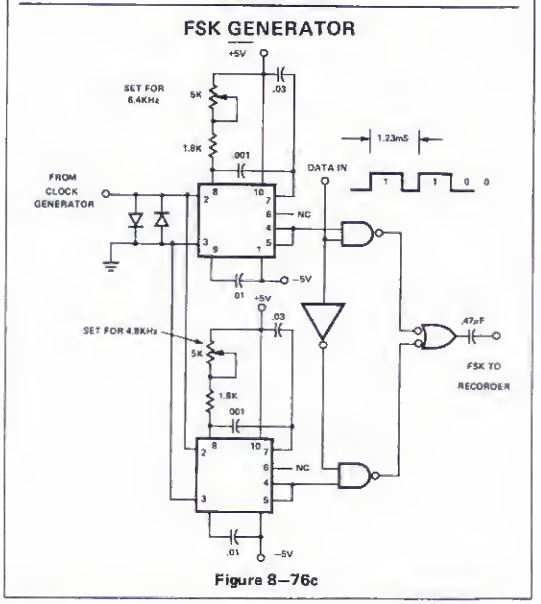


Figure 8–76c

SELF-RESETTING DIGITAL CLOCK

The following application, submitted by Don Lancaster of Goodyear, Arizona, makes use of the 561B as a 60kHz AM detector.

"The 561B Phase Lock Loop may be combined with TTL integrated circuits to form an always-accurate digital clock based upon the monitoring and direct display of the time code provided by NBS radio station WWVB operating at a 60kHz carrier frequency. Unlike the other time services, WWVB presents a time code directly in BCD digital form, coded as a 10 decibel AM reduction of the carrier. A clock based on this time code information would always be accurate as no counters would be involved and the digital display would always correct itself after a power failure, unlike regular electric clocks which must be manually reset.

Until recently, this type of clock circuitry would have been prohibitively expensive, but now the PLL makes the receiver portion of the clock extremely simple, while recent drastic price reductions in TTL MSI make the display and readout also a simple and relatively economical proposition.

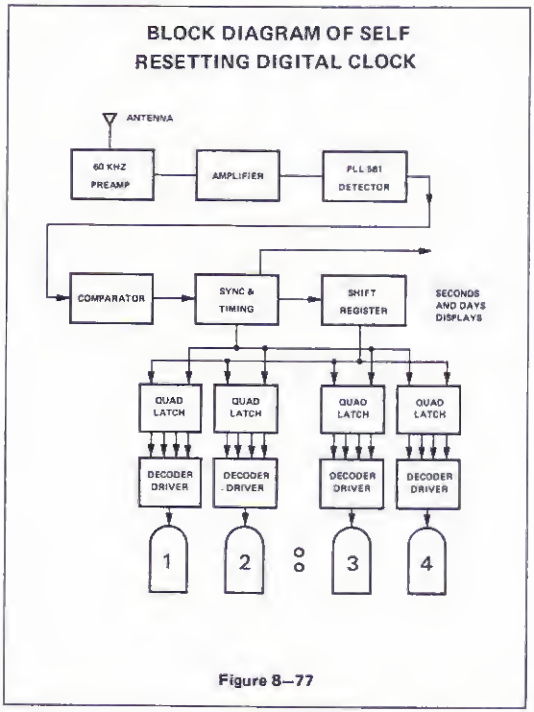


Figure 8–77

Figure 8–71 shows a block diagram of the system. A high Q antenna and a suitable low noise preamplifier are used for a front end, followed by an additional gain stage and the 561 set up as a synchronous AM detector. The output of the 561 consists directly of the demodulated time code.

The code is then translated with a comparator and routed to a two-monostable synchronizer that seeks the double once-each-minute sync pulse that identifies that the tens of hours code will follow (Figure 8–78). After synchronization, the code is "1"–"0" detected and routed to a five stage shift register. On every fifth count (consisting of a BCD word and a marker) one of four quad latches are strobed. The latches then store the appropriate minutes, tens of minutes, hours and tens of hours. Each quad latch then drives a BCD/Decimal Decoder/Driver, which in turn drives a NIXIE® or other suitable display tube.

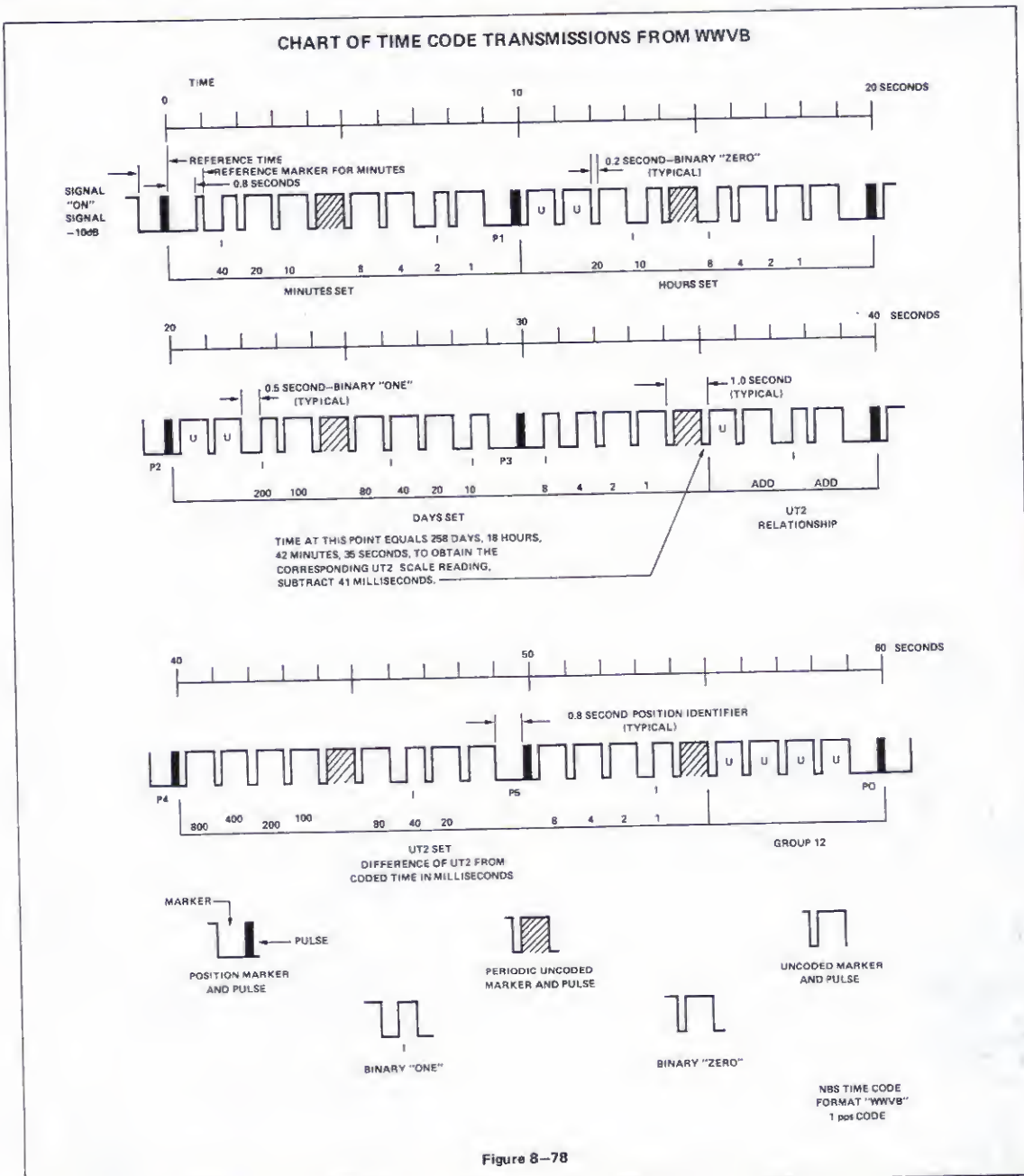


Figure 8–78

The display gives the time to the nearest minute and is updated every minute. Seconds are added simply by a blinker, or else a divide-by-60 counter and decoder driver may be used. This counter may be reset every minute by the sync pulse; thus, after a power failure, the clock would correct its seconds reading within a minute of the power being reapplied. If desired, the day of the year may be similarly displayed and if local time is preferred to GMT, a suitable BCD adder or subtractor may be placed between the shift register and the latches.

Figure 8–79 shows the PLL detector circuit. It was found that either a rooftop hula hoop or a ferrite rod and a local 10dB gain amplifier was sufficient to drive the PLL if a single transistor gain stage was added between the two. The amplified 60kHz signal is applied directly to the RF input and applied to the AM Multiplier input via a 90° phase shift network. The output of the multiplier is triply RC filtered to give a good rejection of 60Hz hum, while still allowing the 0.2 second minimum-width pulses to pass with good fidelity."

PLL PORTION OF SELF-RESETTING DIGITAL CLOCK

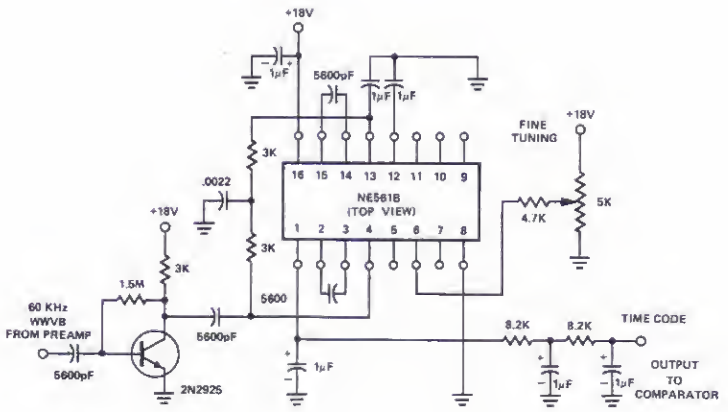


Figure 8–79

TAPE RECORDER FLUTTER METER

Using the 561 as a flutter meter for tape recorders was suggested by Ronald Blair of Houston, Texas. His circuit is given in Figure 8–80.

"The Signetics PLL 561B is used to detect the frequency variations of the playback 3kHz tone. The VCO frequency is set to a nominal 3kHz by C_o and fine tuning trimmer. The demodulated output is ac coupled to a high input impedance amplifier. An oscilloscope can be used to measure peak deviations and a true RMS voltmeter is used to make RMS flutter readings. Note: Waveform is complex and averaging or peak reading meters will not give true readings.

The output may be calibrated by feeding in a 3kHz tone from an oscillator and offsetting the frequency by 1% and measuring the output level shift. Good recorders have RMS flutter of less than 0.1%. The output can be filtered to study selected frequency bands.

Speed variations in the movement of tape across the heads in a 4 tape recorder cause the playback frequency to vary from the original signal being recorded. These speed variations are caused by mechanical problems associated with the tape drive and tape guidance mechanisms. The variation in frequency of the playback signal is called flutter and is generally measured over a frequency range of 0.5Hz + 0.200Hz.

Test tapes with low recorded flutter variations are available to test playback mechanisms. These tapes are standardized at 3kHz. With systems equipped with record heads, a 3kHz tone can be recorded for analysis."

[Note: A 565 may be used in place of the 561B since the frequency is quite low.]

FLUTTER METER USING 561B

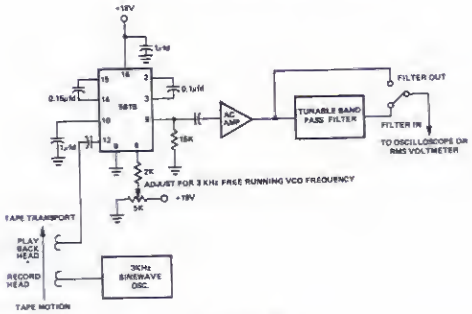


Figure 8–80

PHASE LOCKED LOOP FLUID FLOWMETER

Whenever a phase locked loop is locked, its VCO signal is 90° out of phase with the input signal (unless the input signal is off frequency and very weak). It has been found that the loop can lock to itself if its VCO signal is phase shifted 90° and then applied to the input. The loop will then run at whatever frequency develops a 90° phase shift in the phase shift network. An interesting application of this technique was submitted by Richard E. Halbach of Milwaukee, Wisconsin. Mr. Halbach used the time delay of a mass (bolus) of fluid moving through a length of tubing as a phase shift mechanism so that the PLL frequency became a function of the flow rate. Figure 8–81 shows this technique in block diagram form (a) and implemented using a 560B (b).

"Simply stated, Nuclear Magnetic Resonance (NMR) is that precession of nuclei, in this case hydrogen, in the presence of a magnetic field. Its precession can be detected by an appropriate receiver coil assembly. A coil up-stream from the receiver coil when activated changes the nuclear magnetization of a bolus (or mass) of fluid in such a way that this change can be detected in the receiver as the bolus subsequently passes through it...transport delay from the tag coil to the receiver, an inverse function of flow velocity, can be used to introduce a 90° phase lag into the external feed back loop of the PLL, which when matched with the 90° internal lag of the PLL, allows the loop to lock. The VCO frequency is then a direct function of velocity of flow."

[Note: A 565 can be used as well as the 560 at this low frequency. Frequency can be read out at the low pass filter (using a low frequency integrating voltmeter) or by measuring the period of the output waveform (flow is then inversely related to the period). If the VCO is run at a carefully chosen higher frequency and then divided down prior to the phase detector and tag coil, the frequency of the VCO as read by a counter can be adjusted to indicate in flow units directly.]

PHASE LOCKED LOOP FLUID FLOW METER

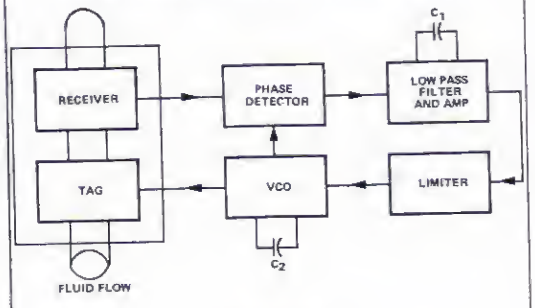
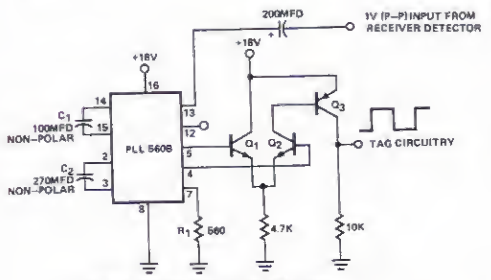


Figure 8–81a

PHASE LOCKED LOOP FLUID FLOW METER



C_1 WAS CHOSEN FOR STABLE LOOP OPERATION
R_1C_2 DETERMINES OPERATING FREQUENCY RANGE OF 1–3Hz
Q_1 Q_2 Q_3 FORM DIFFERENTIAL OUTPUT AND DRIVE FOR TAG CIRCUITRY

Figure 8–81b

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6. Mattis, J. A., "The Phase Locked Loop – A communication system building block", *Broadcast Engigineering,* Feb. 1972.
7. Grebene, A. B., "A monolithic signal conditioner/ synthesizer," *NEREM Record,* vol. 12, pp. 60–61, Nov. 1970.
8. Chu, L. P., "Phase-locked AM radio receiver," *IEEE Trans. Broadcast and Television Receivers,* vol. BTR-15, pp. 300–308, Dec. 1969.
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HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

INTRODUCTION

Traditionally, designers of analog voltage comparators have been confronted with a speed versus input parameters performance tradeoff. High speed in a comparator is attained primarily through smaller base geometry and low resistivity substrate. This has an adverse effect on breakdown voltage with a corresponding decrease in the common mode voltage range of the comparator. In addition, high speed comparators also employ gold doping to reduce storage time and thus decrease propagation delay. This causes unfavorable offset and bias currents in voltage comparators.

The development of the NE521/NE522 dual comparators has virtually eliminated this design tradeoff. The key element in this has been the use of Schottky diodes to clamp the switching transistors at a level above V_{CE} sat. By inhibiting saturation, and the corresponding storage time, transistor switching speed is increased significantly. The forward voltage of the Schottky diode is less than that of the base collector junction of the transistor. With the transistor in the active region, therefore the Schottky diode is reverse biased and has no effect on the transistor. As the transistor is driven towards saturation, the Schottky diode diverts excess base current from the collector-base junction, thus preventing the transistor from reaching classic saturation. Since there is no minority carrier storage associated with the barrier diode, the switching times will be very fast.

FEATURES

- GUARANTEED LARGE SIGNAL PROPAGATION DELAY OF 12ns MAX.
- TWO COMPARATORS PER PACKAGE
- ±5 VOLT SUPPLIES
- OUTPUT STROBE CAPABILITY
- INPUT BIAS CURRENT OF 20 μA MAX. OVERALL
- VOLTAGE GAIN OF 5000V/V

GENERAL DESCRIPTION

The SE/NE521 and SE/NE522 are state-of-the-art ultra high speed dual voltage comparators.

Overall system simplicity is achieved through the use of common and individual strobe controls. These inputs provide on-chip strobing and chip enable functions with no additional system propagation delay.

An additional feature of the 522 is its open collector output topology. Open collector allows the use of wired -OR output configurations, for overall system simplicity in memory designs.

Applying the 521/522 comparators is relatively straightforward. However, since the devices are capable of extremely wide bandwidths at very low signal levels, the following precautions should be taken.

The 521/522 is capable of resolving sub-millivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. During design of a system, attention should also be paid to the power supply lines. Good power supply bypassing should be provided close to the comparator. A tantalum capacitor of 1 to 10μfd in parallel with 500 to 1000pf will prove effective in most cases. Short lead length must be used if high frequency bypassing is to be achieved.

When using only one comparator of a package, the unused inputs should be biased in a known condition. The high gain bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known output state. If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

APPLICATIONS OF THE NE521/NE522 DUAL COMPARATORS

LEVEL DETECTOR

One of the primary applications of voltage comparators is to accomplish level detection of an input signal with a known reference levels. When the input signal exceeds the established reference limit, the comparator output changes states.

The 521/522 comparators are particularly well suited for voltage level detection. The overall voltage gain of the amplifier is 5000V/V, thus allowing level detector resolution in the millivolt level. Input bias current is typically 7.5 μA, thereby allowing the use of large source resistors for the level detector. Finally, Schottky clamping the 521/522 provides level detection in 20ns max for a 5mV overdrive.

The range of input signals acceptable to the comparator is bounded by two factors. First, the comparator must possess good small signal resolution. The major factors affecting sensitivity are gain and offset voltage. During the design, sufficient gain is provided to effectively eliminate its influence on resolution. In most IC comparators the DC input parameters of offset current and offset voltage determine the smallest voltage which may be compared. Second, large signal restrictions arise from the common mode range and differential input ranges of the comparator. The differential input range is usually larger than the common mode range and poses less of a problem. In the case of the 521/522 the common mode voltage is ±3 volts minimum.

If common mode signals larger than ±3 volts is anticipated the input and threshold voltages should be attenuated. Large voltages can be easily accommodated by including simple resistor dividers at the inputs.

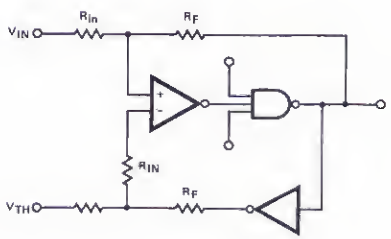
LEVEL DETECTION WITH HYSTERESIS

The amplifiers used in voltage comparators are seldom in the linear region; they are saturated high or low. To obtain maximum speed, the amplifiers in comparators are operated open loop and without frequency compensation.

If, however, the comparators are operated in the linear region, without frequency compensation, the outputs tend to oscillate. This is a common problem in successive approximations D/A converters, test equipment limit detectors, etc.

To avoid this oscillation in the linear range, hysteresis can be employed from output to input of the 521/522.

LEVEL DETECTOR WITH HYSTERESIS

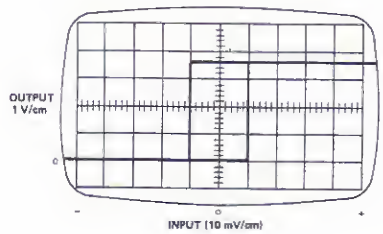


a.

FIGURE 1

Figure 1A shows the configuration for a level detector employing a 10mV positive and negative hysteresis loop. Since only one TTL output is available from the 521, an additional inverting gate is necessary to provide hysteresis below the threshold level.

0 VOLT LEVEL DETECTOR WITH ± 10mV HYSTERESIS



b.

FIGURE 1

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to threshold the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 1B, prevents output chatter with signals having slow and erratic zero crossings.

As is shown in Figure 1A the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \cdot R_{IN}}{R_{IN} + R_f}$$

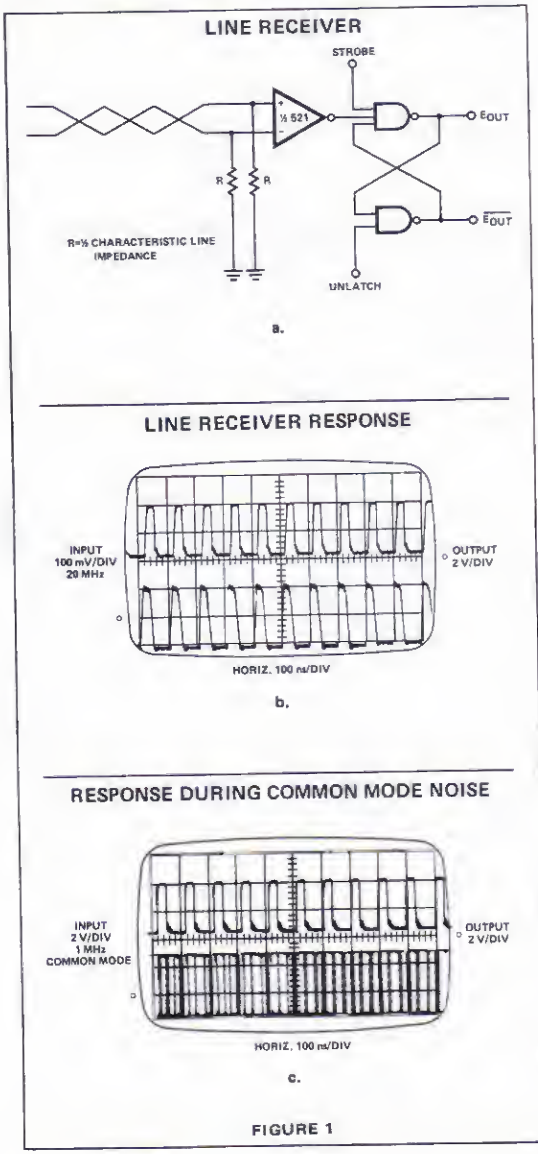
where E_{OUT} is the gate output voltage. The hysteresis voltage is bounded by the common mode range (±3 volts) and the ability of the gate to source the current required by the feedback network.

LINE RECEIVER

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

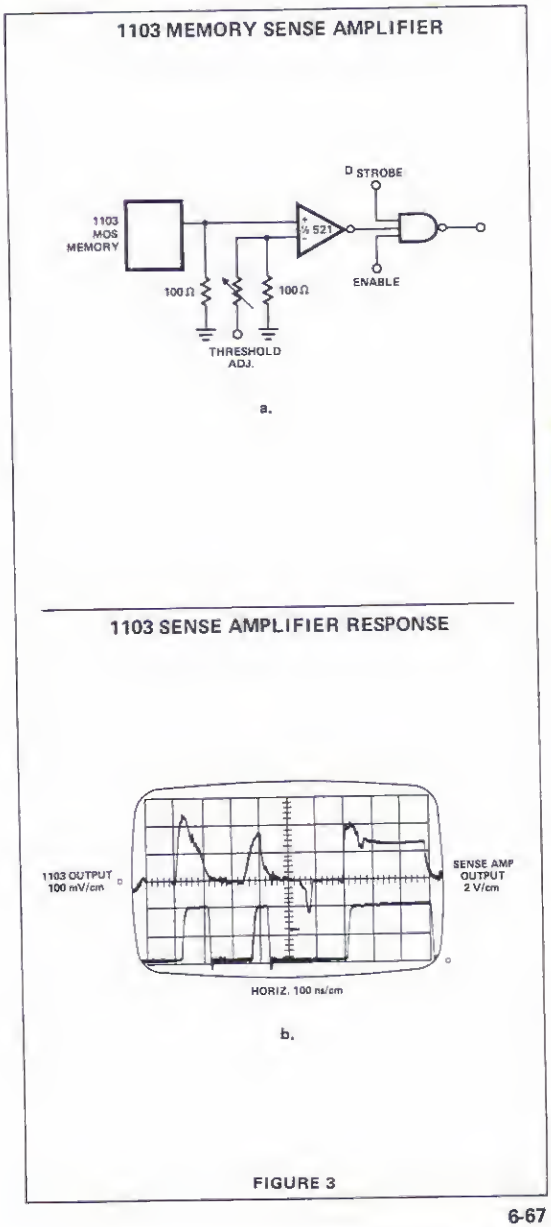
Since the electrical noise imposed upon a pair of wires takes the form of a common mode signal, the very high common mode rejection of the 521/522 makes the unit ideal for differential line receivers. Figure 2A depicts the simple schematic arrangement. The 521 is used as a differential amplifier having a logic level output. Because common mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 2B illustrates the 521 response to a 200mV peak to peak 10MHz differential signal. In Figure 2C the same signal has been buried in 5 volts peak to peak of 1MHz common mode "noise". As shown the circuit suffers no degradation of signal. If desired several 522 comparators may be "wire -OR'D", or a latch output can be accomplished as shown.



SENSE AMPLIFIER

Current outputs of the 1103 MOS Memory, require sense amplifiers for conversion to standard DTL/TTL logic. The 521/522 comparators are ideal in this application because of the low offset voltage, low offset current, and high speed. Use of the Schottky clamped comparators significantly increase total access time of the semiconductor memory. In large memory systems, the NE522 can be used for the "wire -or'd" memory data lines.

Figure 3A shows a typical memory configuration with a photograph of the 521 response appearing in Figure 3B.



PEAK DETECTOR

Peak detection of a signal may be quickly obtained by connecting a voltage comparator as shown in Figure 4A. When a signal is applied to the positive input the negative input is charged to the peak value of that signal through the diode. Some stored charge then provides input bias current, discharging the inverting input to slightly below the peak signal. At the peak of the following cycle the input exceeds the stored charge causing the output to go high. With the output high the diode furnishes an additional charge to the inverting input which causes the output to go low again. Thus the output is a pulse beginning at the peak of the input waveform and having the duration equal to the inverting input.

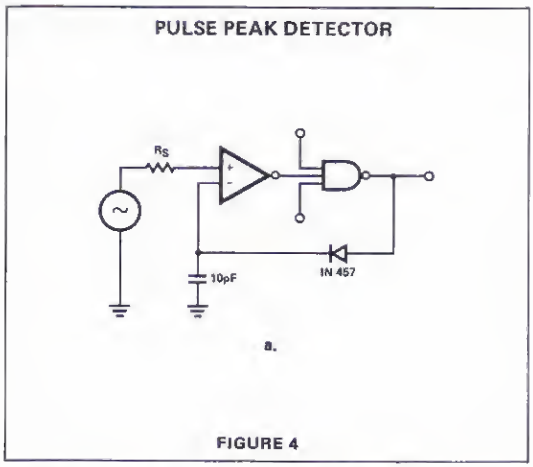


FIGURE 4

Figures 4A and 4B show the diagram and the response of such a circuit to a 20MHz, 1 volt peak-to-peak sine wave. The 1N457 diode was selected for its relatively slow turn on time to increase the feedback delay time. If desired a resistor may be added in series with the diode to provide an additional RC time constant to increase the pulse width even further.

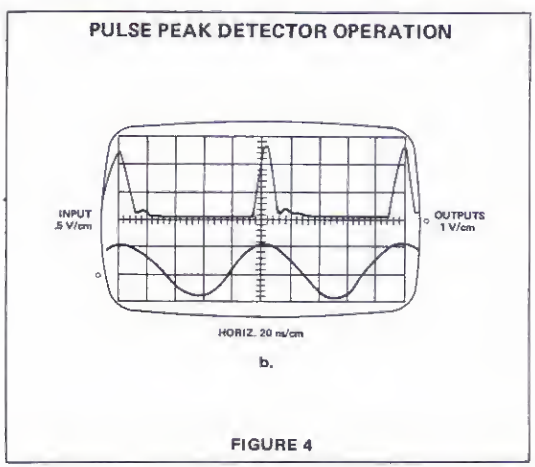


FIGURE 4

DOUBLE ENDED LIMIT DETECTOR

Many systems designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single 522 package. The schematic and transfer curve of the circuit is shown in Figure 5.

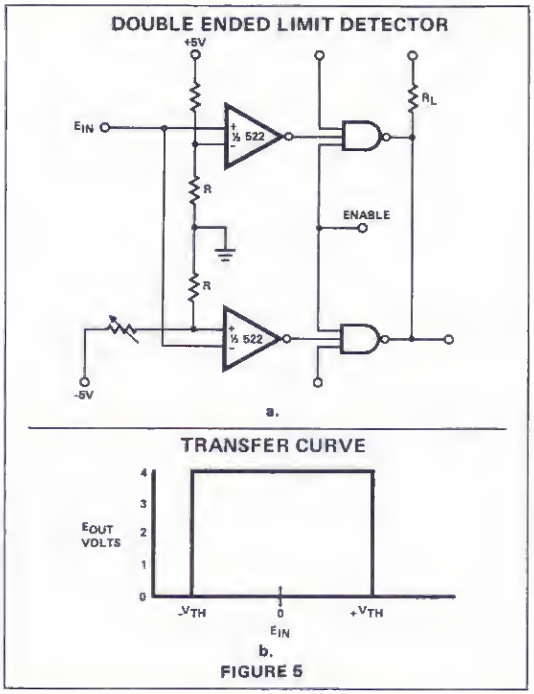


FIGURE 5

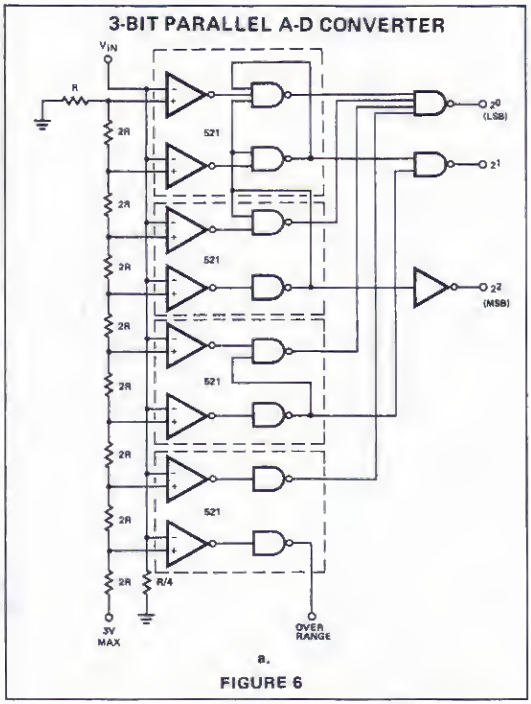
ANALOG TO DIGITAL CONVERTER

There are many types of A to D converter designs. Each has its own merits. However, where speed of conversion is of prime interest the multi-threshold parallel conversion type is used exclusively. It is apparent from Figure 6B that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2^{n-1}. Although the 521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3 bit parallel A-D converter is shown in Figure 6A with a 3 bit digital equivalent of an analog input shown in 6B.

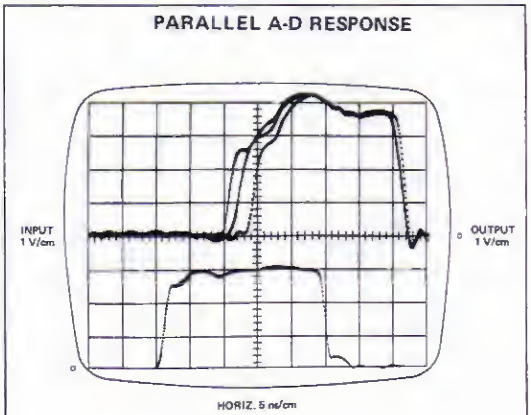
Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ±½ bit.



a.

FIGURE 6

It is apparent from the schematic that the individual strobe line and duality features of the 521 has greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 6B. All 3 bit outputs have settled and are true a mere 15ns after the input step of 3 volts has arrived. The output is, therefore, usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.



b.

FIGURE 6

OSCILLATORS

Any device with a resonable gain can be made to oscillate by applying positive feedback in controlled amounts. The 521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 7 shows a typical oscillator circuit.

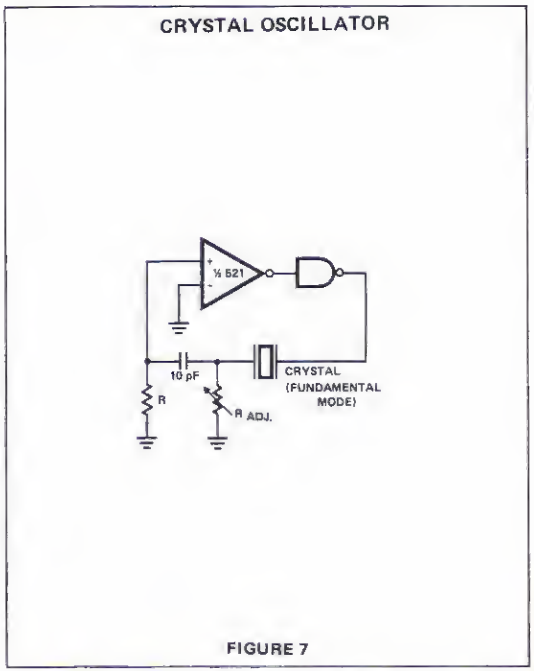


FIGURE 7

The crystal is operated in its series resonant mode, providing the necessary feedback through the capacitor to the input of the 521. The resistor R_{adj} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs.

The 521 will oscillate up to 70MHz. However, crystals with frequencies higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out the crystal will tend to oscillate at the fundamental frequency.

CONCLUSION

The NE521/NE522 dual Schottky clamped devices represent a new concept in comparators; super-speed with precision input characteristics. As such, the applications for the devices are abundant. The penalties of high speed comparators has been over come with the advent of the NE521/NE522, so, in this note, we have tried to key on a few of the more important applications that take advantage of the features of the device. In general, the NE521/NE522 represents a significant breakthrough in comparator technology and will interface well with the new generation digital and linear systems in design today.

FAST SLEWING OPERATIONAL AMPLIFIER

INTRODUCTION

Monolithic operational amplifiers have become some of the most widely used components in linear system design. These devices have achieved success, in spite of poor AC response, primarily due to low cost and excellent DC characteristics. A fast slewing monolithic operational amplifier, the SE/NE 531, offers vastly improved AC performance while retaining DC characteristics equal to the best general purpose types.

A circuit diagram of the monolithic chip is shown in fig. 1. A unique aspect of the circuit is the input state, which achieves a wide dynamic range by means of its class B operation. The differential input signal is developed at the bases of Q7 and Q8. Q13, Q15, and Q16 form a unity gain current inverter which causes the input signal to appear single ended at the base of Q14. Q14 is an emitter follower which buffers the signal to Q33. It will be seen that Q33 drives the cascade connected output stage which includes the double cross coupled emitter follower, Q27, Q28, Q29, and Q20. The entire circuit arrangement has been found to be quite satisfactory, offering fast slewing and excellent stability at virtually no degradation in DC characteristics over previously available units.

SCHEMATIC DIAGRAM

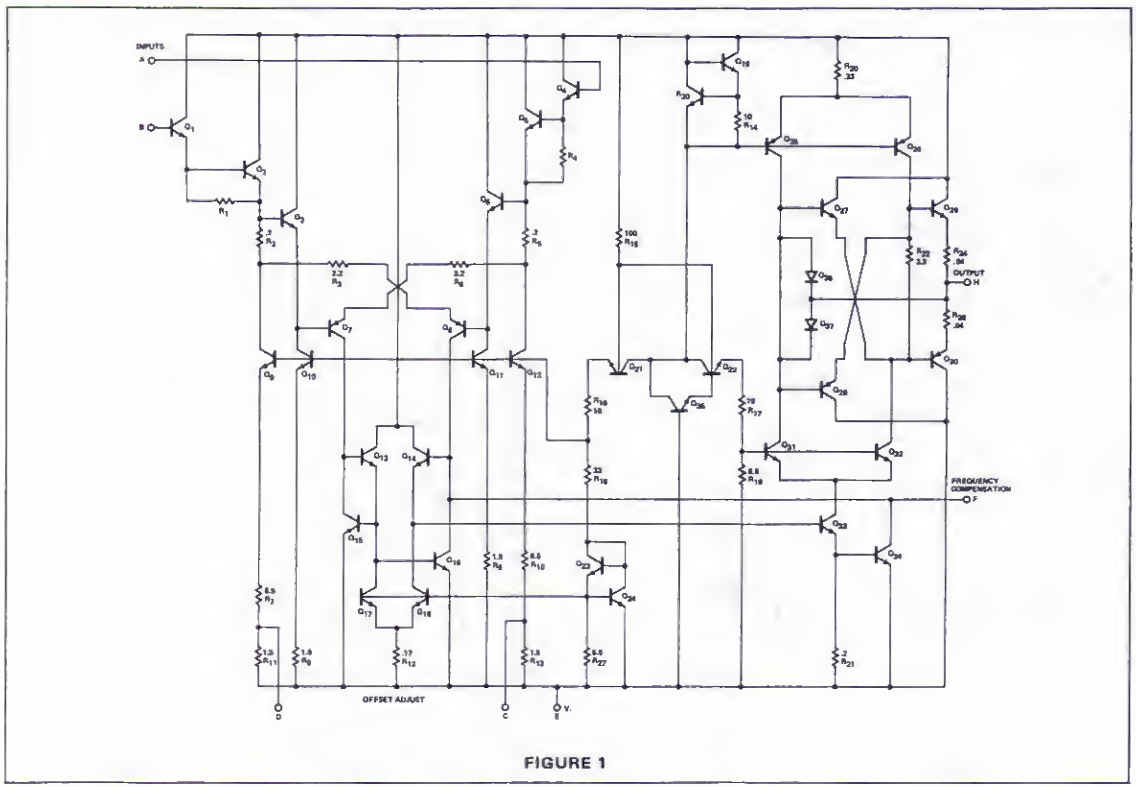
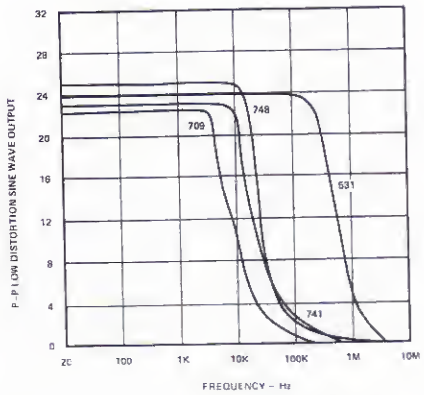
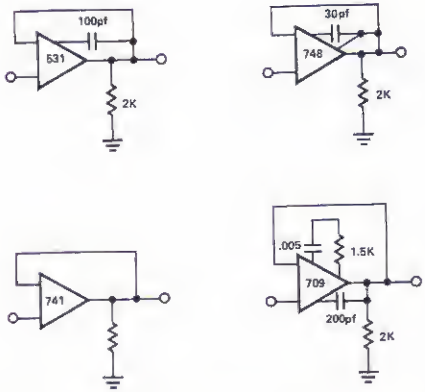


FIGURE 1

The principal advantage of the 531 over older devices is apparent from an examination of the large signal and small signal frequency response curves, shown in Fig. 2a and Fig. 2b. The large signal response indicates that, in the Voltage Follower (A_V = +1) configuration, the 531 can deliver undistorted large amplitude sine waves at much higher frequencies than any of the other circuits. The small signal plots show a similar advantage in the A_V = -100 amplifier configuration.

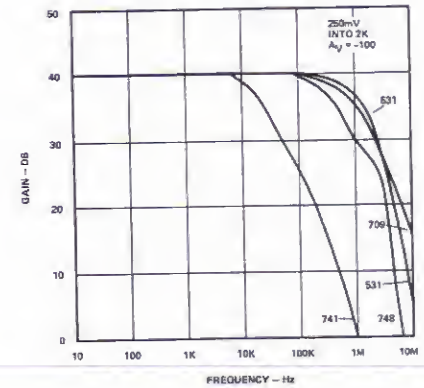
LARGE SIGNAL FREQUENCY RESPONSE A_V=+1

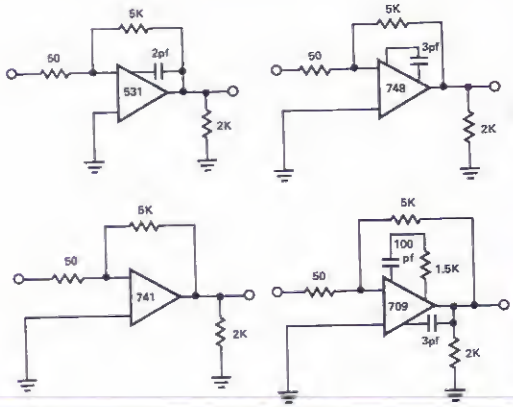




a.

SMALL SIGNAL FREQUENCY RESPONSE





b.

FIGURE 2

Superior ac response allows the use of the new general purpose device in many applications where it would previously have been difficult or impossible to use an operational amplifier. An excellent example is the fast setting voltage follower of Fig. 3. This is the simplest circuit possible utilizing an op amp, but because of the slew limited response of older devices, its use has been limited. A 531 connected as a voltage follower can give performance superior to specialized voltage follower integrated circuits, providing a .01% settling time of 2.5μsec on 20 volt input pulses.

An application which makes good use of the fast settling characteristics of the 531 is the sample and hold circuit of Fig. 4. In this circuit, the instantaneous value of an input signal is sampled at the time of the strobe pulse and held at the output until the occurrence of the next strobe pulse. The sample and hold is useful in a variety of applications, including multiplex demodulation.

FAST SETTLING VOLTAGE FOLLOWER

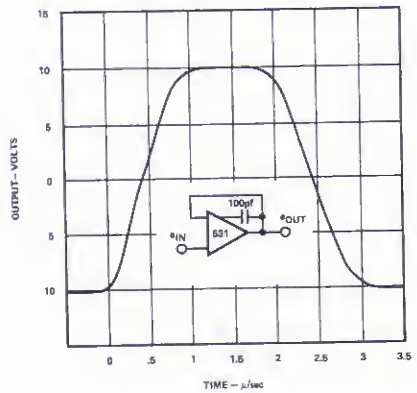


FIGURE 3

SAMPLE AND HOLD

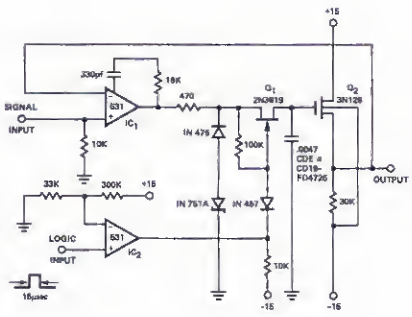


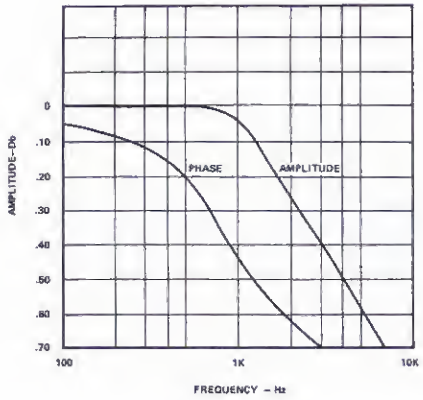
FIGURE 4

The operation of the circuit is quite simple: A strobe pulse developed from a logic input at IC_2 turns on Junction FET Q_1. This completes the feedback loop, IC_1, Q_1 and Q_2, and forces the capacitor C_1 to charge to a voltage equal to the input voltage plus the gate to source offset voltage of the MOS transistor Q_2. At the end of the strobe time, the loop is broken, and this voltage is held by capacitor C_1 until the time of the next strobe pulse. Using the MOS FET in this way, of course, minimizes greatly any drift or offset, and results in a tracking accuracy of better than .01%.

With the components shown, a 15 microsecond strobe pulse was used and the decay of the output voltage between samplings was measured at less than 1 millivolt per second. It should be noted, however, that to achieve this performance the circuit board should be clean and free from moisture.

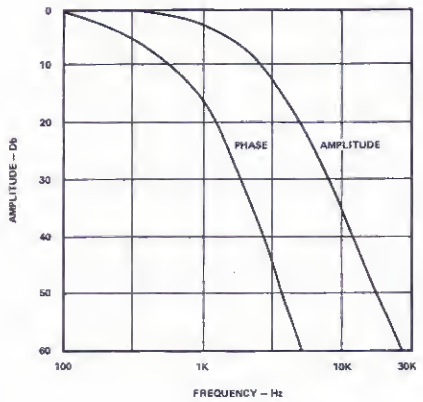
The use of operational amplifiers in active filters has received a great deal of attention, but one particular configuration has been largely neglected. This configuration, which uses cascaded op amps, each contributing one complex pole-zero pair, may be used to synthesize many different kinds of high-pass and low-pass filters. With the 531, this configuration is particularly useful, yielding filters which work to above 100k Hz and which will handle large input and output voltage swings. Figure 5a is a plot of the measured frequency response of a 4 pole Butterworth filter of this type, showing the 80 dB/decade rolloff and maximally flat amplitude characteristic. Figure 5b is a plot of a filter identical in form, but with R and C values adjusted for the Bessel, or maximally flat delay, characteristic. The deviation of these measured curves from the theoretical filter characteristic is virtually unmeasurable.

4 POLE LOW PASS ACTIVE BUTTERWORTH FILTER



a.

4 POLE LOW PASS ACTIVE BESSEL FILTER

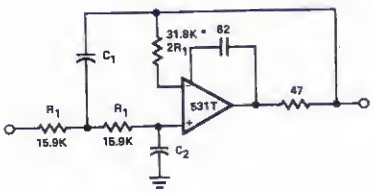


b.

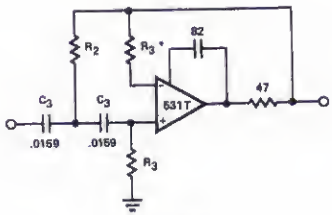
FIGURE 5

ACTIVE FILTERS (2, 3, AND 4 POLE)

2-POLE



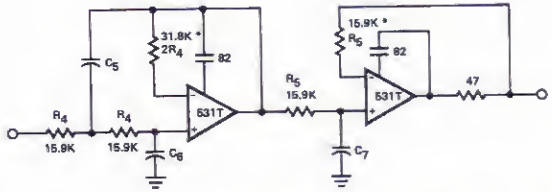
LOW PASS



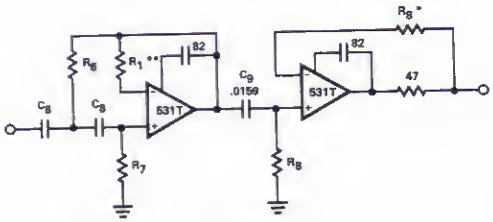
HIGH PASS

1kHz FILTER		
R OR C	BUTTER-WORTH	BESSEL
C_1	.0141	.00667
C_2	.00707	.005
R_2	7.07k	15k
R_3	14.1k	20k

3-POLE



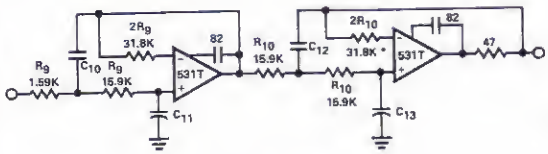
LOW PASS



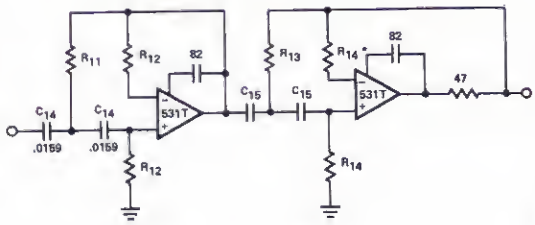
HIGH PASS

1kHz FILTER		
R OR C	BUTTER-WORTH	BESSEL
C_5	.0200	.00644
C_6	.00600	.00265
C_7	.0100	.00431
R_6	5.00k	18.4k
R_7	20.0k	35.1k
R_8	10.0k	23.2k

4-POLE



LOW PASS



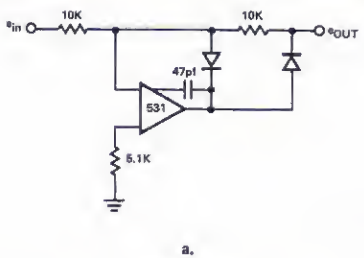
HIGH PASS

1kHz FILTER		
R OR C	BUTTER-WORTH	BESSEL
C_{10}	.0261	.00345
C_{11}	.00385	.00317
C_{12}	.0108	.00475
C_{13}	.00924	.00183
R_{11}	3.83k	29.0k
R_{12}	26.1k	31.6k
R_{13}	9.24k	21.0k
R_{14}	10.8k	54.6k

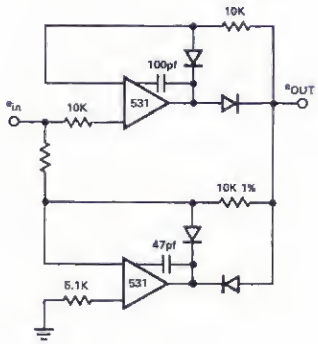
FIGURE 6

Figure 6 is a tabulation of the R and C values for 2, 3 and 4 pole Butterworth and Bassel filters. For frequencies other than 1k Hz, the capacitor values should be scaled inversely with the frequency ratio; thus, for 2k Hz filters, halve the capacitor sizes. For 500Hz, double the values shown etc. Butterworth and Bessel filters are only two of the filters which may be synthesized using this technique. For a complete discussion of this circuit, see Reference 1.

PRECISION RECTIFIERS



a.
HALF WAVE



b.
FULL WAVE

FIGURE 7

Two useful circuits are the precision rectifiers of Figure 7. These circuits use diodes in the feedback loop to obtain highly accurate half and full wave rectification with negligible dead zone and independent of the diode characteristics. It is found, however, that when these circuits are implemented with the most commonly used general purpose operational amplifiers serious distortion appears in the output at frequencies above a few hundred Hz. This is caused by the transients generated when the amplifiers switch through the dead zone in the circuit feedback loop. With ordinary operational amplifiers, the designer must either live with this problem or resort to far more elaborate and less accurate circuits. When the 531 is used in the arrangement shown, however, the circuits have negligible distortion and are usable to at least 10k Hz.

VOLTAGE CONTROLLED AMPLIFIER

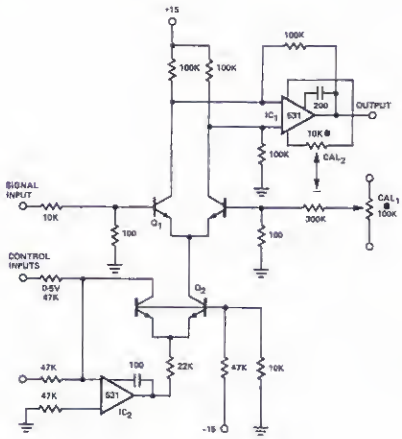


FIGURE 8

In some applications, an amplifier is required in which the gain may be remotely adjusted by a control voltage, and in which the control voltage does not appear in the output (2 quadrant multiplier). Such a design is shown in Figure 8. This circuit accepts a 0 to 5V control voltage and has an input signal range of ±2.5V for low distortion. Q_1 is a low noise dual transistor with a 2 millivolt or better V_{be} match and functions as a current controlled amplifier. Q_2 is a similar transistor which, in combination with IC_2 generates the control current for Q_1. IC_1 servies as a buffer and level shift amplifier. The amplifier has full large signal and small signal output from DC to about 300k Hz, and a noise level 60-70 dB below full output.

HIGH SPEED INVERTER

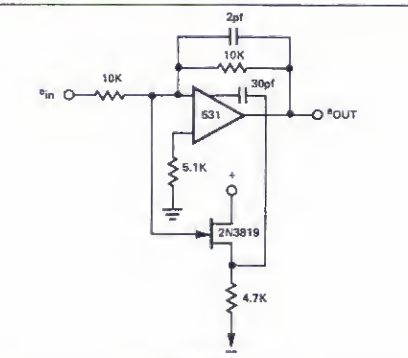


FIGURE 9

Because of the low excess phase of the 531 output stage, it is possible to utilize feed-forward compensation techniques to achieve improved small signal bandwidth and slew rate.

Figure 9 is a high speed inverter realized by feed forward compensation. The bandwidth of this circuit is about 10m Hz and the slew rate better than 60V/μsec. In addition, frequency peaking with the attendant overshoot is nearly absent.

There are few special precautions to be observed when using 531. Observing the normal design practices for any general purpose monolithic op amp will give excellent results. Some simple rules are:

1. Power Supply bypassing with small .01μf ceramic capacitors is required for stability.

2.When using the 531 at less than ±15 volt supplies, the usable negative common mode range decreases. The negative common mode input range is -10 volts at VS = ±15V. At VS = ±9 volts, it is -4 volts.

Thus the negative common mode range decreases by 1 volt for every 1 volt decrease in the negative supply.

3.Compensation of the 531; Fig. 10 shows the value of the required compensation capacitor as a function of the closed loop gain. The upper curve is for noninverting amplifiers and the lower curve is for inverting amplifiers.

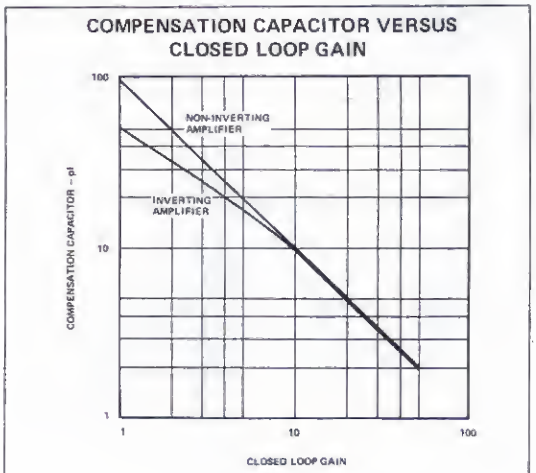


FIGURE 10

The circuits which have been described here, when implemented with the 531, offer better performance than those previously obtainable with general purpose operational amplifiers such as the 709, 741, 748, 101, etc. The advantages of this unit should justify its increasingly wide use as a general purpose operational amplifier wherever good AC response is required.

REFERENCES:

1. "RC Filter Design By The Numbers," Russel Kincaid, *The Electronic Engineer*, October 1968, PP. 57-64.

TOUCH TONE® TELEPHONE ENCODER

INTRODUCTION

The Signetics SE/NE 566 is a voltage controlled oscillator which lends itself easily to frequency shift or swept frequency signal generation. The purpose of this memo is to familiarize the reader with the Touch Tone® telephone system and offer a solution for the generation of necessary tones.

The Touch Tone® system represents each of the digits from 0 thru 9 with two tones of different frequencies. A four by four matrix is set up for this purpose, yielding sixteen possible combinations of the eight tones. Refer to Figure 1 for the frequencies and tone allocations.

	1209	1336	1477	1633
697	1	2	3	Spare
770	4	5	6	Spare
852	7	8	9	Spare
941	Spare	0	Spare	Spare

FIGURE 1

Ten of these combinations are used for the digits 0 thru 9. The remaining six combinations are used by the telephone company for special signaling purposes.

Common user telephones utilize only a 3 X 4 matrix. This arrangement covers the digits 0 thru 9 with 2 matrix positions not being used.

Since a 3 X 4 matrix arrangement is the most common, the circuit design described here will deal only in these seven frequencies. It is a simple matter, however, to expand the system to a 4 X 4 or even larger matrix if desired. One need only to add the additional timing resistors.

The frequency of the 566 may be changed by any one of three methods; by changing the capacitor C_1, by controlling the voltage at pin 5 or by changing the charging current by changing the value of R_1. Since the generation of tones in this case is a switching function from one tone to another, the latter frequency control method is used. Two SE/NE 566 VCO's are used to produce the two simultaneous frequencies required.

SCHEMATIC DIAGRAM

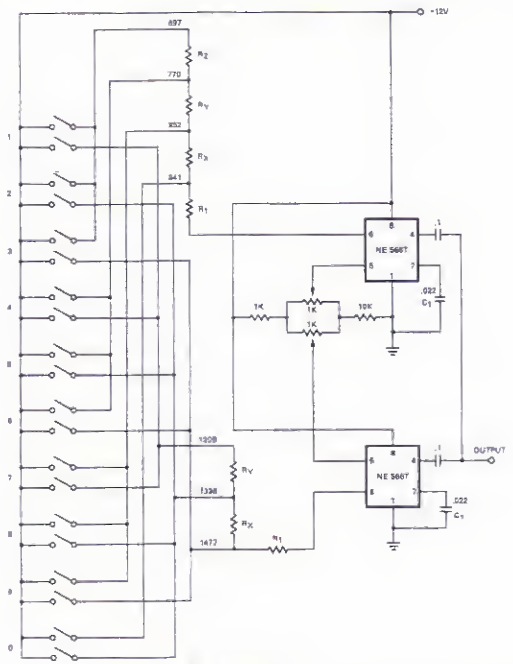


FIGURE 2

The VCO operating frequency is determined by:

$$f_o \simeq \frac{2}{R_1 C_1} \cdot \left[\frac{V_8 - V_5}{V_8 - V_1}\right]$$

Where V_8, V_5 and V_1 are voltages at pins 8, 5 and 1 respectively.

C_1 is selected at .022 μfd for both oscillators and R_1 is selected at 12.1K and 6.8K. These values set up the highest frequency to be generated. Due to the high linearity of the VCO, additional resistors may now be calculated to program the remaining frequencies. (See Figure 2). Ratios may be easily used to determine the values:

$$R_X = \frac{F_1 R_1}{F_2} - R_1$$

Where F_1 is the next higher frequency, R_1 is the known resistor and F_2 is the new frequency desired. The resistor R_X is then placed in series with R_1. R_Y is now determined by ratio:

$$R_Y = \frac{F_2 (R_X + R_1)}{F_3} - (R_X + R_1)$$

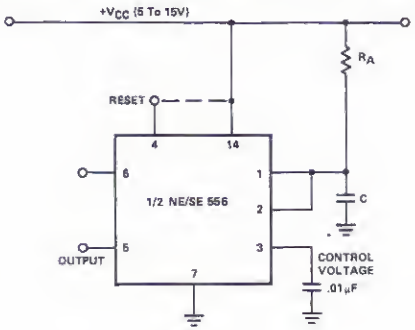
It should be noted here that total resistances between 2K and 20K ohm should be used for R_1 to insure temperature stability and linear operation.

Calibration of only one of the frequencies is needed since all the frequencies are set by resistor's ratios. A dc control voltage at pin 5 is required for circuit operation. A trimmer at this point is all that is required for calibration. The trimmer should be adjusted to obtain the proper frequency at the output of the 566 depending upon which keyboard switch is closed.

APPLICATIONS INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.



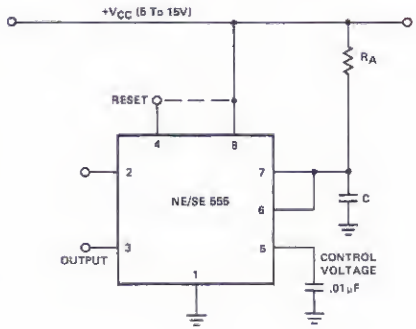


FIGURE 1a.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant $\tau = R_A C$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t = 1.1\ R_A C$ and can easily be determined by Figure 1c. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing

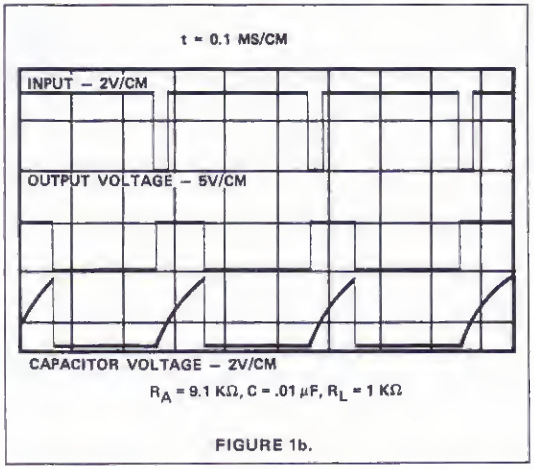


FIGURE 1b.

interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

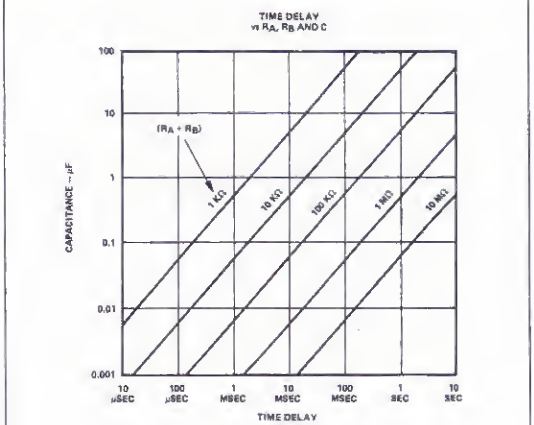
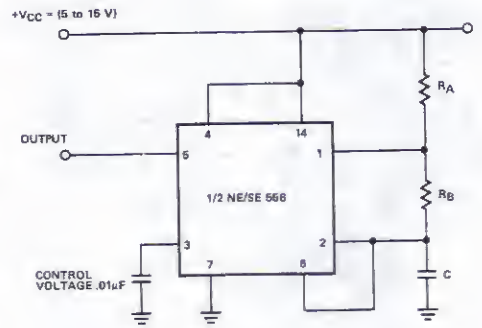


FIGURE 1c.

ASTABLE OPERATION

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

APPLICATIONS INFORMATION (Cont'd)



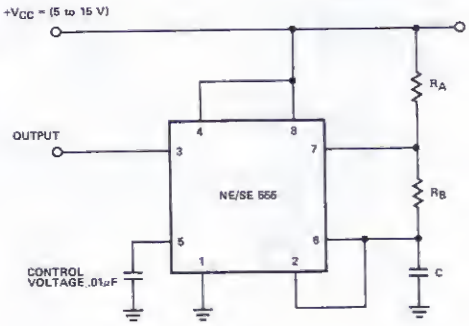


FIGURE 2a.

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.

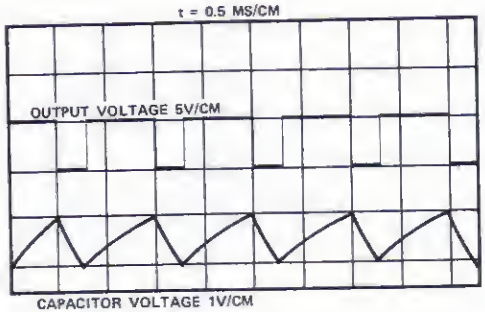


FIGURE 2b.

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

and the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

and may be easily found by Figure 2c.

The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

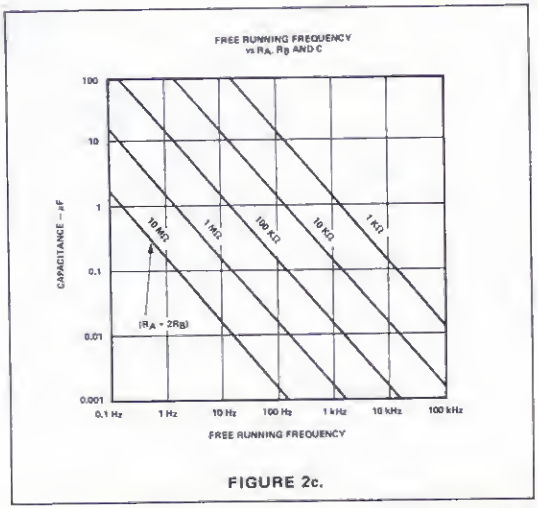


FIGURE 2c.

HERE ARE SOME ADDITIONAL INGENIOUS APPLICATIONS DEVISED BY SIGNETICS ENGINEERS AND SOME OF OUR CUSTOMERS.

MISSING PULSE DETECTOR

Using the circuit of Figure 3a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 3b shows the actual waveforms seen in this mode of operation.

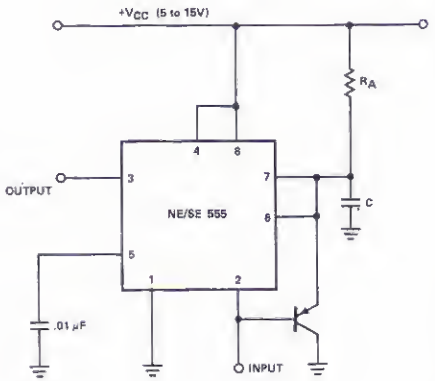


FIGURE 3a.

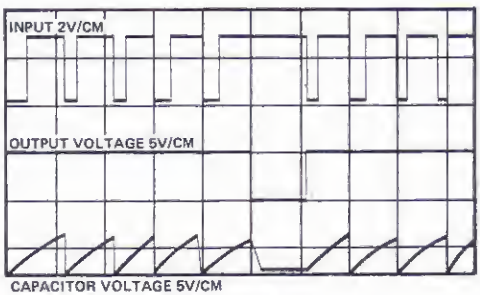


FIGURE 3b.

FREQUENCY DIVIDER

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle. Figure 4 shows the waveforms of the timer in Figure 1a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

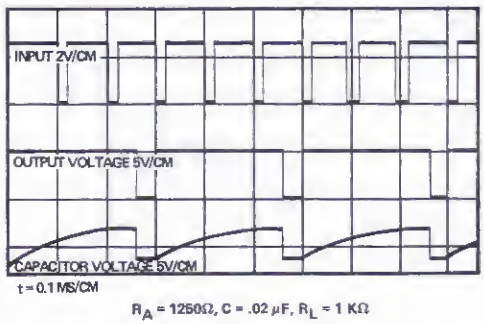


FIGURE 4.

PULSE WIDTH MODULATION (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 5a. The circuit is triggered with a continuous pulse train and the threshold voltage is

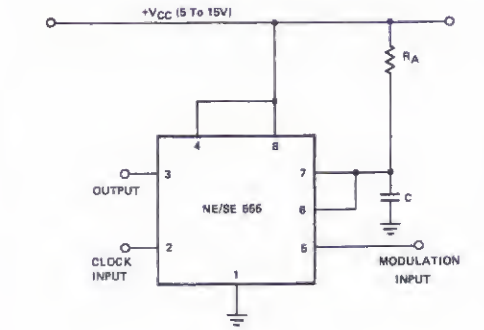


FIGURE 5a.

APPLICATIONS INFORMATION (Cont'd)

modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 5b shows the actual waveforms generated with this circuit.

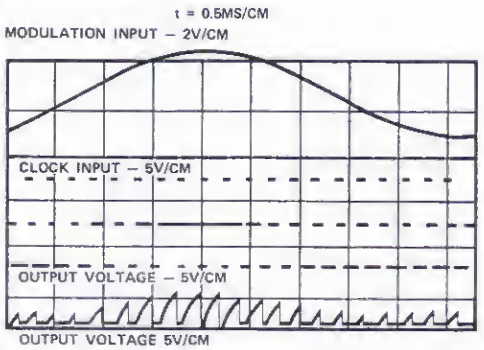


FIGURE 5b.

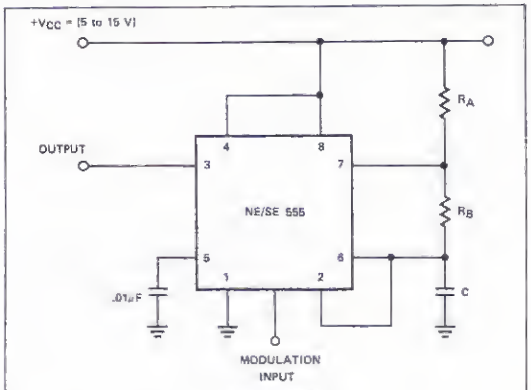


FIGURE 6a.

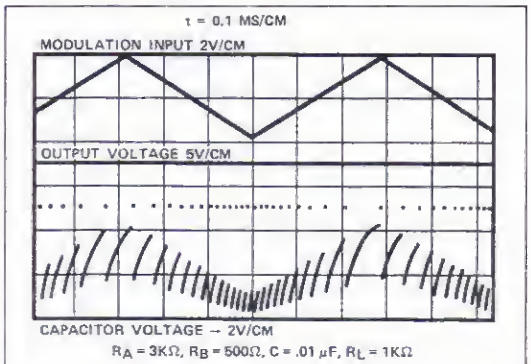


FIGURE 6b.

PULSE POSITION MODULATION (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 6a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 6b shows the waveforms generated for triangle wave modulation signal.

TEST SEQUENCER

Figure 7 shows several timers connected sequentially. The first timer is started by momentarily connecting pin 2 to ground, and runs for 10 msec. At the end of its timing cycle, it triggers the second circuit which runs for 50 msec. After this time, the third circuit is triggered. Note that the timing resistors and capacitors can be programmed digitally and that each circuit could easily trigger several other timers to start concurrent sequences.

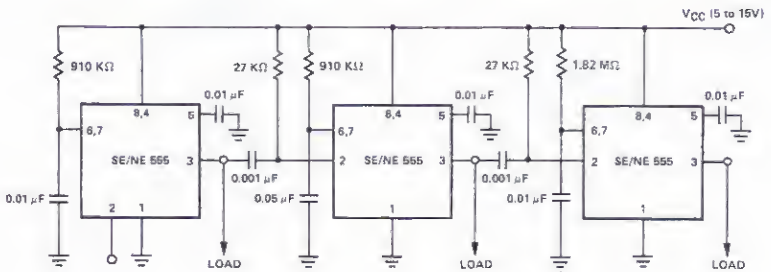


FIGURE 7.

APPLICATIONS INFORMATION

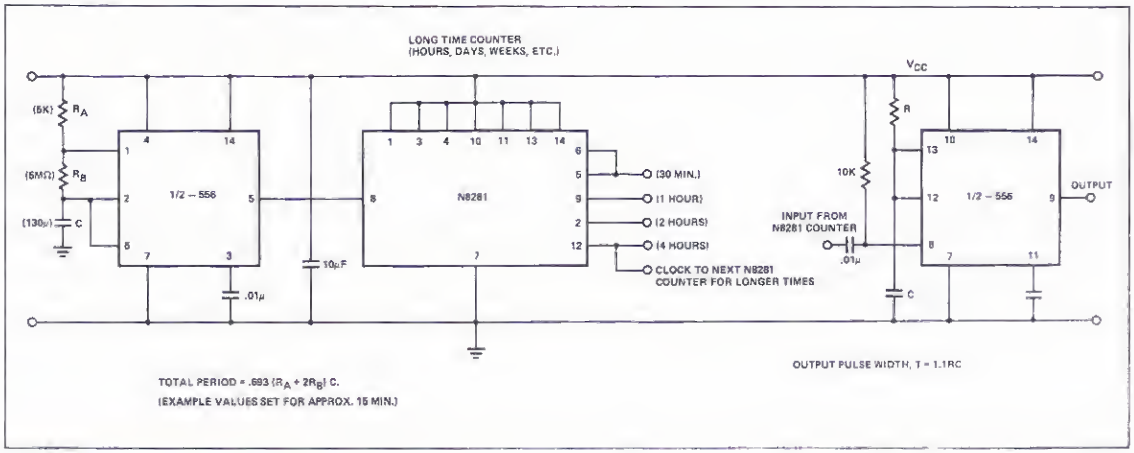
Each half of the 556 behaves like a separate 555 timer and as such all of the applications indicated in the Data Sheet for the 555 also are applicable to the 556.

LONG TIME DELAYS

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays expensive capacitors with extremely low leakage are required. The practicality of the components involved limits the time between pulses to something in the neighborhood of ten minutes.

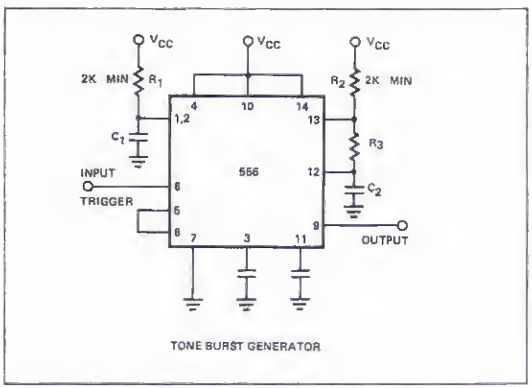
To achieve longer time periods both halves may be connected in tandem with a "Divide-by" network in between the first timer section operates in an oscillatory mode with a period of $1/f_0$.

This signal is then applied to a "Divide-by-N" network to give an output with the period of N/f_0. This can then be used to trigger the second half of the 556. The total time delay is now a function of N and f_0.



TONE BURST GENERATOR

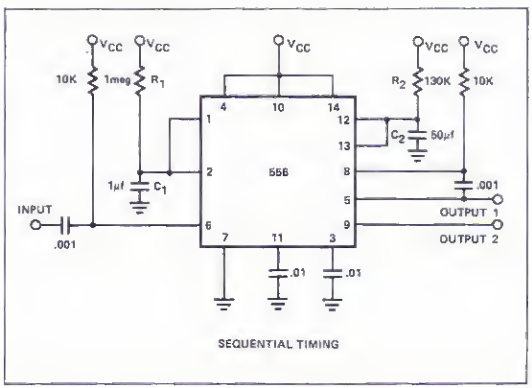
The 556 Dual Timer makes an excellent Tone Burst Generator. The first half is connected as a one shot and the second half as an oscillator.



The pulse established by the one shot turns on the oscillator allowing a burst of pulses to be generated.

SEQUENTIAL TIMING

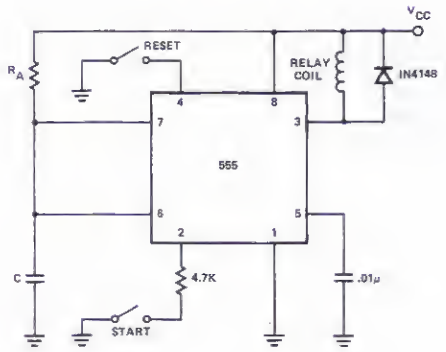
One feature of the Dual Timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a .001μfd coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay.



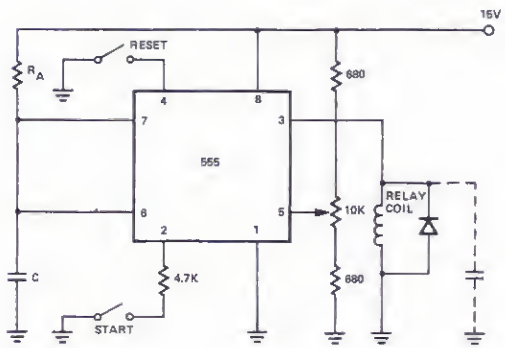
The first half of the timer is started by momentarily connecting pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its time duration is determined by $1.1R_2C_2$).

APPLICATIONS

SIMPLE TIME DELAY

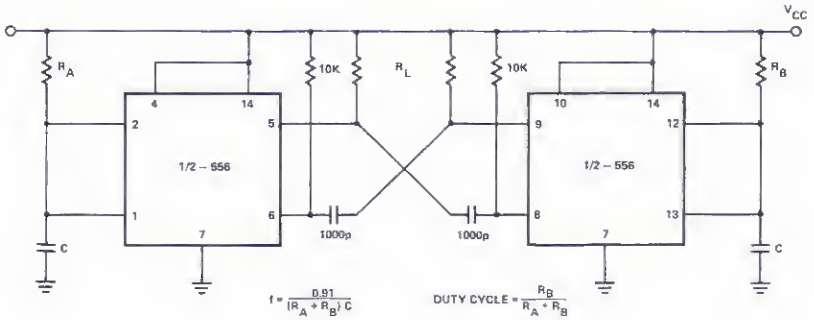


SIMPLE TIME DELAY



APPLICATIONS (Cont'd)

DUAL ASTABLE



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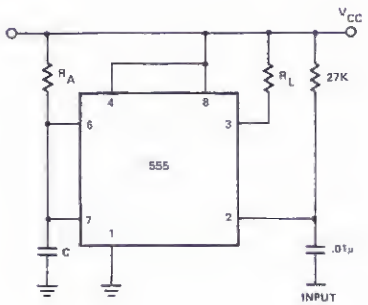

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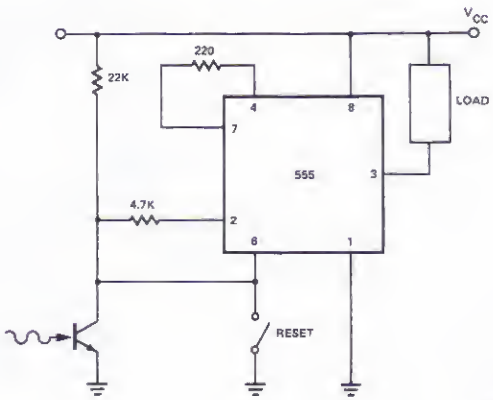
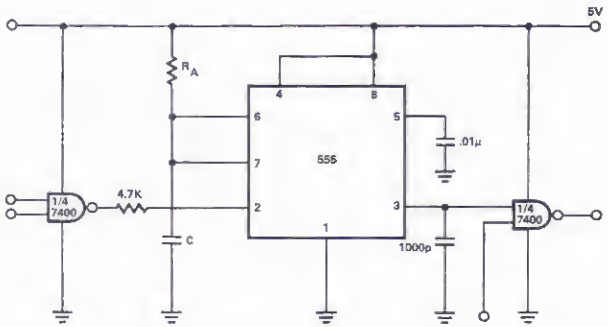
BURGLAR ALARM



TTL MONOSTABLE



APPLICATIONS (Cont'd)

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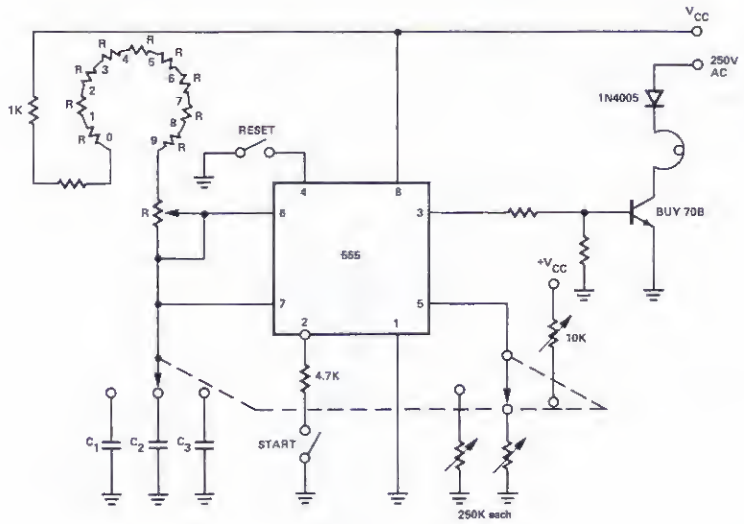
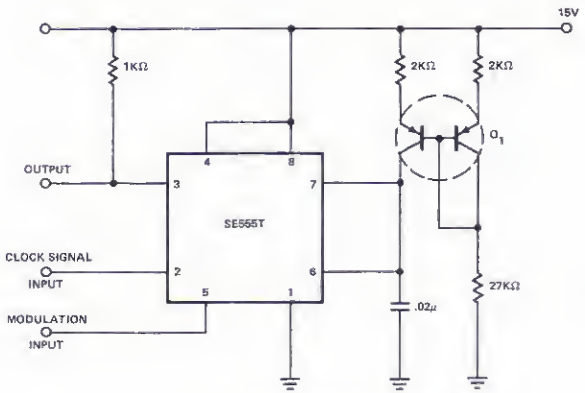


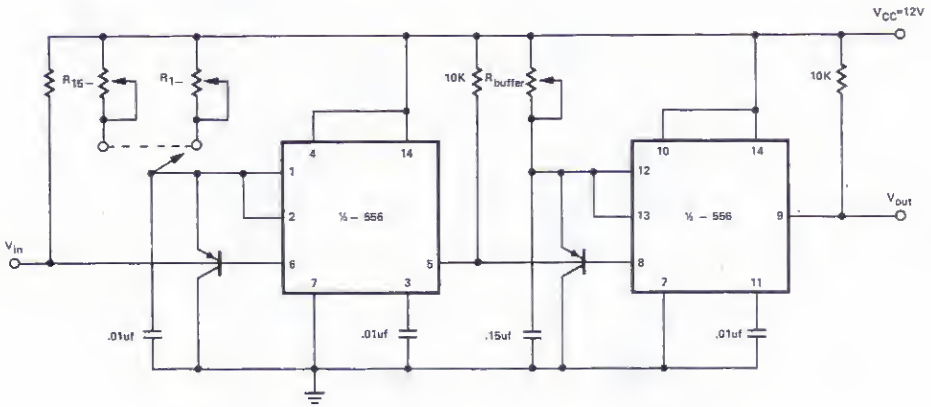
LINEAR PULSE WIDTH MODULATOR



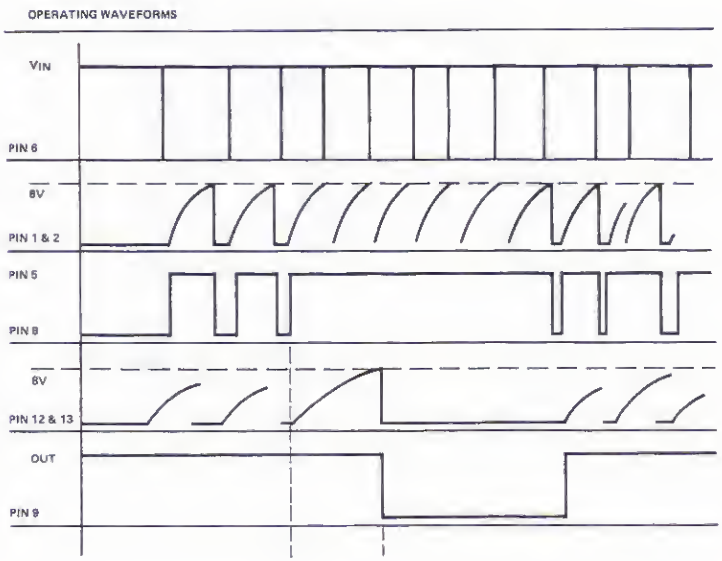
LINEARITY, ±0.2% over +4 to +12 volt input

(Cont'd)

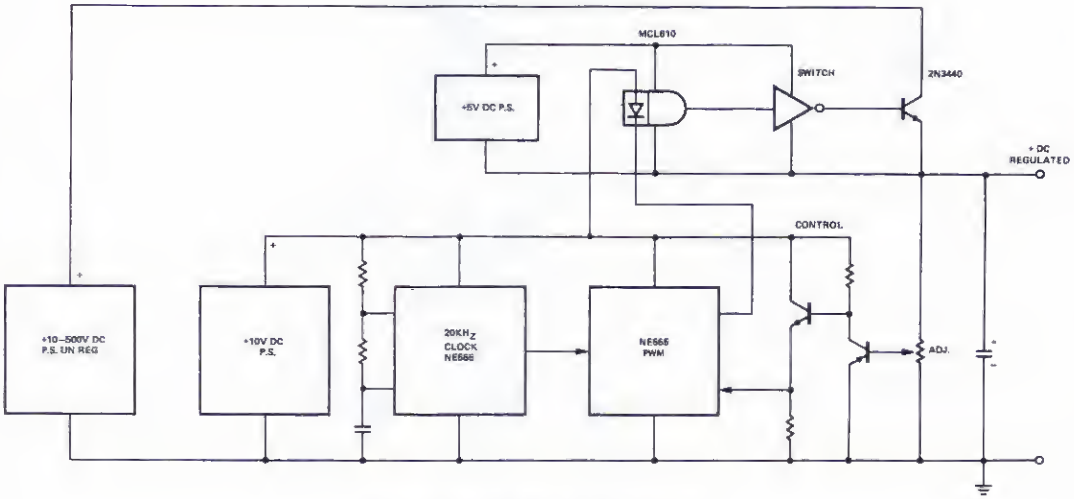
SPEED WARNING DEVICE



OPERATING WAVEFORMS

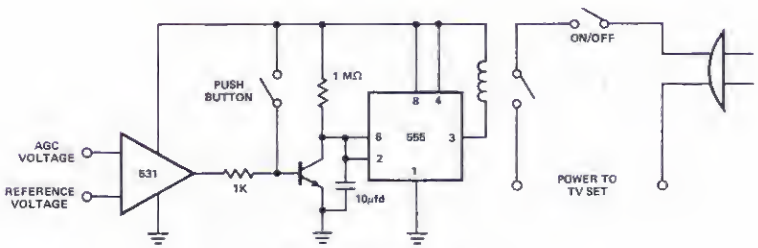


REMOTE CONTROLLED DC SWITCHING REGULATOR



APPLICATION–A PULSE WIDTH MODULATOR TO FEED DIGITAL PULSES INTO SWITCHING SECTION OF REGULAR PROPORTIONAL TO ERROR SIGNAL, ADJUST POT CAN BE REMOTELY POSITIONED.

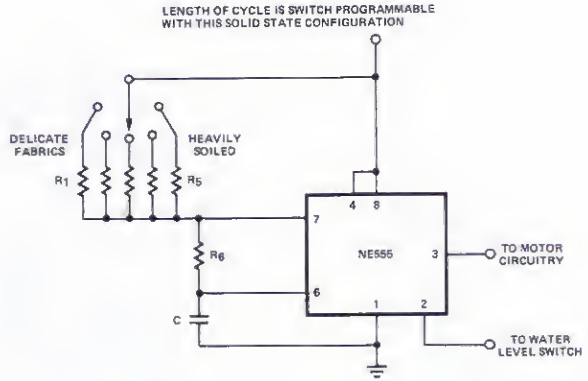
AUTOMATIC TURN OFF FOR TV SET



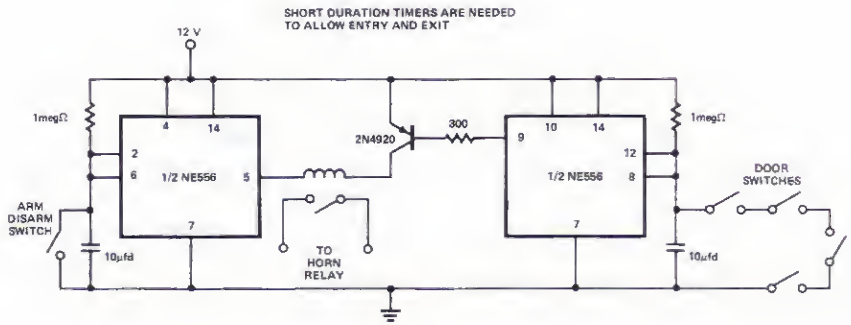
SET TURNS OFF SHORTLY AFTER TV STATION STOPS BROADCASTING

APPLICATIONS (Cont'd)

WASHER TIMER

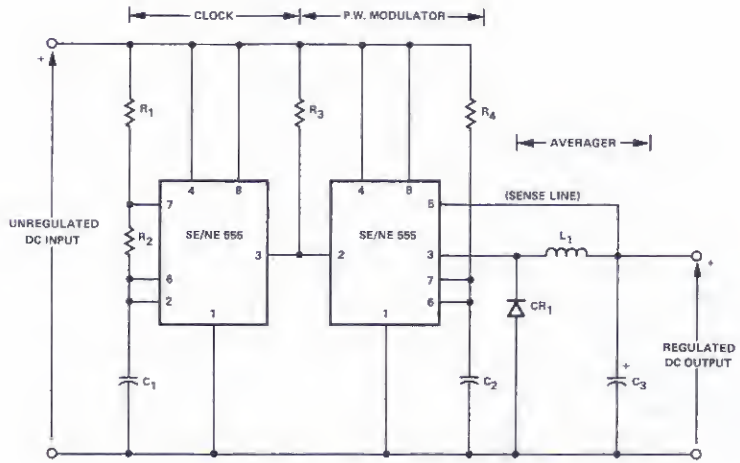


AUTO BURGLAR ALARM



APPLICATIONS (Cont'd)

SWITCHING STEP-DOWN REGULATOR



signetics

MOS
APPLICATIONS

7

MOS

INTRODUCTION

Each family of digital products that appears on the market brings with it a new set of system design rules and interface requirements. The different implementing technologies have individual combinations of features and characteristics that systems designers must take into account if they are to optimize their product designs. TTL, for example, is generally oriented for speed and drive capability. On the other hand, MOS offers high density and low power. Each has its appropriate place in a system logic design. A user who familiarizes himself with the dominant available technologies will be able to take advantage of the key features of each, and will be able to partition his system in the most economical manner.

This MOS User's Guide explores N-Channel and P-Channel silicon gate MOS technologies from several points of view. It is intended to acquaint the user with the basic MOS processing, with the trade-offs involved in the design of MOS integrated circuits, and with the resulting product characteristics. This helps to pin-point the areas of system circuitry where MOS can be used most effectively.

The Guide discusses the basic characteristics of internal MOS logic and circuit implementation. This knowledge enables the user to better understand many of the timing and control requirements necessary for proper operation of MOS products.

Knowing why it was made and how it operates, an additional requirement is to understand how the MOS device interfaces to the circuits that may surround it. Input and output circuitry is explained in detail and specific interface designs are discussed for each of several logic families.

The goal of the Guide is to provide the information necessary for a user to be able to fully optimize his use of MOS. This knowledge will allow the designer to make better trade-offs at the systems levels so that he can implement the best mix of technologies to accomplish his functions.

MOS PROCESS AND PRODUCT CHARACTERISTICS

MOS TECHNOLOGIES

There is a class of semiconductor devices known as Field Effect Transistors. The FET uses an electric field to control the flow of current through the transistor. FETs are divided into categories based on various methods of implementation. When FETs are formed using layers of Metal Oxide and Semiconductor material, the resulting transistors are called MOSFETs or MOS devices. Within the MOS category there are further differences of construction, and each provides a particular set of characteristics for the resulting circuits.

Figure 1 is a simplified diagram of the cross-section of a MOSFET. The source and drain regions are diffused into the substrate. The gate dielectric isolates the gate from the substrate, but is thin enough to allow the field of the gate to influence the current flow between the source and drain.

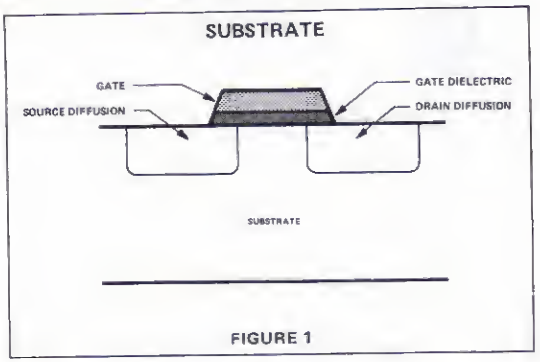


FIGURE 1

Early MOS products used "metal gate" techniques where the gate is made of aluminum. Many metal gate products are still being manufactured. One variation that has been used with metal gate is a different crystal orientation to provide better TTL compatibility. Ion implanted or nitride variations offer other combinations of characteristics.

Silicon gate technology uses a conducting form of silicon as the gate material instead of metal. It also allows the gate to be formed before the source and drain are diffused so that the structure can be "self-aligned." Silicon gate processing offers several important advantages over other techniques:

1. Lower threshold voltage, due to the physics of the gate material. This allows 1-1-1 crystal to be used, yet still retains TTL compatibility.
2. Higher gain, due to the greater current carrier mobility in the 1-1-1 crystal.
3. Lower power, due to the lower gate capacitance of the self-aligned structure and the lower supply voltages allowed by the lower threshold.
4. Higher speed, due to the lower threshold, higher gain and lower gate capacitance.
5. Higher density, due to lack of alignment tolerance needed with the self-alignment and the use of the gate material as an extra partial layer of interconnect.
6. Reliable plastic packaging, due to the several protective layers between the gate and the packaging material.

All new MOS designs at Signetics have used silicon gate since 1970.

Figure 2 shows a cross-section of a typical silicon gate device.

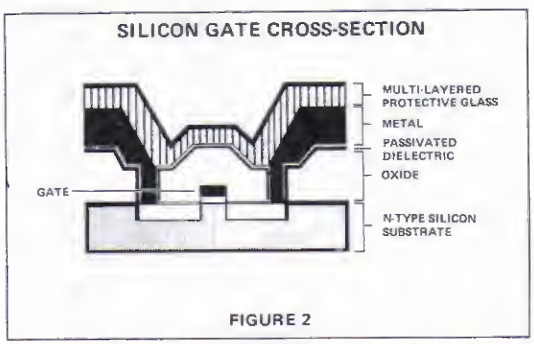


FIGURE 2

Another technology variation concerns the polarity of the conducting path ("channel") between the source and drain in the MOS transistor. P-Channel used P-type silicon for the source and drain diffusions and requires negative voltages with respect to the substrate to control the current through the positive polarity channel. N-Channel uses n-type silicon and positive voltages. P-channel has historically dominated product designs because the cleanliness constraints are less demanding than for N-channel, thus making the processing somewhat easier. As the manufacturing problems have been solved, N-channel has become an increasingly important factor in new MOS product designs. Because of the physics of the devices, N-channel offers several key advantages. The current carriers in N-channel are electrons instead of holes as in P-channel. The greater mobility of electrons means that the same size transistor is faster or the same speed transistor is smaller in N-channel. Lower thresholds and lower supply voltages are also possible with N-channel. It is even practical to use a single standard +5 volt supply on some products for the ultimate in TTL compatibility. Signetics has been building standard N-channel silicon gate products since mid-1972.

CMOS (complementary MOS) is a technology that combines both P-channel and N-channel devices on the same chip. Its key advantage is extremely low power, but it gives up quite a bit of density in exchange. The product philosophy and design trade-offs for CMOS are substantially different than for other technologies, and will not be discussed in this guide.

Figure 3 shows some relative comparisons of several MOS technologies for several characteristics. The cumulative figures serve only as a rough guide since they do not take into account quantitative differences.

MOS PROCESS COMPARISON

MOS TECHNOLOGY	SPEED	AREA	POWER	TTL LOGIC LEVELS	EASE OF PROCESSING	TOTAL
P-Channel Metal Gate						
(1,1,1) Crystal	7	3	5	3	1	19
(1,0,0) Crystal	8	3	3	2	1	17
Ion Implanted	5	4	4	3	3	19
MNOS (Nitride Process)	6	4	3	2	4	19
P-Channel Silicon Gate	4	2	3	1	4	14
N-Channel Metal Gate	3	3	3	2	3	14
N-Channel Silicon Gate	2	1	2	1	4	10
CMOS Metal Gate	1	5	1	1	4	12

FIGURE 3

The technologies that will dominate the future of MOS will be those that strengthen as much as possible those key characteristics that make MOS attractive.

MOS MEMORIES

To form a complete MOS integrated circuit, many of the individual MOS transistors are interconnected on a small rectangle ("chip") of silicon. Since MOS transistors are very small compared to transistors in other technologies, and since they can be designed to consume very little power, the two key advantages of the resulting MOS circuits are high density and low power. These key characteristics work hand-in-hand and they form the primary motivation behind the choices of products most suitable for implementation in MOS. Good density and power relationships are achieved not only because of the nature of the basic MOS transistor itself, but also because of the circuit configurations that are possible with MOS. The trade-off on the negative side is that in order to gain the density and power advantages, it is generally necessary to give up speed and drive capability.

The most effective MOS products are those that take the greatest advantage of the high density and lower power possible with MOS technology. This, in turn, implies that functions with regularly patterned circuitry will be the most successful. Randomly oriented circuits, with much of the chip area devoted to metal interconnect, tend to counteract instead of augment the basic density advantages of MOS. Patterned circuits can devote a much larger percentage of this area to active devices.

The reason that MOS memory products are so popular is that they can take full advantage of the dense circuit potential offered by MOS. The vast majority of the area of a memory chip can be allotted to the matrix of circuits that store the individual bits of information. This storage array is highly regular and can be designed to be extremely compact. A very high level of complexity can be obtained without a proportional increase in interface pins required for access to the memory. Shift registers are particularly attractive from the point of view of the circuit-to-pins ratio, since there can be simply one data input, one data output, and a clock. Further, shift registers do not usually require complex on-chip supporting logic for their operation. Read-only and read/write random access memories trade a slightly increased complexity of support logic (decoders, etc.) for their random access capability, with a resulting increase in system performance for many applications.

In order to make the most advantageous use of the characteristics of MOS technology, the Signetics line of MOS products is oriented toward memories in all their variations. Present day memory products may be divided into two general functional classes based on their methods of data retrieval: serial access or random access. Other methods are possible—such as orthogonally addressable or content addressable modes—but the primary thrust of general purpose semiconductor memories has been and will continue to be in serial and random access devices.

Serial access memories are shift registers that write data sequentially into a string of serially connected storage cells. As each new bit of information is inserted into the string, the previously entered data are all shifted forward into the next adjacent cells. The last cell in the string is the output and the data leave the shift register in the same sequence they were entered. Individual bits of information are not associated with particular storage locations. The data format is implicit in the nature of the part: the output data sequence is the same as the input data sequence. Random access memories, on the other hand, allow the user to explicitly address any particular physical storage location within the memory, and to do so in any desired order or sequence. A particular information bit is always associated with a particular physical location in the memory, and any location may be directly addressed.

Both types of memories make excellent use of the density of MOS. The trade-offs between the two depend on the system problems to be solved. Serial memories require very few interface signals and very little support circuitry on the chip. In system situations where serial data is stored, or in low speed cases where the relatively long average time to access any random bit is unimportant, shift registers can provide excellent system economy. Random access memories require a few more interface signals—primarily to handle the address inputs—and somewhat more on-chip support circuits to decode the addresses and make any addressed cell available. In system situations where fast, non-serial storage is required, MOS random access memories can provide excellent system economy.

Within the serial memory classification there are two further categories that define the type of storage cell used to implement the shift register: dynamic and static. Signetics' dynamic registers use fewer devices for data storage and offer higher speed, but they require two-phase, higher voltage clocks and must always be shifted at some minimum rate in order to maintain the validity of the stored data. Signetics' static registers use one more device per cell and run at lower maximum speeds, but they need only a single phase TTL-level clock and have no restriction on minimum operating frequency. As usual, the choice of which register to use is indicated by the nature of the system requirements.

Random access memories can be divided into read/write and read-only categories. Read-only random access memories have a non-volatile, predetermined data pattern stored in the cell array that cannot normally be changed. They can have a greatly simplified cell and support structure so that their bit density is often as much as 8 times that of a comparable read/write random access chip. There are several variations on the basic read-only concept. Generally, the mask programmed versions offer the lowest potential cost per bit. There are also read-mostly types that may be electrically modified, erasable types that may be reprogrammed, and write-once types that are field programmed only once. Signetics' MOS read-only random access memories are all of the mask programmed variety. This provides the greatest density optimization and keeps the per bit costs very low for moderate and high volume applications.

Read/Write random access memories are further subdivided into dynamic and static categories. The original semiconductor R/W RAMs were static and consisted simply of several standard flip-flop circuits tied together. Dynamic cells were then used to improve the storage density. The dynamic versions usually require clock drivers and sense amplifiers and must be periodically refreshed. The new static memories are fully TTL compatible and have no clock or refreshing requirements, but they are less dense than their dynamic counterparts.

MOS LOGIC CHARACTERISTICS

MOS DEVICES

The basic silicon gate MOS transistor is shown in cross-section in Figure 4 along with the circuit symbols commonly used. There are two modes of operation for field effect devices: enhancement and depletion. The devices shown in the figure are enhancement mode devices that are non-conducting with zero volts applied to the gate. A conducting channel is created—enhanced—by the electrostatic field associated with the voltage applied between the gate and source terminals. For the P-channel enhancement mode device in Figure 4a, negative voltages applied to the gate with respect to the source are used to establish a conducting channel between the source and drain at the interface between the gate dielectric and the substrate. Conversely, N-channel enhancement mode devices (Figure 4b) require a positive gate-to-source voltage for conduction between the drain and source. Depletion mode devices are normally conducting with zero volts applied to the gate and require the application of an appropriate gate-to-source voltage to "deplete" the conducting channel in order to turn them off. The majority of present MOS circuit designs use enhancement mode devices.

The operation of MOS transistors differs substantially from that of bipolar devices. The term "bipolar" refers to the two polarities of carriers that exist in these transistors. Both holes and electrons are essential to their operation. Conversely, MOS devices are "unipolar" since only one type of carrier is used in the operation of a particular transistor. For P-channel MOS, the carriers are holes while electrons are the carriers for N-channel MOS. Another distinction arises from the differing locations for the active regions for the two types of transistors. Bipolar devices are "bulk" devices. The active region is located several microns beneath

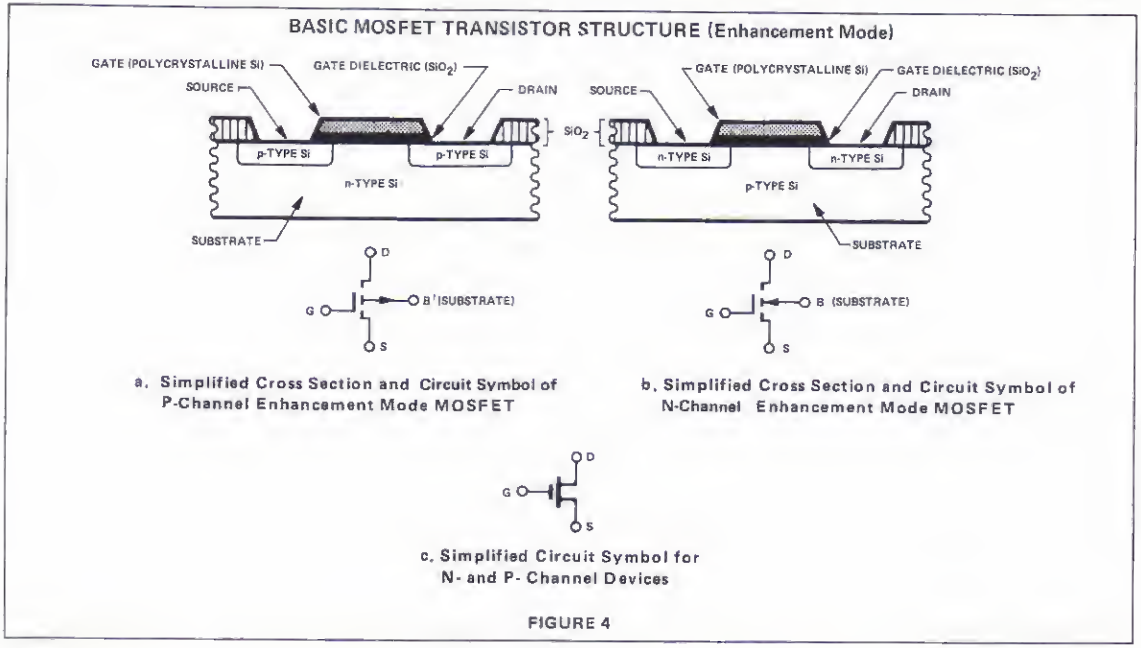


FIGURE 4

the surface in the base region between the emitter and collector. MOS transistors, on the other hand, are surface effect devices. Their active region consists of an induced channel (for enhancement mode operation) located at the silicon-silicon dioxide interface.

Since the MOS transistor is a field effect device, the gate is isolated electrically from any other part of the transistor. As a result, the input dc impedance, using the gate as the input, is extremely high—on the order of 10^{14} ohms. This high dc impedance characteristic to a large extent determines the nature of the MOS input interface.

Figure 5 shows the characteristic V-I behavior of MOS enhancement mode transistors. The output characteristic curves (Figure 5a) depict the drain current as a function of drain-to-source voltage with the gate-to-source voltage as a running parameter. The two areas of interest are separated by the dotted line. When the device operates in the region labelled non-saturated, its V-I characteristic is approximately resistive. The term "non-saturated" means that the device is not conducting as much drain current as possible for a given gate-to-source voltage. The device behaves like a current source or sink when operated in the saturated region of the curves. In this area the drain current is no longer a function of the drain-to-source voltage. Note that the larger the gate-to-source voltage, the larger the saturation current becomes.

The input transfer curve (Figure 5b) shows the drain current as a function of gate-to-source voltage with drain-to-source voltage as a running parameter. Notice that the device is "off" ($I_D = 0$) until $V_{GS} \geq V_T$. Low threshold MOS processes such as silicon gate allow MOS logic to be compatible with standard T^{2}L and other common bipolar logic families whose switching thresholds are about 1.5

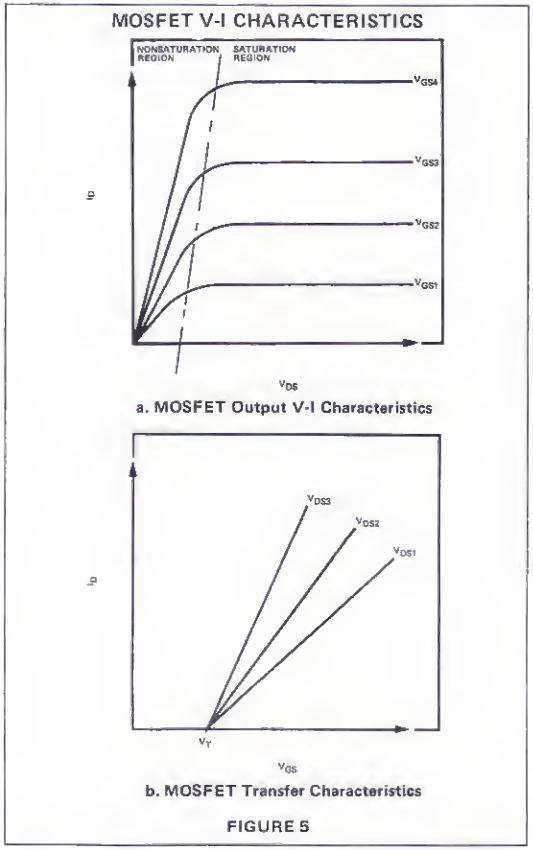


FIGURE 5

volts. For p-channel silicon gate devices V_T is nominally 2 volts while for n-channel silicon gate devices V_T is 1 volt. The variation of threshold voltage with junction temperature is shown in Figure 6. Clearly, the threshold voltage is not very sensitive to temperature variations.

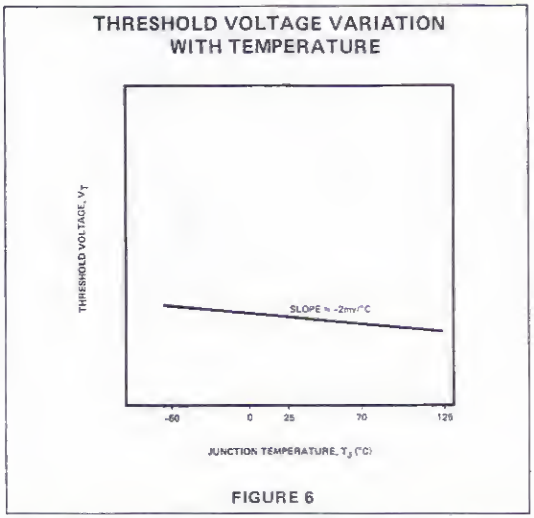


FIGURE 6

The slope of the input transfer curves is the transconductance, g_m. This parameter can be used as a gain figure or transfer function for the MOS transistor since it governs the output current a device can conduct for a given input voltage. Transconductance varies with junction temperature in the manner shown in Figure 7. Notice that g_m decreases with rising junction temperature while current gain (β or h_{FE}) in bipolar devices increases with rising temperature. Some of the implications of this phenomenon, such as the worst-case temperature condition for power dissipation, speed, and output drive capability, are discussed in later sections.

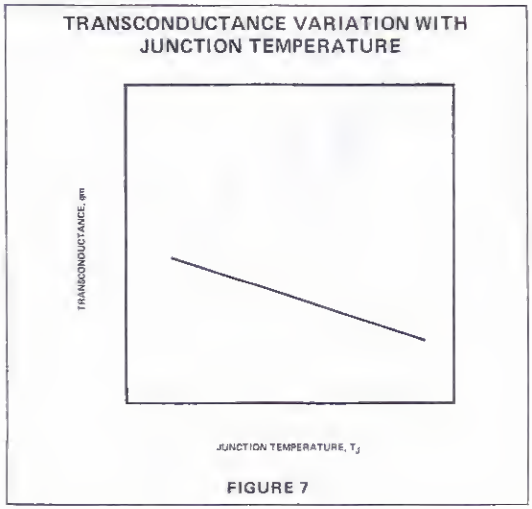


FIGURE 7

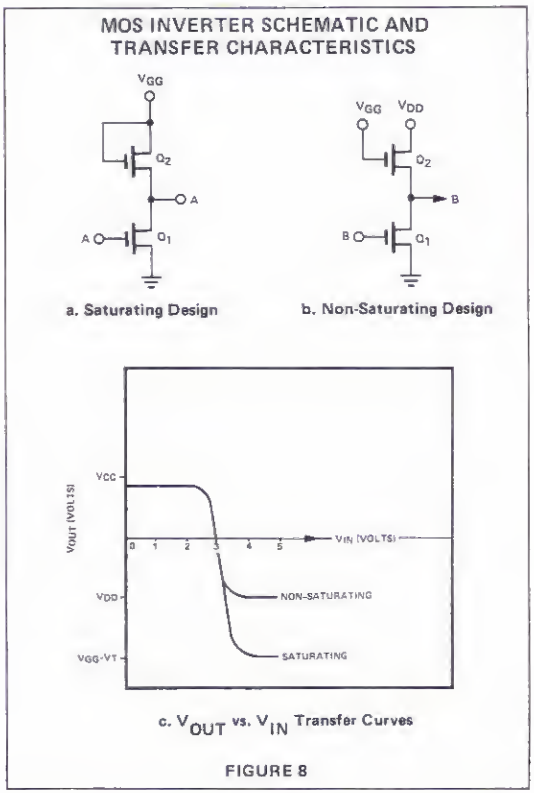
MOS LOGIC IMPLEMENTATION

Figure 8 illustrates how p-channel MOS transistors are used to implement the NOT logic function. The upper transistor in each inverter is used solely as a load resistor, taking advantage of the device's transconductance to construct a large value resistor in a relatively small area. On the chip, resistors are made of relatively low resistivity materials and tend to take up considerable space. This tendency is especially crippling in MOS designs since large value resistors are needed to keep the power consumed in complex functions at a minimum. By choosing an appropriate gate voltage for an MOS device, the designer can make a high value load resistor in a small space since the channel resistivity is governed by the gate voltage.

The difference between the structures shown in Figures 8a and 8b lies in the mode of operation of the load devices. Because $|V_{GS}| \leq |V_{DS} + V_T|$, the load resistor in Figure 8a is saturated and behaves like a current source. The voltage across a load capacitance attached to the output of an inverter that is switching varies with time and has a slope of:

$$\frac{dv}{dt} = i_{SAT}/C_{LOAD} \qquad (1)$$

where i_{SAT} is the saturation current of the load resistor for a given gate-to-source voltage. Note that as the voltage at



a. Saturating Design

b. Non-Saturating Design

c. V_{OUT} vs. V_{IN} Transfer Curves

FIGURE 8

the inverter output swings toward V_{GG}, the gate-to-source voltage of the load resistor is decreasing. Thus, the internal resistance of the load resistor is increasing with time.

The load resistor for the inverter in Figure 8b is non-saturated and behaves like a resistor. The value of this resistor increases as the inverter output voltage swings toward V_{DD}. This "ON" resistance does not vary as much with changing source terminal voltage as it does for the saturated inverter. As a result, the time delay through the non-saturating inverter is shorter than through a saturating inverter of similar size. The primary advantage of the saturating design lies in the saving of a power supply since the non-saturating design requires three voltages. The V_{OUT} vs. V_{IN} transfer curves for an MOS inverter are shown in Figure 8c. The level that the output reaches when the input is at 0 volts is determined by the ratio of the "ON" resistances of Q_1 and Q_2 as indicated by equation (2) for saturating inverters.

$$V_{OUT(HI)} = V_{GG} + (V_{CC} - V_{GG}) \left(\frac{R_{ON(Q_2)}}{R_{ON(Q_1)} + R_{ON(Q_2)}} \right). \quad (2)$$

The same resistance ratio affects the non-saturating inverter output "HI" level. In that case, however, V_{DD} is substituted for V_{GG} in equation (2).

The Boolean NOR function whose truth table is shown in Figure 9a is implemented in MOS circuitry as shown in Figure 9b and 9c. The polarity of the threshold voltage determines whether a series or a parallel structure is used. For p-channel MOS, which lends itself to negative logic conventions, the positive logic NOR gate circuitry utilizes a cascode or series structure.

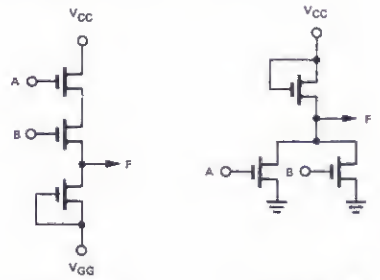
The MOS circuitry used to perform the NAND function is shown in Figures 10b and 10c. Again, the device's threshold voltage polarity determines whether a parallel structure or a series structure is used to perform the function. The parallel structure used in p-channel MOS logic circuits also performs the NOR function in negative logic.

BOOLEAN NOR FUNCTION TRUTH TABLE

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

"1" = MOST POSITIVE VOLTAGE
"0" = MOST NEGATIVE VOLTAGE

a.



b. p-Channel MOS Implementation

c. n-Channel MOS Implementation

FIGURE 9

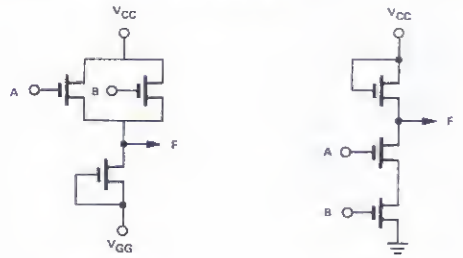
BOOLEAN NAND FUNCTION TRUTH TABLE

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

"1" = MOST POSITIVE VOLTAGE
"0" = MOST NEGATIVE VOLTAGE

a.

MOS NAND IMPLEMENTATION



b. p-Channel MOS Implementation

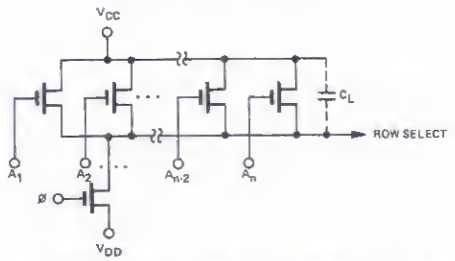
c. n-Channel MOS Implementation

FIGURE 10

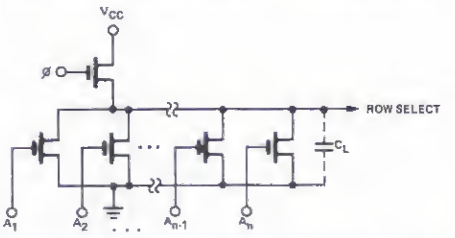
The same logic functions can be accomplished with dynamic circuit structures like those shown in Figures 11a and 11b. This technique involves precharging load capacitor C_L during the clock, $\emptyset$, pulse duration. Then C_L is either left charged or is discharged, depending on the input states, after the clock turns off and isolates C_L from the power supply. This circuit is very useful because it dissipates less power than corresponding static logic gates. Address decoders for random access memories often use this technique.

Implementing combinational logic on LSI chips using MOS circuit technology offers space-saving advantages over bipolar approaches. These advantages arise from several factors. For example, the high dc input impedance of MOS circuits allows simpler connection of logic gates. Also, MOS

MOS DYNAMIC LOGIC



a. Dynamic NOR Gate Decoder in n-Channel MOS Logic



b. Dynamic NAND Gate Decoder in p-Channel MOS Logic

FIGURE 11

processing permits highly dense packing of devices since an isolation diffusion is not required between adjacent transistors. In addition, the MOS devices themselves are inherently smaller than their bipolar counterparts, since they do not require diffusions within diffusions.

Standard TTL is very efficient in performing NAND logic since extra logic inputs slightly increase the input transistor's size but do not add to the device count. In p-channel MOS, the NAND function requires the addition of one relatively small device for each added logic input. In performing the NOR function, TTL circuits require the addition of two devices per added logic input: an input structure and a phase-splitter. P-channel MOS, on the other hand, requires only one added device for each additional input. Of course, there are constraints placed on the number of MOS devices that can be connected in cascode or "stacked up." These constraints arise from the resistance ratio required to drive the next logic stage. The same characteristics apply to n channel MOS logic except that the functions are reversed.

Memory is another essential logic function. A straightforward way to implement the memory function is to use the bistable multivibrator or "flip-flop." The MOS version of a simple R-S flip-flop is shown in Figure 12. This particular circuit uses p-channel MOS devices and consists of two cross-coupled inverters. Outside access to this memory "cell" is accomplished through Q_1 and Q_4. The logic "1" (most positive voltage) level is determined by the "ON" resistance ratio of Q_1 and either Q_2 or Q_3 depending on the state of the cell. The logic "0" level is $-V + |V_T|$. This circuit is used in static MOS read/write random access

STATIC RAM CELL (4-1/2 Interconnects)

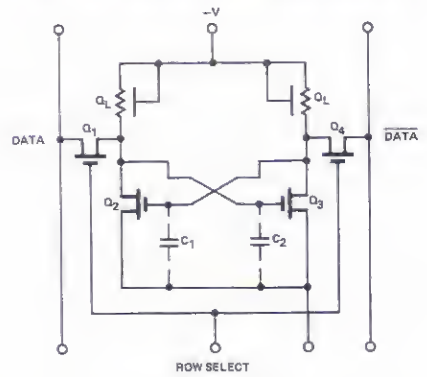


FIGURE 12

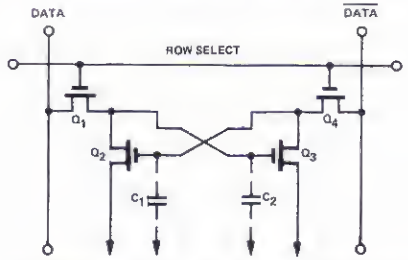
memories. A static memory will hold data as long as power is applied so that refreshing data is not necessary. The n-channel circuit is the same except that the power supply polarity is positive rather than negative. To make a memory matrix from these cells, the designer arranges them into an array such that an addressed cell is connected to a pair of lines called "sense" lines. Then, assuming a read cycle is required, the information stored in the selected cell is placed on the DATA and $\overline{DATA}$ lines and sensed by the output circuitry. If a write cycle is required the DATA and $\overline{DATA}$ lines are forced to the appropriate states, and the selected cell is set accordingly. This cell design requires 6 devices and 4½ interconnections.

The high impedance input that MOS inverters provide permits the use of dynamic memory cell designs. Figure 13 shows the evolution of dynamic MOS read/write RAM cells. The dynamic cell differs from the static cell in that charge is stored on a parasitic capacitance and periodically refreshed to compensate for the small but non-zero leakage current at the storage nodes, rather than continuously refreshed through load resistors.

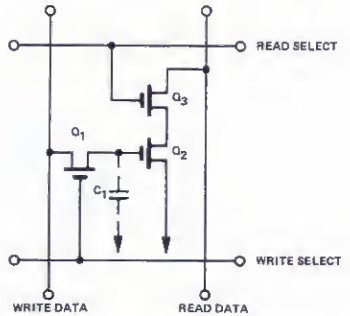
Two factors affect the cell size of the memory circuit. One is the number of transistors used to implement the memory function, and the other is the number of interconnect lines needed to connect the cells to the rest of the circuitry. The cell in Figure 13a is identical to the static cell described earlier, except that the dc load devices have been removed. As a result, the cell has two less transistors and one less interconnect and is correspondingly smaller. The substrate connection is counted as one-half interconnect. This dynamic cell maintains the differential data sense feature offered by the static cell.

A simpler dynamic cell (Figure 13b) has one less transistor and one more interconnect. This is the cell used for the 1103 type of 1024-bit dynamic RAM that appeared on the market in 1970. One interconnect can be eliminated by making the READ DATA and WRITE DATA lines common as in Figure 13c. In this configuration, each access of a cell inverts the polarity of the data on that cell's entire column

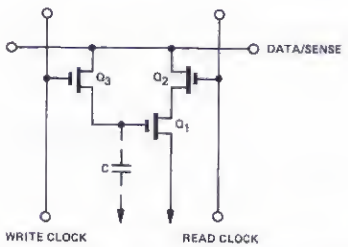
DYNAMIC RAM CELL EVOLUTION



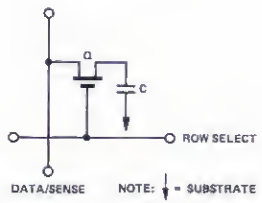
a. 4-Transistor Dynamic Cell With 3-1/2 Interconnects



b. 3-Transistor Dynamic Cell With 4-1/2 Interconnects



c. 3-Transistor Dynamic Cell With 3-1/2 Interconnects



d. 1-Transistor Dynamic Cell

FIGURE 13

necessitating some method for keeping track of the data polarity for that column. This cell approach allows higher levels of density since it uses one less interconnect line.

Larger MOS read/write memories are being designed demanding still greater levels of cell density. One approach is the single-transistor cell shown in Figure 13d. This cell uses a storage capacitor that is isolated from the data/sense line by a series transfer device which is controlled by the ROW SELECT line. This dynamic cell has only 2½ interconnects.

The previous section has shown how MOS circuits can be used to perform the memory or data storage function for random access read/write memories. MOS devices can also be used for serial access memory or shift register functions. The basic dynamic shift register cell of Figure 14 uses two MOS inverters coupled together with transfer devices to isolate one cell half from the other during shifting so that data entering the cell will not interfere with data leaving the cell. The clock waveforms are also shown in Figure 14. The high-voltage clocks are necessary to minimize the size of the transfer and clocked load devices because the larger the clock swing is, the smaller the geometry needed to obtain a given "ON" resistance. The maximum voltage that C_1 or C_2 can be charged to is either $V_{CLOCK} - 2V_T$ or V_{DD}, whichever is least. Thus, by operating the load and transfer devices in a non-saturated mode ($|V_{CLOCK}| > |V_{DD} + 2V_T|$), the voltage on C_1 or C_2 can be maximized without dissipating excessive power. During the time $\emptyset_{IN}$ is low, data stored on capacitor C_1 is transferred to capacitor C_2 through Q_3. During the time $\emptyset_{OUT}$ is low, data is transferred to the output structure through Q_6. Thus, data is shifted from one cell to the next with each pair of clock pulses, i.e., a $\emptyset_{IN}$ pulse followed by a $\emptyset_{OUT}$ pulse. Since the load devices Q_2 and Q_5 are turned on and off by the clocks, dc current does not flow between V_{DD} and the substrate except when a clock is low. Consequently, the power consumed varies with the duty cycle of the clocks.

DYNAMIC SHIFT REGISTER CELL AND CLOCK WAVEFORMS

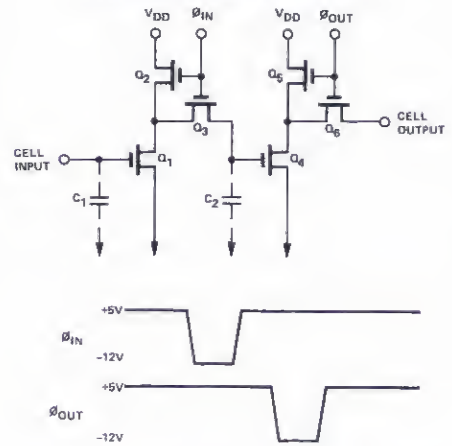


FIGURE 14

The use of dynamic logic for serial memory applications necessitates refreshing to prevent loss of data from C_1 or C_2 just as in dynamic random access memories. Here, refreshing is accomplished by shifting, and a minimum clock frequency constraint is placed on the use of the device. If the dynamic shift register cell is not shifted at some minimum clock rate, the charge stored on C_1 or C_2 will leak away, and the cell will "forget" the data it was storing.

A more complex cell is required to perform the static shift register function. The circuit diagram and clock waveforms are shown in Figure 15. The cell consists of two inverters in cascade with feedback to accomplish the latching function. The feedback path is gated with serial transfer device Q_5 and the feed-forward path is gated by Q_3. These gates isolate each half cell from the other. Placing the level shifting and clock generating circuitry on the chip eliminates the need for external multi-phase high-voltage clocks. The single TTL-level clock then becomes a logic signal input. When the clock input is in the active state (either high or low, depending on the particular device), $\emptyset_1$ is LO ($\approx -12V$), and data is transferred through Q_1 to C_1 either from the output of the previous cell or the data input buffers. During this time $\emptyset_2$ and $\emptyset_3$ are HI ($\approx +5V$), and C_2 is isolated from the input of the cell. When the clock input returns to the inactive state, $\emptyset_1$ goes HI, $\emptyset_2$ goes LO immediately, and $\emptyset_3$ begins to fall. C_1 is now isolated from the cell input, and the data is transferred to C_2. At this point, the cell has gone through a full clock cycle and data has successfully been shifted from the cell input to the cell output. Note that so far the cell has behaved in the same manner as a dynamic shift register cell except that the load devices, labeled Q_L, are not clocked but rather are always conducting.

The static feedback path through Q_5 gated by $\emptyset_3$ is enabled only at relatively low frequencies since about a 5μsec interval is needed to drive $\emptyset_3$ LO. If $\emptyset_3$ went LO as quickly as $\emptyset_2$, the cell would not have time to "flip" and would be bypassed through Q_5. Since O_3 is on only during the inactive clock state, it follows that the device will not retain data in the static state if the input clock signal is stopped in the active state. This operational feature is reflected in the constraint placed on the maximum clock pulse width. Conversely, when $\emptyset_3$ does latch up the cell, data is retained without refreshing (clocking) as long as power is applied.

MOS integrated circuits are also very useful in implementing the read-only memory (ROM) function. A typical MOS ROM cell is shown in Figure 16. If a positive logic "1" is to be stored in a particular cell, holes are cut in the source-drain diffusion mask for transistor Q_1 at the location of that cell. Conversely, if a logic "0" is desired, no holes are cut for Q_1 in that cell. Then, to gain access to a given cell, the appropriate row and column are selected through the address decoders, and the bit line is pulled up to the substrate voltage through Q_1 if a gate is mask programmed to be present for Q_1. If not, the bit line voltage is pulled down to V_{GG} through the load device Q_3. The resulting level is sensed, buffered, and presented to the appropriate output.

Although the data in a ROM cell matrix is non-volatile—the presence or absence of a device is independent of supply voltages—some of the peripheral logic on a ROM chip can be dynamic. For example, to save power in large ROMs, the designer might use dynamic address decoders and require

STATIC SHIFT REGISTER CELL AND CLOCK WAVEFORMS

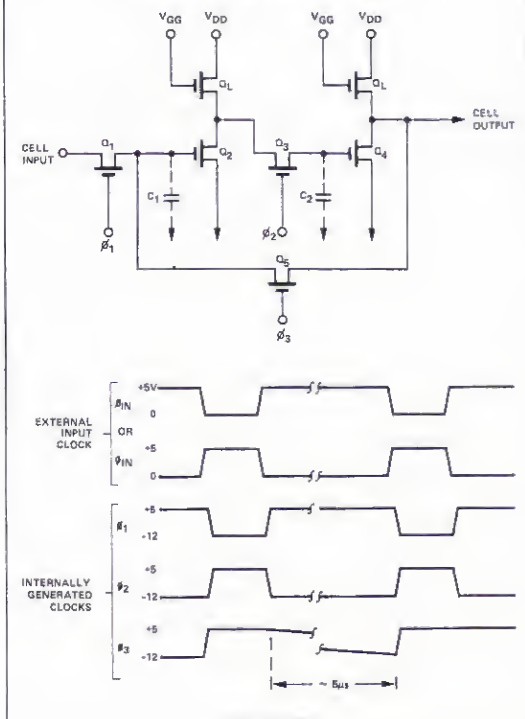


FIGURE 15

READ-ONLY MEMORY CIRCUIT STRUCTURE

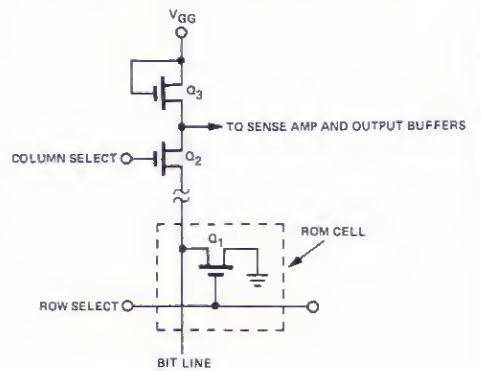


FIGURE 16

DYNAMIC ROM BLOCK DIAGRAM AND CLOCK WAVEFORMS

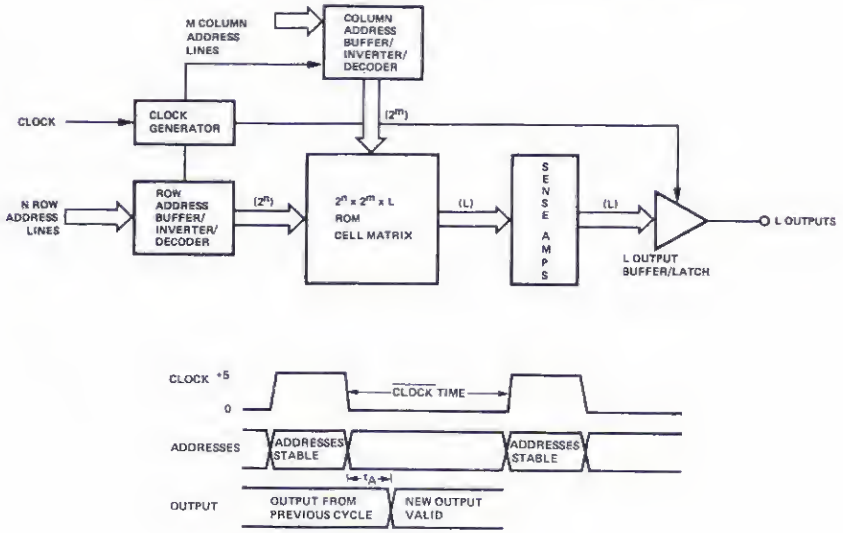
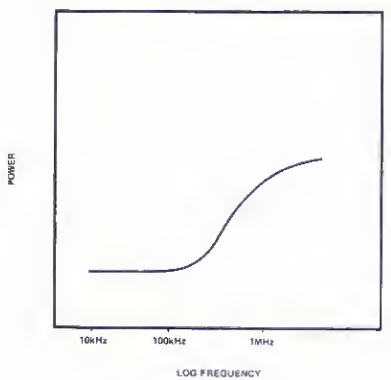


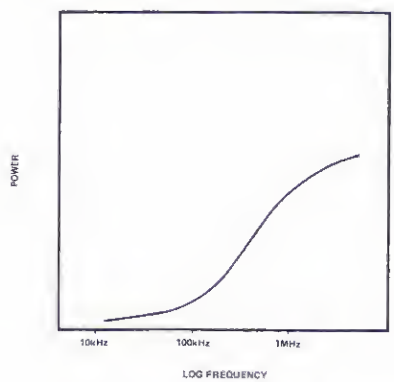
FIGURE 17

the user to supply a logic signal that is used as a clock. In such cases, the product is called a dynamic ROM, even though the stored data is not dynamic. The levels on the address lines are clocked into the decoders, and data is clocked into an output latch. The block diagram and timing requirements for such a ROM are shown in Figure 17. During CLOCK time, the decoder lines (ROW and COLUMN SELECT) are precharged to a negative level. When CLOCK goes high, the address lines are decoded, and data is presented to the output latch. On the trailing edge of CLOCK, the data is strobed into the output latch and presented to the output after an interval t_A has elapsed. The output remains present as long as the chip is enabled or until the next clock cycle. The block diagram shown in the figure is also applicable to static ROMs with the exception of the clock generator circuitry. The static ROM presents outputs one access time after all the address lines become stable in each data cycle.

SHIFT REGISTER POWER vs. FREQUENCY CHARACTERISTICS



a. Static Shift Register Power vs. Frequency



b. Dynamic Shift Register Power vs. Frequency

FIGURE 18

Due to the nature of dynamic logic, some special system considerations arise from designing memories with dynamic MOS circuits. Two of these, variation of power with frequency and the need to periodically refresh data, have already been mentioned. Figure 18 shows a comparison of the average power vs. frequency characteristics for static and dynamic shift registers. Notice that above about 100KHz the two curves have similar shapes. This behavior is consistent with the similarity of operation between the dynamic shift register cell and the static shift register cell at frequencies above where the slower feedback path can function. The steepest slope occurs between 100KHz and 1MHz. In this range, capacitor charging current is the predominant power component. The inflection point that occurs within this range on both curves is due to the decrease in g_m as junction temperatures rise with increased power dissipation. The resulting higher on-chip resistances tend to reduce the slope of the power vs. frequency curves for both static and dynamic shift registers. Below this range, the primary power factor for static shift registers is the dc power drawn by the memory cells. For dynamic shift registers, the dominant factor is leakage current.

Although the circuits are configured differentially, the same mechanisms affect other static and dynamic memory circuits. In general, dynamic memories draw large currents during short intervals at some point in their cycle. The resulting current spikes create system noise problems which must be considered in the system design. Some typical current waveforms are shown in Figure 19 for a 2048x1 MOS RAM. Note the large I_{DD} current drawn at the leading edge of $Clock_1$. This current spike corresponds to the precharging of address decoder lines which represent a large capacitive load that is effectively switched onto the V_{DD} line by the leading edge of $Clock_1$. Static logic circuits, on the other hand, do not require large transient currents. They dissipate a more constant power although they tend to consume more average power per function at low speeds.

MOS I/O CHARACTERISTICS

As MOS integrated circuits become widely used to implement complex logic functions, designers will pay more attention to the unique characteristics of this relatively new technology. One area of concern is the interface between MOS devices and other technologies.

Pioneer MOS complex logic products were high threshold voltage devices. Their switching threshold voltage was incompatible with the more common logic elements such as Diode-Transistor Logic (DTL) or Transistor-Transistor Logic (TTL). This voltage discrepancy hindered the practical use of these original MOS parts because of the need for intervening voltage level translating devices. The advent of low threshold MOS technologies drastically simplified the use of MOS devices in implementing LSI (large-scale integration) functions. This section describes the input, output, and power characteristics of silicon gate MOS integrated circuits and will aid the user in defining the interface needed to operate these devices in systems with other logic families.

INPUTS

The input structure presented in Figure 20 is a typical p-channel input inverter/buffer. It is representative of data, clock, and control line inputs for both static and dynamic logic. As shown by the figure, it consists of a series diffused resistor whose nominal value is 2K ohms (for clocks, this resistor is around 100 to 200 ohms), the associated

TYPICAL CURRENT TRANSIENTS

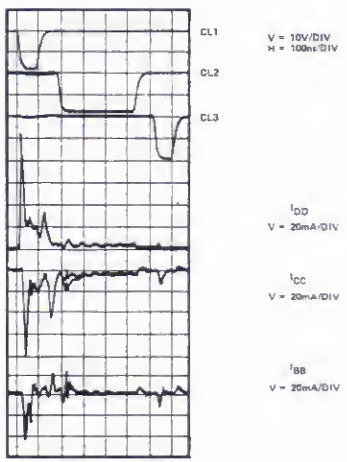
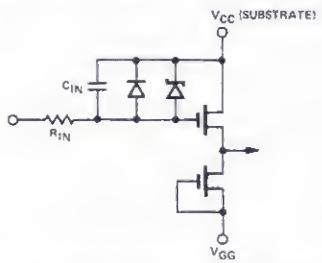
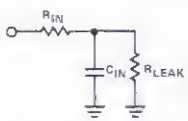


FIGURE 19

MOS INPUT EQUIVALENT CIRCUIT



a. Typical p-Channel Si Gate MOS Input Structure



b. Equivalent Circuit

FIGURE 20

substrate diode, a distributed junction and gate-to-source overlap capacitance, a high threshold field-turn-on MOS transistor (modelled here as a zener diode), and the gate of the input inverter transistor.

Due to their high dc input impedance, MOS integrated circuit inputs are susceptible to damage caused by static charge accumulation. Early MOS metal-gate devices were very easily damaged since their designs made little or no provision for dissipating this excess static charge. As a result, charge accumulated until the gate-to-source breakdown potential (~120 volts) was reached, and the gate oxide catastrophically broke down. The requisite amount of static charge could be obtained from simple free-air contact with an open input. Thus, a device could be permanently damaged by merely leaving it on a workbench. A good deal of effort has been devoted to making present silicon gate MOS devices immune to static damage. Reasonable care must still be exercised in handling these circuits, but the problem has been drastically reduced.

The purpose of the resistor, capacitor, substrate diode, and field-turn-on transistor shown in Figure 20a is to protect the gate of the input transistor from damage due to static charge accumulation. The field-turn-on device is activated if the input voltage exceeds $V_{SS}{}^{-24}$ volts where V_{SS} is the substrate voltage. Thus, the accumulated charge is drained off to the substrate long before the gate can be damaged. The 2K ohm resistor and the distributed capacitor (about 5pF) are used to slow down fast rising transient voltage spikes so that the high threshold device has sufficient time to turn on and dissipate the associated excess charge. The substrate diode clamps the input to prevent any positive-going static voltage excursions in excess of V_{SS} + 0.7 volts.

Possible problem areas in handling silicon-gate circuits include:

- *soldering pins with an unisolated soldering iron;
- *wearing silk smocks when handling MOS devices;
- *leaving MOS input pins unterminated on a printed circuit board.

Avoiding these problem areas helps insure that devices will not be damaged from static charge build-up. Soldering should be done in a properly grounded wave-soldering machine or with an isolated soldering iron.

Workers handling MOS devices or PC boards with unterminated MOS inputs should not wear silk smocks or work in a static-charge producing environment. Silk and other materials tend to pick up large amounts of static charge as the wearer moves around.

All MOS input pins should be terminated before traces connected to them leave the printed circuit board since an unterminated trace is equivalent to leaving the MOS input pin open, even though the MOS device is soldered to the board. Termination can be accomplished with a TTL buffer, a pull-up resistor to V_{CC}, or the output of another MOS device. Shipping PC boards with MOS inputs unterminated should be done with the same care exercised in shipping individual devices; that is, the traces at the edge connector of the PC board should all be shorted together. Unless these precautions are taken, plastic shipping containers should not be used for shipping parts or boards. MOS devices are shipped from the manufacturer in a low impedance environment such as conducting foam, shunts, or conducting tubes and should be stored by the user the same way.

A non-catastrophic failure mode that often occurs because pins are left open arises from the fact that input pins left floating on MOS devices are *not* at a logic "1" level as are open inputs for TTL circuits. Instead, floating MOS inputs are logically ambiguous. For example, control inputs such as $\overline{\text{RECIRCULATE}}$ for a shift register that are left open might cause a device to be in the wrong operating mode if sufficient charge is accumulated to reach the input switching threshold voltage. In this case, the device would not necessarily be damaged but would appear to malfunction. An input resistor is not required when terminating unused inputs.

Since the dc gate input impedance for MOS integrated circuits is characteristically very high, the input equivalent circuit can be derived from the behavior of the input protection network. This derivation assumes that the input voltage swing is restricted to the normal operating range of V_{CC} + 0.3 volts to V_{CC} − 18 volts. In this range, the substrate diode is reverse biased and the high threshold field turn-on device is inactive. Since these components consist of very clean p-n junctions, the leakage current each of them exhibits is very small. If these junctions are modelled as a large-value lumped resistance in parallel with the input capacitor, the equivalent circuit in Figure 20b results. Since R_{LEAK} is very large, it can be ignored in most input circuit analyses. The input, then, behaves like a series R-C network returned to the substrate. As a result, the output fanout (the number of MOS inputs that can be driven from one driver) is limited only by the rise and fall time constraints in the system because the resulting load impedance presented to a data or clock driver by multiple MOS chips is the parallel combination of series R-C networks which exhibit no dc component. The voltage requirements at the MOS inputs are of primary concern, since the device is voltage controlled. Figure 21 is a bar chart showing the input voltage requirements for both P- and N-channel integrated devices. The levels shown for P-channel devices assumes a V_{CC} of 5.00 volts. Since V_{CC} is the substrate reference voltage for P-channel devices, the input voltage requirements track variations in V_{CC}, e.g., $V_{IL(MAX)}$ = 0.80 volts for V_{CC} = 4.75 volts, and $V_{IL(MAX)}$ = 1.3 volts for V_{CC} = 5.25 volts. If the specification limits were restated with respect to V_{CC}, they would be $V_{IH(MIN)}$ = V_{CC} −1.8 volts and $V_{IL(MAX)}$ = V_{CC} −3.95 volts. Because the ground pin for N-channel devices is the substrate reference, the input voltage values specified include the V_{CC} variations, and the switching threshold is relatively unaffected by V_{CC} variations.

Several factors contribute to what could be called the "dynamic dilemma" which could be defined as the quandry that arises when, in order to take advantage of dynamic logic speed and low standby power, the designer must contend with the problems inherent in using dynamic logic. These factors include the need for high voltage clock

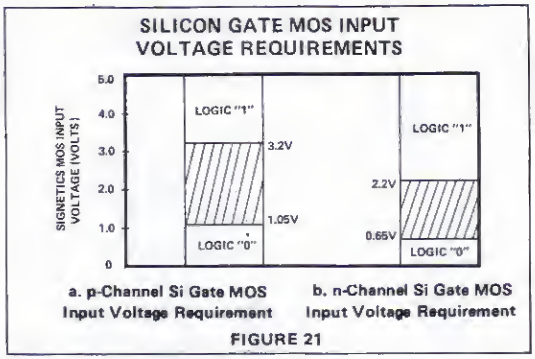


FIGURE 21

swings, large capacitive loads on the clock drivers, clock ringing problems, and inter-clock coupling problems. The first two factors imply that the clock driving circuitry, whether discrete or monolithic, must supply large amounts of power. The high voltage clock swings—typical swings are around 15 to 17 volts for p-channel silicon gate devices—contribute to the high power required due to the voltage-current product and due to the fact that the power required to charge and discharge a capacitive load varies with the square of the voltage swing. This charge/discharge power also varies directly with the capacitance of the load and the operating frequency.

Since the load presented by the clock inputs in an MOS dynamic system is reactive in nature with no dc load component, any parasitic series or parallel inductance tends to cause ringing on the clock edges. Because the P-channel MOS substrate is tied to V_{CC}, ringing during the clock transition from low to high can adversely affect the device. An example of this clock overshoot in dynamic shift registers is shown by the waveforms in Figure 22a. In general the isolation diodes on P-channel dynamic logic chips which are used to electrically isolate individual transistors will be forward-biased if any input, including the clocks, is more than 0.3 volts more positive than the substrate potential—in this case V_{CC}. In memory devices forward-biasing the substrate diode may cause sporadic loss of data. Since for N-channel devices the substrate is tied to ground, input undershoot rather than overshoot is critical.

Another noise problem becomes apparent when using multiple phase clocks in a dynamic logic system. Figure 22b shows an example of crosstalk or interclock coupling in a two-phase dynamic device. There are two factors that principally affect the crosstalk problem. The first involves the parasitic coupling capacitors that are distributed through-out the system on the monolithic clock driver circuit, on the printed circuit boards, in backplane wiring, and on the MOS integrated circuit itself due to the proximity of the two clock phases. This distributed capacitance couples the two clocks together whenever either of them changes levels. Careful system design and layout can significantly reduce crosstalk. Some practical design guidelines include:

1. Drive only one phase of a multiphase clock with any given monolithic clock driver package.

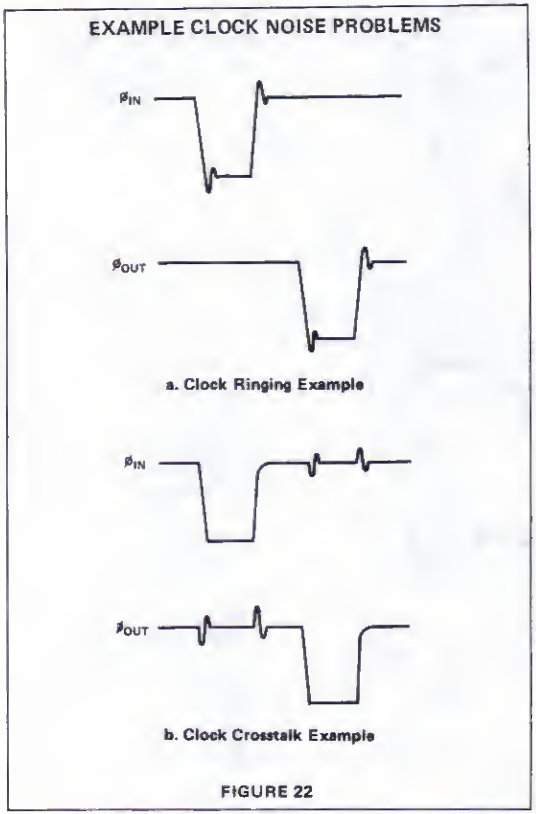


FIGURE 22

2. Do not run clock lines for different phases in close proximity.
3. Minimize the cross-over capacitance on the MOS integrated circuits.

Observing Rule 1 eliminates the clock coupling on the clock driver circuit because both ends of the coupling capacitor on the clock driver chip are driven by the same signal. Rule 2 helps minimize the stray capacitance coupling the clocks on the printed circuit. Of course, Rule 3 is observed by the MOS manufacturer and is not under the control of the system designer.

The second factor of interest is the impedance looking back into most monolithic clock drivers. When these drivers finish switching from low to high, the edge current source shuts off and exhibits high impedance behavior. As a result, the phase that is in the logic "1" state is noise-sensitive when the other phase switches. The differentiated waveform is superimposed on the quiescent (HI level) clock. If the negative-going spike is large enough, it becomes a "phantom" clock. If the positive-going portion of the spike is large enough, it can cause the isolation substrate diodes to be forward-biased, just as with rising clock edge overshoot.

Device manufacturers have made significant strides recently in desensitizing dynamic logic devices to positive-going clock noise. For example, the dynamic shift registers have

been redesigned so that clock overshoot cannot forward-bias the substrate diodes. Negative-going clock noise while the clock is high, however, is still a prevalent dynamic logic system problem. Experience shows that most user problems with typical dynamic shift registers can be traced to clock overshoot and crosstalk problems. A good, reliable serial memory system cannot be achieved without clean clock signals.

Memory devices utilizing static logic are generally less noise sensitive on the inputs than dynamic memories since all inputs are buffered before being used on the chip. As a result, the memory cells themselves are isolated from noise on input lines. In addition, the cells in static memories are latches and do not depend solely on stored charge for memory. Thus, a relatively large input noise spike is required to change the state of the cell. In addition, it is simpler to generate the low voltage signals required for static devices with acceptable noise levels than to generate the higher voltage signals needed for dynamic logic. These features of static logic memories make them easier to use in systems compared to dynamic memories, but at the expense of increased chip size and manufacturing cost.

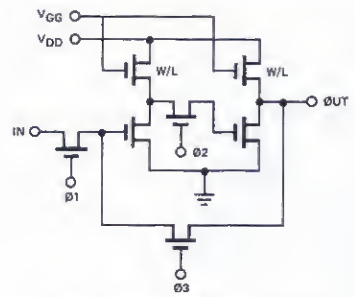
POWER STRUCTURES

Since MOS logic contributes most to applications where high density and low power are required, the power consumption behavior of MOS devices is an important consideration. Power consumption variations with temperature, circuit techniques for reducing power on the chip, power-saving techniques that the user can implement, and a discussion of power-up sequences are included in this section.

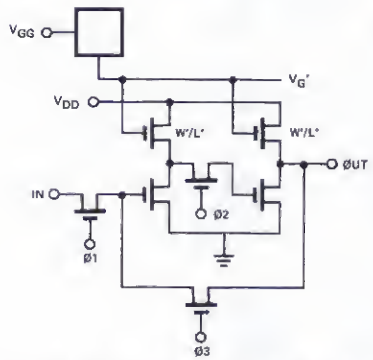
One of the differences already mentioned between bipolar and MOS circuit characteristics is the relationship between the on-chip gain figure and junction temperature. Since on-chip gain for MOS circuits decreases with increasing junction temperature, the worst-case power dissipation occurs at low ambient temperatures. This power consumption decreases as junctions heat up so that a power surge can occur at low ambient temperatures.

Figure 23 shows a circuit design technique used to reduce the power consumed by complex logic functions while minimizing the chip size. Shown here is a comparison of a standard static shift register (SSR) cell and an SSR cell using an intermediate voltage generator (IVG). The V_{GG} power for the cell in Figure 23a is brought directly in from the V_{GG} pin. The load devices are shown with geometry ratios W/L. The length L is large in order to achieve a sufficiently large value of resistance. The same large resistance could be obtained by using a smaller gate voltage and a shorter length as in Figure 23b where the IVG is used to derive the smaller voltage. By utilizing this technique, a smaller geometry can be used for the load device, thus effecting a smaller chip size. Alternatively, a larger resistance can be constructed with the same geometry, thus effecting a saving of power consumed.

INTERMEDIATE VOLTAGE GENERATOR POWER SAVING TECHNIQUE



a. SSR Cell With Direct Power Lines



b. SSR Cell With Intermediate Voltage Generator

FIGURE 23

Another technique for conserving power uses a non-saturating load device design. In this case, the main dc power path is between V_{CC} (+5V) and V_{DD} (either ground or −5 volts). The higher voltage V_{GG} supply provides power for load device gates and some peripheral logic and requires only a small amount of current. As a result, the major current component is multiplied by five volts (or 10 volts if $V_{DD} = -5V$) instead of 17 volts as it is for saturated load device designs. The trade-off is the extra pin required for the additional power supply.

Several methods for minimizing system power dissipation are available to the user of MOS circuits. In general, dynamic logic devices dissipate more power at higher frequencies than at lower frequencies. The power versus frequency characteristic for dynamic shift registers, for example, shows that operation around 100KHz in the standby mode substantially reduces power over operation in the megahertz range (see Figure 18b). Note that further reduction in frequency, however, saves relatively less power. Since bit droppage problems can occur when the frequency is switched over an excessively large range, the designer should restrict the lower frequency of operation

to a value within two orders of magnitude of the upper frequency. A reduction in operating frequency from the megahertz range to less than 100KHz realizes most of the power savings available from this characteristic of dynamic shift registers. Below this range, power is relatively insensitive to frequency variations. In addition to lowering the frequency of operation, the designer can minimize the clock pulse width, thereby reducing the amount of time that load resistors are on during a given clock cycle. This technique does not reduce the power consumed in some dynamic RAMs where power is a stronger function of the number of clock edges occurring per unit time than of the clock duty cycle. Since information is stored on substrate capacitors in dynamic RAMs the other power supply (usually called V_{DD}) can be shut off when the RAM is not cycling. This technique saves power in large memory systems, but only saves a small amount of power on individual parts since when the clocks are not cycling, the major power component is proportional to leakage current.

Static logic device power consumption is less sensitive to frequency variation. Some power savings can be realized, however, since for example, the static shift register power versus frequency characteristic (Figure 18a) shows that the dissipated power at frequencies less than about 100KHz is about half of what it is at maximum frequency. This fact allows the system designer to save power by shutting off the clocks in the standby mode. Care must be taken, however, to ensure static operation by stopping in the proper clock state.

Some savings in power dissipation can be realized in static RAMs by reducing the power supply voltage. As with dynamic RAMs, power can be reduced in static RAMs by pulsing the V_{DD} supply voltage if the RAM is designed with enhancement mode load devices. Data will be lost if the design uses depletion mode load devices, however.

For MOS products that do not have separate substrate bias inputs, the sequence in which power supplies are turned on is not critical as long as the isolation diodes on the chip remain reverse biased. The crucial factor is that no device pin may go more positive than the V_{CC} pin for P-channel devices or more negative than the ground pin for N-channel devices. Those P-channel devices that do have separate substrate bias inputs require the substrate bias supply to be turned on before V_{CC}, and to be turned off after V_{CC}.

OUTPUT STRUCTURE

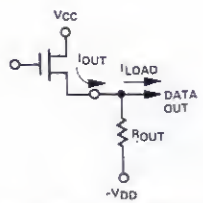
There are several output structures commonly used in MOS circuit designs. Figure 24 presents the major configurations. These are the current sourcing output (bare drain) of Figure 24a, the totem-pole or push-pull outputs of Figures 24b and c, and the tri-state output structure of Figure 24d.

The current source output is most commonly used in MOS dynamic memory devices where optimum speed is a major design goal. The propagation delay through this bare drain structure is relatively short compared to the other outputs. High speed dynamic read/write RAM designs rely on current-sensing bipolar sense amplifiers to interface this type of output to standard logic voltage swings. The outputs of simpler dynamic shift registers are designed with a sufficiently large value of I_{OUT} to allow easy interfacing with TTL logic circuits by merely adding on external pull-down resistor, R_{OUT}. The minimum value of R_{OUT} is determined from dc considerations as shown by the following equation:

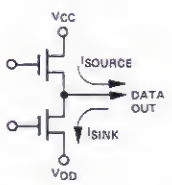
$$R_{OUT} = \frac{V_{OH\,(MIN)} + V_{DD}}{I_{OUT} - I_{LOAD}} \qquad (3)$$

where $V_{OH(MIN)}$ is the desired minimum output voltage with respect to ground in the logic "1" state, V_{DD} is the negative supply voltage to which R_{OUT} is returned, I_{OUT}

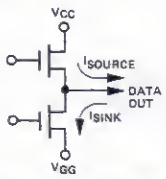
MOS OUTPUT STRUCTURES



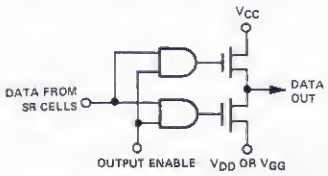
a. Bare Drain Output Structure



b. Push-pull Output Structure (Non-Saturating)



c. Push-pull Output Structure (Saturating)



d. Signetics Patented MOS Tri-state Output Structure

FIGURE 24

is the minimum current that the MOS output will supply for a given $V_{OH(MIN)}$, and I_{LOAD} is the current required by the output load when the output voltage equals $V_{OH(MIN)}$. This structure allows the outputs to be wire-OR'ed for simpler system configurations. One disadvantage of using this type of output is that an external component is required to interface it to another device. Another disadvantage is that the device supplies drive current only during a transistion from LO to HI. In addition, this drive current is shared between the external resistor and the output load impedance since the external resistor cannot be switched off.

Figures 24b and c present the totem-pole or push-pull output. They are the most commonly used output structures for present silicon-gate MOS designs. The two versions indicated differ in the operating mode of the circuitry that drives them. The totem-pole output of a Figure 24b is driven by non-saturating logic. The resulting output voltage swings from V_{CC} to V_{DD}. Since V_{DD} is smaller in magnitude than V_{GG}, the non-saturating totem-pole output dissipates less power for a given output current than the saturating structure of Figure 24c whose output voltage swings between V_{CC} and V_{GG} +2 $|V_T|$. Both push-pull structures actively supply edge current in both directions for enhanced driving of capacitive loads. While the output is being pulled toward V_{DD} or V_{GG} by the lower device, the upper device is turned off. Conversely, as the output is being pulled toward V_{CC} by the upper device, the lower device is turned off. Consequently, the entire drive current capability of the output is supplied to the load rather than being shared with an inactive pull-down or pull-up resistor.

Note that when interfacing this type of output circuit with other logic families, the MOS output voltage range may be greater than the normal input voltage range of the driven logic circuit, and damage to the input structure of the logic circuit is sometimes possible. Concern about the output voltage swing of MOS devices generally focuses on the logic "0" level voltage and the associated sink current characteristics of saturating structures and those non-saturing outputs where V_{DD} is more negative than the most negative supply voltage of the driven device. Typical sink current characteristics of push-pull outputs are shown in Figures 25a and b with respect to ambient temperature and V_{GG} power supply voltage variations. Since chip size constraints preclude building overly large output buffers on MOS circuits, the current sinking capability of MOS outputs is never large enough to damage a driven device's input clamp diode. For this reason the input network of MOS driven logic gates can be adequately protected by a modest-size clamp diode capable of continuously conducting 3 to 5ma of current. Most bipolar logic families have sufficient clamps already on the chip. These that have none require an external clamp diode from the MOS output to the most negative supply voltage (usually ground) of the MOS-driven logic gate.

The sink current curves show that the worst-case drive capability occurs at the high ambient temperatures and at the minimum supply voltages. This result is to be expected since g_m, which decreases with rising temperature, and the

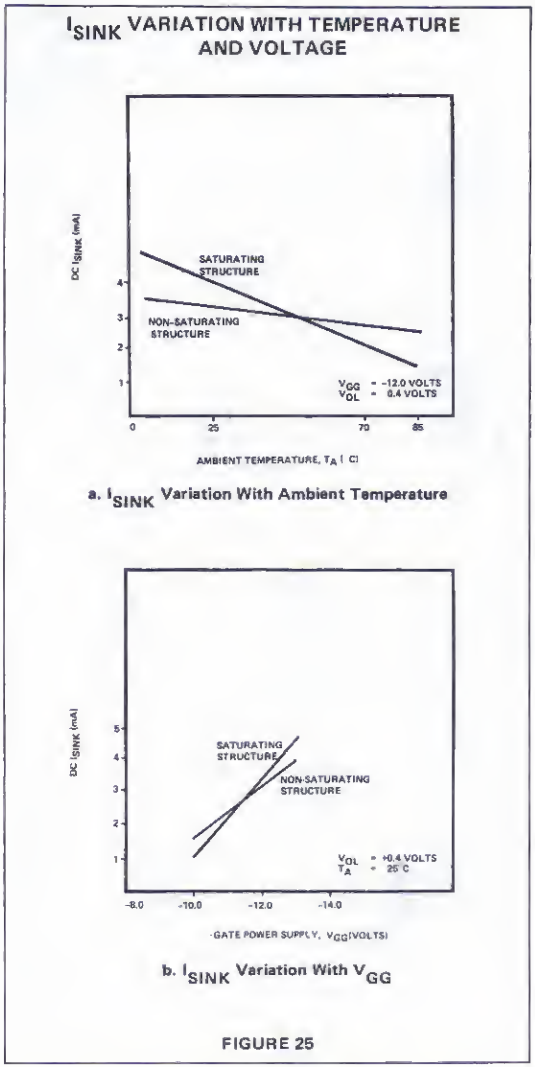


FIGURE 25

gate supply voltage directly affect the current capability of the output transistors. Note that maximum drive capability is required when interfacing MOS to TTL at room temperature rather than at T_A = 70°C. Figure 25b shows that a reduction in V_{GG} drastically decreases the drive current capability of the output for both saturating and non-saturating designs. One advantage of the non-saturating design over the saturating approach is indicated by the slopes of the I_{SINK} versus temperature and I_{SINK} versus V_{GG} curves: the non-saturating design drive capability is less sensitive to temperature and voltage variations.

A variation of the totem-pole output is shown in Figure 24d. This circuit allows the push-pull structure to be disconnected from the load by turning off both the upper and lower drive transistors. The resulting output impedance is very high. This tri-state output structure allows several

outputs to be tied together on a single bus. The number of tri-state outputs that can be wired together is determined by the combined leakage current of the disabled devices that a single enabled output must drive, the load current required to drive the next logic gate, and the rise and fall time constraints in the system. The example in Figure 26 illustrates how the number of devices whose outputs can be tied together is determined. Equation (4) summarizes the results of this derivation:

$$n = \frac{I_{O(MOS)} - I_{IN(TTL)} - (C_{IN} + C_{DIST})\frac{dV_{OUT}}{dt} + I_{LK(MOS)}}{I_{LK(MOS)} + C_{OUT}\frac{dV_{OUT}}{dt}} \quad (4)$$

where $I_{O(MOS)}$ is the MOS output current available; $I_{IN(TTL)}$ is the input current required by the TTL gate; C_{IN} and C_{DIST} are the TTL input capacitance and the distributed stray wiring capacitance respectively; $I_{LK(MOS)}$ is the leakage current of one disabled MOS output; C_{OUT} is the output capacitance of one MOS output; and dV_{OUT}/dt is the desired output voltage slew rate. An example calculation using equation (4) is shown below.

Assume:

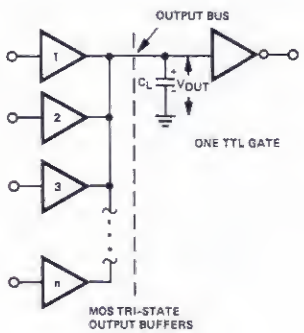
$C_{IN} + C_{OUT} = 15pf$

$dV_{OUT}/dt = 1$ volt/20 nsec = 0.05 v/nsec

$C_{OUT} = 5pf$

$I_{O(MOS)} = 1.6mA$

TRI-STATE BUS INTERFACE CALCULATIONS



$$I_{O(MOS)} = (I_{LK(MOS)})(n-1) + I_{IN(TTL)} + C_L\frac{dv_{OUT}}{dt}$$

Where:

$$C_L = \sum_{i=1}^{n} C_{OUT\text{-}i} + C_{IN} + C_{DIST}$$

$$I_{IN(TTL)} = \begin{cases} 0 \text{ for } v_{OUT} \geq 1.8 \text{ VOLTS} \\ 1\text{-}1.5mA \text{ for } v_{OUT} < 1.8 \text{ VOLTS} \end{cases}$$

$\frac{dv_{OUT}}{dt}$ = Desired Voltage Slew Rate

$$n = \frac{I_{O(MOS)} - I_{IN(TTL)} - (C_{IN} + C_{DIST})\frac{dv_{OUT}}{dt} + I_{LK(MOS)}}{I_{LK(MOS)} + C_{OUT}\frac{dv_{OUT}}{dt}}$$

FIGURE 26

$I_{IN(TTL)} = 0$ until TTL switching threshold

$I_{LK(MOS)} = 1\mu A$

Then:

$$n = \frac{1.6mA - (15pf)\ (.05v/nsec) + .001mA}{.001mA + (.05v/nsec)\ (5pf)}$$

$$= \frac{1.6mA - .75mA\ .001mA}{.001mA + .25mA} = \frac{.851}{.251} = 3.4$$

With the modest slew rate requirement used in this example, one tri-state MOS output will drive one TTL load and three other MOS outputs. To increase the fanout with this load would require a larger value for $I_{O(MOS)}$. One way to increase this value is to use nominal supply voltages rather than minimums and to restrict the upper temperature limit to less than 70°C since the $I_{O(MOS)}$ specification assumes worst-case voltages and temperatures.

The circuit techniques used to construct MOS output structures have evolved in roughly the same order as presented in this discussion. The earliest designs utilized the bare drain approach. The totem-pole output was the next development with saturating and non-saturating versions appearing at about the same time. A modified non-saturating output where V_{DD} equals zero volts was then developed to eliminate the need for any external clamping diodes by restricting the minimum logic "0" voltage to ground. This technique is used wherever the extra pin required for the V_{DD} power line can be spared. The ultimate in TTL compatibility can now be attained by using an N-Channel silicon gate process which allows operation with only a five-volt power supply. This approach offers the designer the option of directly mingling the highly dense MOS technology, with all its power savings and complex logic function advantages, with high speed, low cost TTL technology in order to obtain the most optimum system design.

MOS INTERFACE CHARACTERISTICS

This section provides suggested techniques for interfacing MOS devices with other specific logic families. There is a separate entry for each logic type. The interface circuits presented represent suggested methods—other approaches are possible and will be more appropriate in some contexts. The previous sections of the User's Guide were designed to acquaint the user with the characteristics of Silicon Gate MOS devices. Given this background information, the user can derive any required interface where silicon gate MOS circuits are used in conjunction with other logic families. The following sections cover suggested MOS interfaces to the more common logic families, and each contains separate subsections cover the MOS input interface and the MOS output interface.

TRANSISTOR-TRANSISTOR LOGIC

This logic family is the most commonly used in existence today. The need for TTL-compatible MOS circuits was one of the major motivations for developing the silicon gate process.

Figure 27a shows the output structure of a standard 7400 series logic gate. The accompanying charts in Figures 27b, c, d, and e graphically illustrate one of the common misconceptions of using MOS devices with standard TTL circuits. The TTL specifications (Figure 27e) appear to indicate the normal output logic "1" levels from TTL devices are insufficient to drive silicon gate MOS devices directly. Further examination of the TTL specifications and the output structure of the TTL devices themselves will show that this conclusion is not valid. The following equation, referring to Figure 27a, gives the output logic "1" level, V_{OH}.

$$V_{OH} = V_{CC} - I_B R_B - V_{BE(Q1)} \left|_{I_{OUT}} - V_{d1}\right|_{I_{OUT}} \quad (5)$$

The fact that V_{CC} is the substrate reference voltage for P-channel silicon-gate is an important point. For this reason, the V_{OH} equation need not take V_{CC} variations into account since the MOS threshold is really $V_{CC} - V_T$. As a result, the MOS input voltage requirements directly track V_{CC} variations such that if V_{CC} = 4.75 volts, the MOS $V_{IH(MIN)}$ = 2.95 volts, and $V_{IL(MAX)}$ = 0.8 volts. Thus, the input noise margins shown in Figures 27c and d are independent of V_{CC} variations as long as the TTL circuits and the MOS circuits utilize the same V_{CC} power supply. The term $I_B R_B$ in the equation (5) is negligibly small. The other two terms are the voltage drops across the two diodes in the TTL output structure at a forward current equal to I_{OUT}. In the case of loading the TTL device with an MOS device, I_{OUT} is extremely low (at most 500nA). At this current level, V_{D1} and $V_{BE(Q1)}$ are about 480mV each at T_A = 25°C. The resulting V_{OH} is

$$V_{OH} = 5.00 - \cancel{I_B R_B}^{\,0} - 0.48 = 4.04 \text{ volts} \quad (6)$$

Substrating a correction for each diode of 2mV/°C, V_{OH} at T_A = 0°C, worst case with respect to ambient temperature, is

$$V_{OH}\left|_{T_A = 0°C} = V_{OH}\right|_{T_A = 25°C} - (.002)\,(25)\,(2) \quad (7)$$

$$= 4.04 - 0.010 = 3.94 \text{ volts}$$

Measurements of V_{OH} without load current verify this result. Therefore, the noise margin for a logic "1" level at T_A = 0° C is approximately 800mV. When the TTL gate is loaded with a fanout of ten and an MOS input, V_{OH} is

$$V_{OH} = 5.00 - 0.63 - 0.63 = 3.74 \text{ volts} \quad (8)$$

Again, subtracting a temperature correction for each diode at T_A = 0°C, V_{OH} is

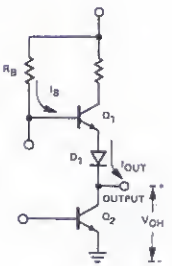
$$V_{OH}\left|_{T_A = 0°C} = V_{OH}\right|_{T_A = 25°C} - 100mV \quad (9)$$

$$= 3.74 - 0.10 = 3.64 \text{ volts}$$

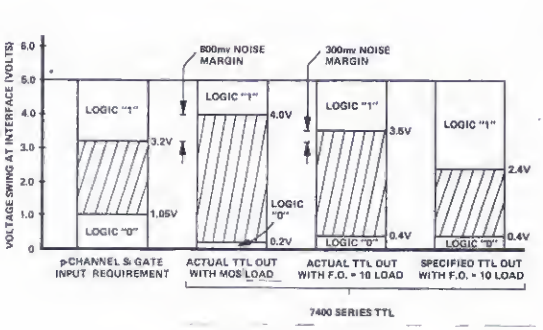
For this situation, then, the noise margin at T_A = 0°C is about 400mV. The original TTL specifications, now taken as industry standards, evolved from the TTL input voltage requirements. Specifying TTL $V_{IH(MIN)}$ at 2.0 volts and allowing for 400mV of noise margin implies $V_{OH(MIN)}$ = 2.4 volts even though, physically, the devices' V_{OH} is considerably higher. The conclusion derived from this treatment is that input pull-up resistors are not required on Signetics P-Channel silicon gate MOS devices in order to construct the proper TTL to MOS interface.

The MOS to TTL interface is equally straightforward with the exception of the MOS bare drain output which requires

VOLTAGE RANGE COMPARISON FOR AN INTERFACE EXAMPLE



a. Standard TTL Output Structure



b. c. d. e.

*NOTE: The Voltage Values Given Are For V_{CC} = 5.00V.

FIGURE 27

an external pull-down resistor. Refer to the Output Structure section of the handbook for the method used to calculate the value of this resistor. Subfamilies of the standard 7400 series TTL group such as 74L, 74S, 74H, and 74LS have different interface requirements for the MOS to TTL interface, but not for the TTL to MOS interface. The MOS output structure is designed to handle one standard TTL load over the full commercial temperature and voltage tolerance range. The 74H and 74S families require the MOS output to handle 1.25 standard TTL loads. This stricter load requirement constrains either the voltage range (especially V_{GG}) or the temperature range over which the MOS devices can be operated. The 74L and 74LS devices place less stringent demands on the MOS outputs than standard 7400 series. Their logic "0" input current requirements are about 200μA and 400μA respectively, or 0.125 and 0.25 standard TTL loads. As a result, these TTL families can be used to increase the fanout of the MOS outputs.

The 82S series, another subfamily of Transistor-Transistor Logic, uses the Schottky process and a pnp input structure to reduce the input logic "0" current requirement to 0.25 to 0.5 standard TTL loads.

Figure 28 is a table that contains a summary of the various TTL family gates and their input current requirements with respect to a standard TTL load (1.6mA with VIL = 0.4 volts). Care must be taken when tying TTL inputs together to perform an inverter function because NOR gates represent two TTL loads when two inputs are tied together.

TTL INPUT LOAD REQUIREMENTS

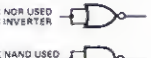
STRUCTURE	NO. OF STANDARD TTL LOADS PRESENTED TO MOS OUTPUTS
 74XX	1.0
 74H	1.25
 74L	0.125
 74S	1.25
 74LS	0.25
 82S	0.25 - 0.50
 74XX NOR USED AS INVERTER	2.0
74XX NAND USED AS INVERTER	1.0

FIGURE 28

COMPLEMENTARY MOS LOGIC

Complimentary Metal Oxide Semiconductor logic is rapidly becoming the most popular technology for high speed, low power applications where the relatively large current drain of the TTL family proves prohibitive. Although CMOS devices are fabricated with the MOS processing technology, there are significant differences in the input structure of CMOS gates. The input voltage is restricted to range from V_{DD} to V_{SS} because input protection devices are returned to both power supplies. The resulting diodes are large enough, however, to handle the output sink current drawn by the driving MOS device in the MOS to CMOS interface. The diagrams presented in this section suggest an interface based on the type of MOS output structure that is used.

The CMOS to silicon gate MOS interface is very direct. The output voltage swing of CMOS devices is from V_{DD} −0.05 volts to V_{SS} +0.05 volts with zero load current. Consequently, CMOS gates will directly drive silicon gate MOS devices as long as the CMOS power supply voltages are correctly chosen. The restriction on the power supplies results from the ability of CMOS to operate on as little as three volts differential between V_{DD} and V_{SS}. As a result, to drive silicon gate MOS directly, V_{DD} must be greater than VIH (Min) for the silicon gate MOS device, and V_{SS} must be less than VIL (Max). These values are typically 3.2 volts and 0.8 volts, respectively. (See pages 7-28 and 7-29)

DIODE-TRANSISTOR LOGIC

Diode-Transistor Logic circuits, at one time the most popular logic family, are still in widespread use today. The input and output characteristics of these devices are very similar to those of TTL circuits. For this reason, the DTL to MOS and MOS to DTL interfaces are the same as those used for the TTL family. For ease of reference, the interfaces are repeated in this section. (See pages 7-30 and 7-31)

EMITTER-COUPLED LOGIC

The increased need for high speed logic gates in memory system applications where MOS memories are used has created a need for simple conversion from MOS logic levels to Emitter-Coupled Logic levels. The conversion from TTL levels to ECL levels can be accomplished with already-existing monolithic translators such as the 10124 (TTL-to-ECL) and the 10125 (ECL-to-TTL). Taking advantage of the TTL-compatibility of silicon gate MOS, the MOS-to-ECL and ECL-to-MOS interfaces are very easily constructed with these two products as shown in the accompanying diagrams. The current loading factor of the TTL-to-ECL translator must be taken into account since silicon gate MOS outputs are only designed to handle one TTL load. If the input load current for the translator is greater than 1.6mA, a standard TTL buffer can be inserted between the translator and the MOS device. (See pages 7-32 and 7-33)

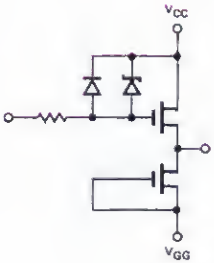
TTL OUTPUT CIRCUITRY

INTERFACE CIRCUITRY

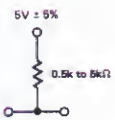
MOS INPUT CIRCUITRY

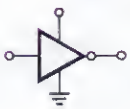
74XX 74LXX
74HXX 74LSXX
74SXX 82SXX

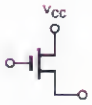
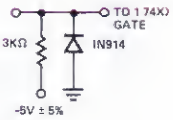
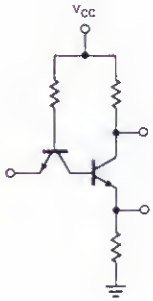
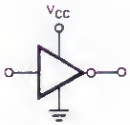
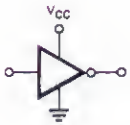
TTL WITH PUSH-PULL OUTPUT STRUCTURE

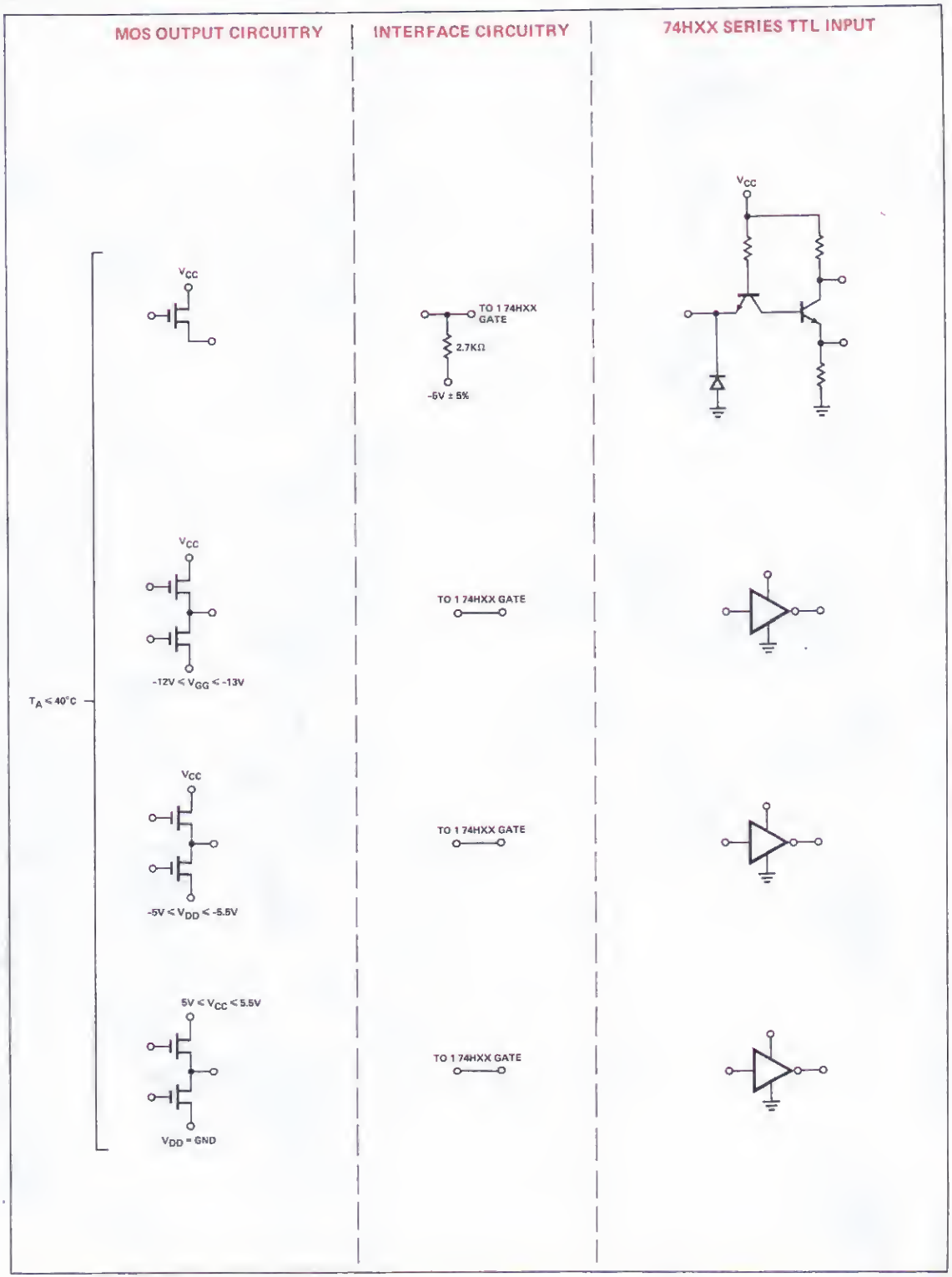


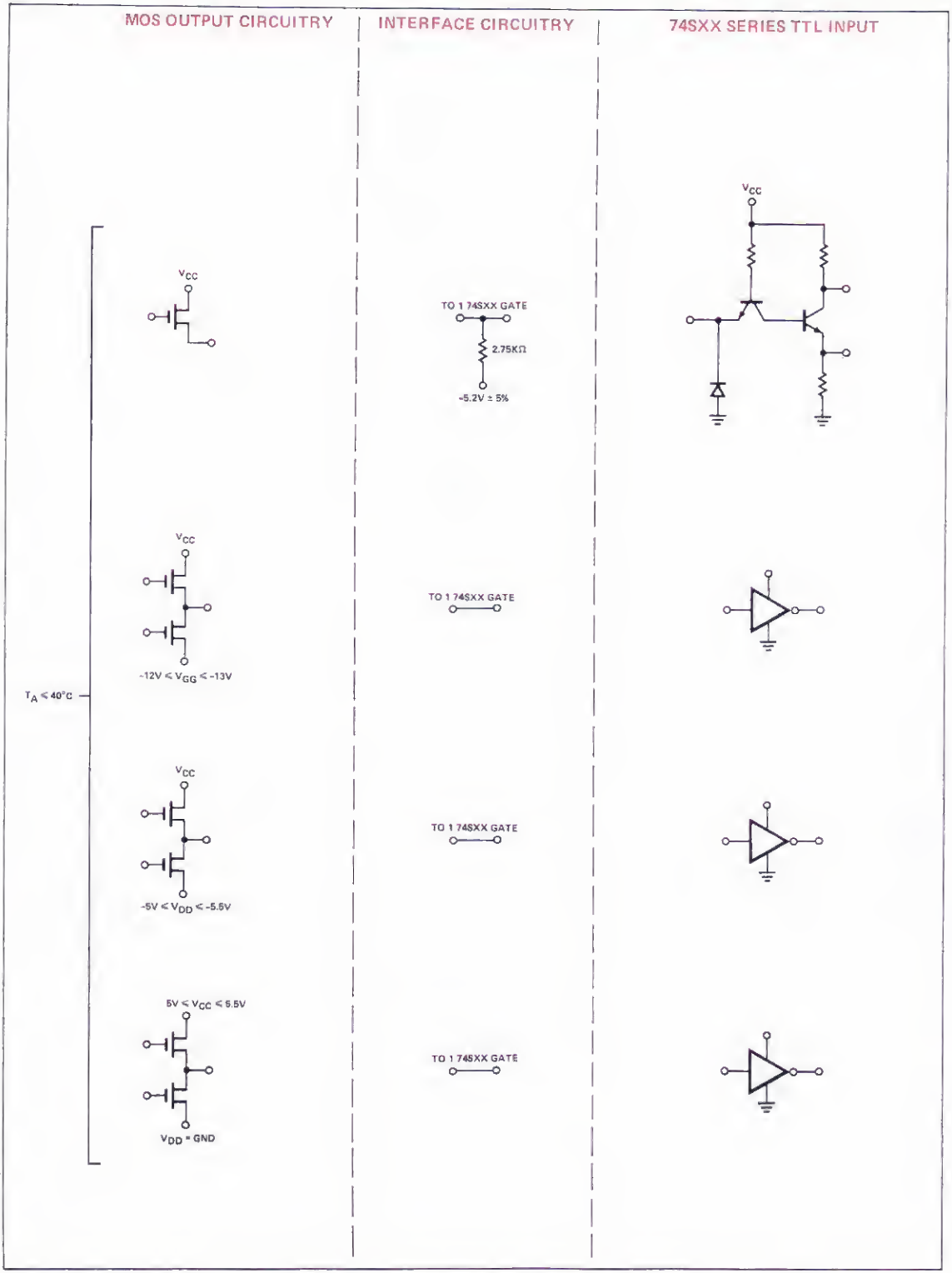
TTL WITH OPEN COLLECTOR OUTPUT STRUCTURE

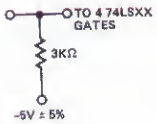
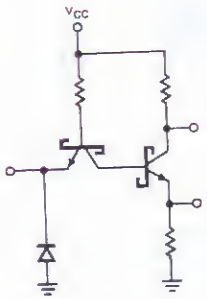
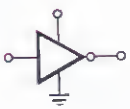
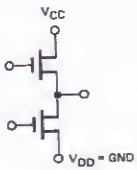
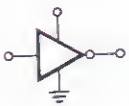


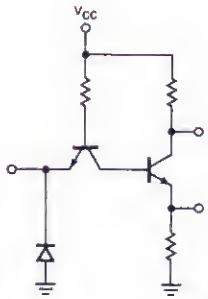
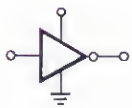
MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	74XX SERIES TTL OUTPUT
		
		
		
		

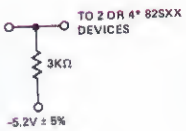
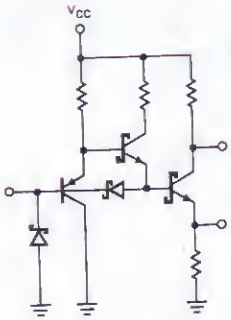
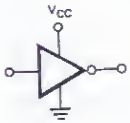
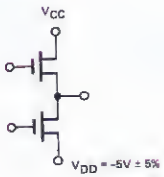
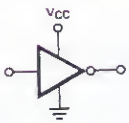
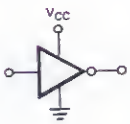
MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	74XX SERIES TTL INPUT (NO CLAMP DIODE)
		
		
		
		


MOS OUTPUT CIRCUITRY
INTERFACE CIRCUITRY
74HXX SERIES TTL INPUT
V_{CC}
TO 1 74HXX GATE
2.7KΩ
-5V ± 5%
V_{CC}
TO 1 74HXX GATE
-12V ≤ V_{GG} ≤ -13V
V_{CC}
TO 1 74HXX GATE
-5V ≤ V_{DD} ≤ -5.5V
5V ≤ V_{CC} ≤ 5.5V
TO 1 74HXX GATE
V_{DD} = GND
T_A ≤ 40°C


MOS OUTPUT CIRCUITRY
INTERFACE CIRCUITRY
74SXX SERIES TTL INPUT
$T_A \leq 40°C$
V_{CC}
TO 1 74SXX GATE
2.75KΩ
-5.2V ± 5%
V_{CC}
$-12V \leq V_{GG} \leq -13V$
TO 1 74SXX GATE
V_{CC}
$-5V \leq V_{DD} \leq -5.5V$
TO 1 74SXX GATE
$5V \leq V_{CC} \leq 5.5V$
V_{DD} = GND
TO 1 74SXX GATE
V_{CC}

MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	74LSXX SERIES TTL INPUT
		
		
		
		

MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	74LXX SERIES TTL INPUT
		
		
		
		

MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	82SXX SERIES TTL INPUT
		
		
		
		

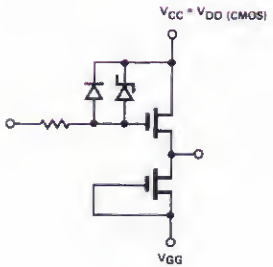
* Depending on I_{IL} (Max) for particular 82SXX Device

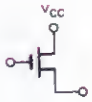
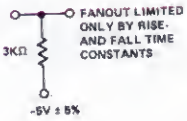
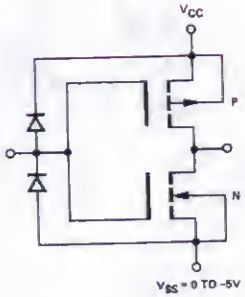
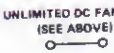
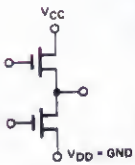
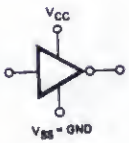
C–MOS OUTPUT CIRCUITRY

C-MOS LOGIC

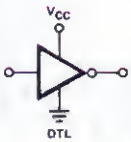
INTERFACE CIRCUITRY

MOS INPUT CIRCUITRY



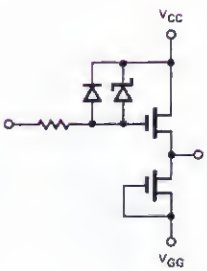
MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	C-MOS LOGIC INPUT
		
		
		
		

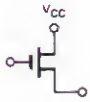
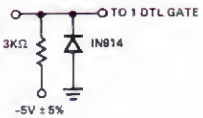
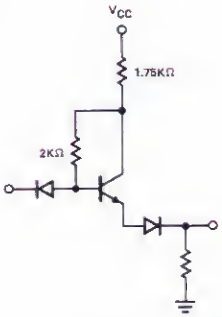
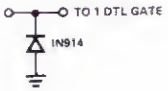
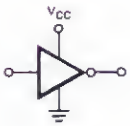
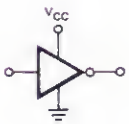
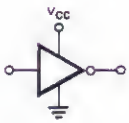
DTL OUTPUT CIRCUITRY



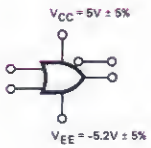
INTERFACE CIRCUITRY

MOS INPUT CIRCUITRY



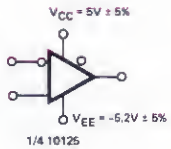
MOS OUTPUT CIRCUITRY	INTERFACE CIRCUITRY	DTL INPUT CIRCUITRY
		
		
		
		

ECL OUTPUT CIRCUITRY



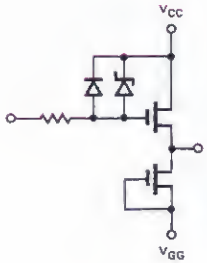
ECL

INTERFACE CIRCUITRY



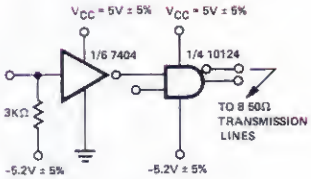
1/4 10125

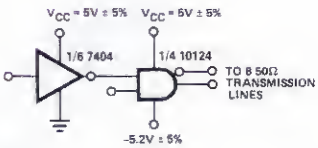
MOS INPUT CIRCUITRY

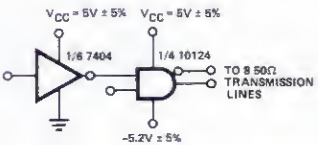


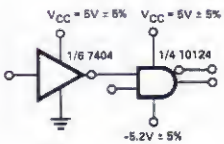
MOS OUTPUT CIRCUITRY

INTERFACE CIRCUITRY

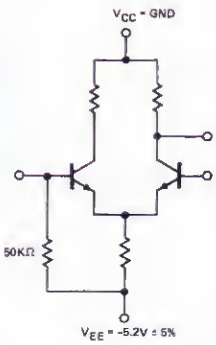


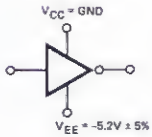


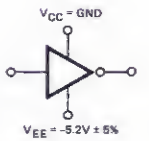


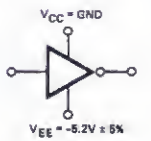


ECL INPUT CIRCUITRY









INTRODUCTION

The 2526 is a high speed 5,184-bit Static Read-Only Memory. It may be organized as 64 x 9 x 9 for use as a character generator in dot matrix displays, or as a 512 x 9 ROM for general purpose use. It features TTL compatible inputs, three-state TTL compatible outputs, two standard supply voltages (+5, −12), output data latches, and less than 700ns access time. The 2526 is fabricated using Signetics P-MOS silicon gate process and is packaged in a 24-pin silicone dual in-line package.

INPUT CIRCUITS

The inputs to the 2526 use a configuration similar to that used in most of the other 2500 series products. Interface requirements with TTL circuitry are described in detail in the Signetics MOS Users Guide. In general, a standard TTL gate driving only the 2526 does not require any interfacing resistors. See Figure 1. If another TTL gate is driven in addition to the 2526, a 10k ohm pull-up resistor will improve the input noise margins.

INPUT INTERFACE

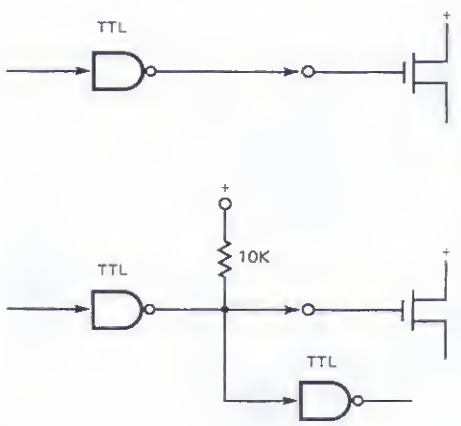


FIGURE 1

OUTPUT CIRCUITS

The outputs from the 2526 use a three-state push-pull configuration that allows wired-OR connection of several circuits for expanded capacity. The push-pull circuitry provides low impedance outputs for both high and low output voltages. See Figure 2. For a low output voltage Q_2 is turned ON and Q_1 is turned OFF with Q_3 and Q_4 kept OFF by a high Output Enable voltage. For a high output voltage Q_1 is turned ON and Q_2 is turned OFF while Q_3 and Q_4 are OFF. When the Output Enable voltage goes low, however, both Q_3 and Q_4 are turned ON, keeping Q_1 and Q_2 both OFF for any condition the output latch assumes. In this state the output of the 2526 is essentially floating,allowing other circuits to dominate the output line.

Figure 3 shows one way to make use of this three-state output. Two 2526 Character Generators are tied together at their outputs and fed to the receiving logic circuitry, e.g., a parallel to serial converter. One 2526 can contain the dot matrix information for upper case characters and the other can contain the lower case information, thus providing a full 128 character set. All inputs for the two generators are tied in parallel except the Output Enables which serve as A11 address inputs. One 2526 receives the A11 signal and the other receives $\overline{A11}$. In this way only one set of outputs at a time will activate the output lines. If the system configuration requires periods where neither output is active, that fact can be gated with A11 to turn off both Output Enable signals. To reduce power dissipation, the A11 information can be gated with the READ signals to avoid turning on the unused 2526.

OUTPUT CIRCUITRY

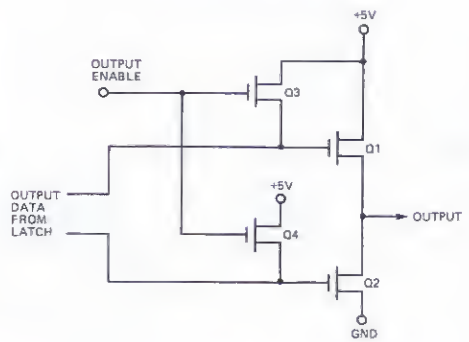


FIGURE 2

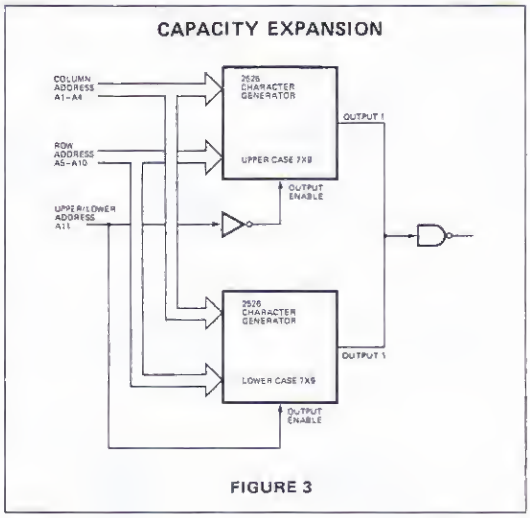


FIGURE 3

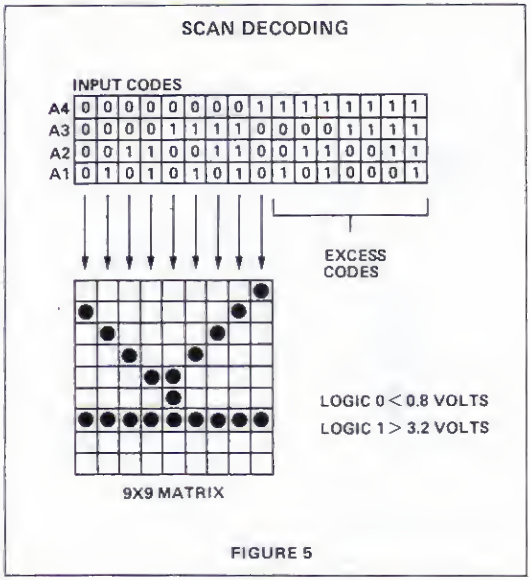


FIGURE 5

ADDRESS DECODING

The Signetics 2526 Character Generator is organized to provide 64 character locations with each location described by a 9 x 9 matrix of bits. The block diagram in Figure 4 shows the address assignments for the character and scan functions. The six address inputs A5 through A10 are decoded directly to provide a 1-of-64 character selection. The four address inputs A1 through A4 are decoded to provide a 1-of-9 selection of scans within each character. Since four address lines can generate 16 scan selections instead of only 9, there are seven excess codes. See Figure 5. The 1-of-9 scan decoder forces the excess input codes to generate all logic "0's" at the output latches. The address deciding circuits are only activated during a READ operation in order to save power when the memory is not being used.

TIMING

The timing diagram in Figure 6 shows how the READ signal controls the operation of the memory. The address inputs propagate through the decoders and the bit matrix when READ goes low. The output data are strobed into the latches when READ goes high. The state of the OUTPUT ENABLE signal determines whether or not the latched data are transferred to the outputs. With OUTPUT ENABLE high, the worst case access time from stable addresses to valid output data is 700ns. Notice that addresses must be stable for only a short period of time so that address changes may be made in parallel with the access operations. Once the data are set into the latches, they remain stable for a full READ cycle until the next cycle's data are available.

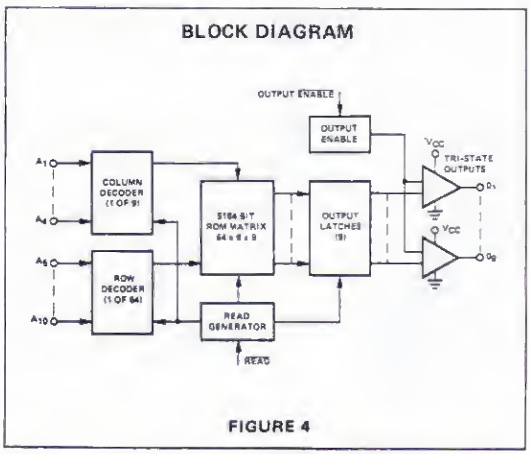


FIGURE 4

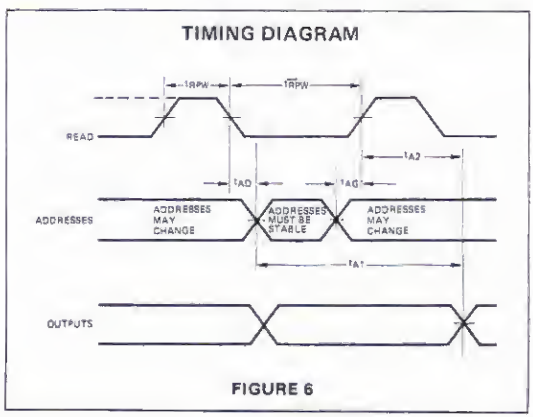


FIGURE 6

MEMORY ORGANIZATION

The 2526 is intended primarily for use as a 7 x 9 dot matrix character generator, and the address decoding scheme reflects this purpose. Address lines A1 through A4 (see Figure 5) generate the required nine scan selects plus seven excess codes. Thus, an attempt to use the 2526 with all ten address lines in a 1024 x 9 configuration would fail because there are only 5,184 bits in the memory and the excess input address codes would not be able to generate relevant output data. However, if address input A4 is tied to a logic "0", the excess codes are eliminated. The remaining nine address lines may then be used to address a 512 x 9 ROM. The ninth scan in each character is ignored along with the excess codes and a subset of 4,608 bits is used to provide the 512 x 9 capacity.

Other organizations are possible, of course, as long as the total memory capacity is not exceeded. 576 x 9 is the real capacity of the memory (576 x 9 = 5,184). The extra 64 x 9 (576 x 9 – 512 x 9 = 64 x 9) can be accessed by careful use of address A4. See Figure 7. The critical condition is stated in the figure: when A4 is logical "1", A0, A2, and A1 should be logical "0's". When A4 is logical "0", any code is allowed in the remaining nine bits. When some form of counter is used to generate the address inputs, it will often be convenient to assign the most significant bit (MSB) to A4 and the six least significant bits to A5 through A10. In this way, the highest allowed bit configuration will correspond to a binary count of 575 and the forced zero states of A3, A2, and A1 will be easier to implement.

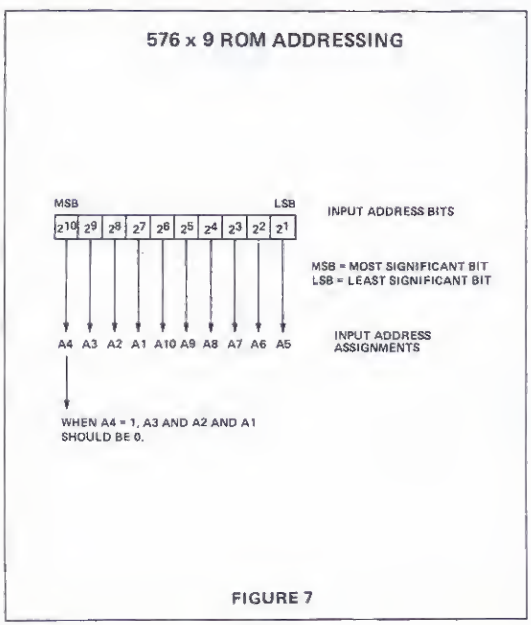


FIGURE 7

CHARACTER ORGANIZATION

When used as a 7 x 9 dot matrix character generator, the 9 x 9 dot configuration of each character allows the 2526 to be used with either vertical or horizontal scanning techniques. Figure 5 shows a 7 x 9 configuration for the letter K that is oriented for use with a horizontal scan. As each horizontal slice through the character is extracted from the ROM, the two extra bits may be ignored and the seven remaining bits serially shifted to control the dot formation.

Figure 8 shows the letter K oriented within the 9 x 9 matrix for use with a vertical scan. Each vertical slice through the character is extracted from the ROM and then serially shifted to control the dot formation. Two complete scans are not used for dots and may supply blank spaces between characters or may be ignored. Alternatively, those extra scan positions may be put to good use for translating character codes. When a code translation is desired, the column address (A1 through A4) is set to the appropriate translate scan instead of one of the dot matrix scans, and the code to be translated forms the row address (A5 through A10). The dot matrix contents of that character location are not related to the input code, but the output from the translate scan provides the desired new code.

Assume that the dot matrix letter K in Figure 8 is placed in the character array at an address corresponding to the ASCII-6 code for K (001011). Then the dots for K can only be retrieved by using the proper ASCII code as an address. The same code pattern in EBCDIC, however, stands for the period. To perform an EBCDIC to ASCII translation it is only necessary to insert the ASCII code for the period (101110) in the translate scan of the K character position. This code can then be used directly for any purpose or it can, in turn, be applied as an input to select the dot matrix for the period.

The spare bits in the 9 x 9 matrix of each character are most convenient to use for translations when the matrix is arranged for vertical scans. In that way a single read operation can perform the translation. A 7 x 9 vertical matrix leaves two spare scans for translations so that a two-way translation between two codes is possible, or two source codes can be translated into a single target code. The spare bits in the horizontal scan case are only available two at a time, so are more awkward to use for translations. In either case, the spare bits can be used to expand the character dot matrix from 7 x 9 to 9 x 9. Several special characters can be constructed (e.g., arrows) and some augmented standard characters (e.g., %) can be more legible.

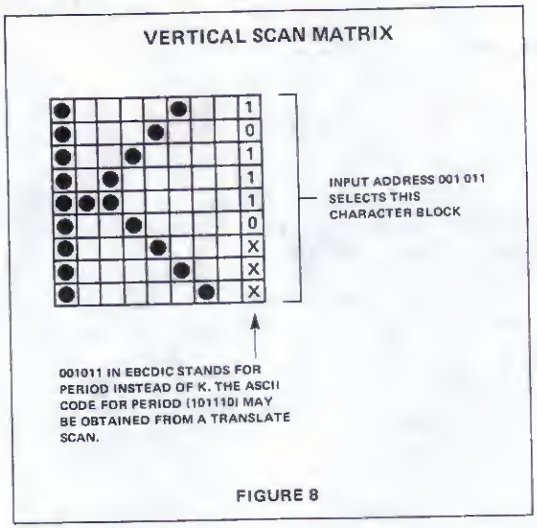


FIGURE 8

APPLICATION AREAS

There are many places where a nine bit wide ROM can be useful. A nine bit output from a function look-up table can provide an extra degree of accuracy. A sine function table, for example, could supply an added bit of resolution in the result. For arithmetic tables with 8-bit operands, the ninth output bit can be used as a sign bit or a carry bit for increased flexibility. Many byte-plus-parity systems are organized around 9-bit data paths and some of their memory requirements can only be satisfied with a 9-bit ROM. 9-bit or 18-bit minicomputers often need Read Only instruction storage for bootstrap loaders and other non-volatile routines.

The added sophistication of new CRT terminal designs is making 7 x 9 characters more and more popular. Increased legibility, decreased errors and better lower case characters are the immediate advantages. The 2526 provides an economical, easy-to-use approach for implementing 7 x 9 character graphics.

1024-BIT STATIC MEMORY

INTRODUCTION

The Signetics 2602 is a 1024-bit Random Access Read/Write Memory. It is fabricated with Signetics N-Channel Silicon Gate technology.

FEATURES

- 1024 x 1 ORGANIZATION
- COMPLETELY STATIC OPERATION
- +5 VOLT POWER SUPPLY ONLY
- TTL COMPATIBLE INPUTS
- THREE-STATE TTL OUTPUT
- 16-PIN DIP PACKAGE
- 200mW DISSIPATION TYPICAL
- N-CHANNEL SILICON GATE TECHNOLOGY
- 1 μs ACCESS AND CYCLE TIMES

SUPPORT CIRCUITRY

The dominant system design characteristic for the 2602 is ease of use. This is a result of several unusual features, with fully static operation as perhaps the most important. Since the static memory cell does not depend on stored charge for its data retention, it does not need periodic refreshing. Thus, the memory does not require external circuitry to generate and control refresh cycling and refresh addresses. The on-chip support logic can also be simplified. See the block diagram in Figure 1.

BLOCK DIAGRAM

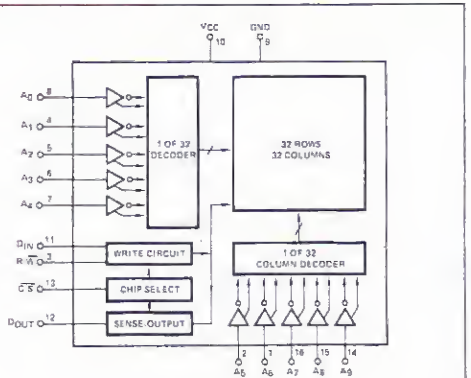


FIGURE 1

In addition to the refresh hardware costs imposed by dynamic memories, there is also a performance price to pay. Each refresh cycle ties up the memory and makes it unavailable for normal data operations. There are several interesting approaches to minimizing the performance impact of the refresh cycles, but each involves an even greater investment in support logic. Both the hardware and performance penalties of dynamic memory refreshing are eliminated by the 2602 since no refreshing of any kind is required by the device.

In the 2602 the on-chip support circuits, as well as the memory cells, are static. Thus no clocks are required for any part of the memory operation. Memory clocks for dynamic memories have proven to be very difficult to drive, distribute, and time properly so that their complete elimination saves design and debug expenses, and reduces support logic, clock driver and distribution circuitry costs.

The output of the 2602 is a three-state, push-pull circuit that can drive a TTL data bus. For increased capacity several chips may be directly wire-ORed, taking advantage of the three-state output. No sense amplifiers or chip buffers are required. The problems associated with the distribution of low level sense lines and with coupled sense noise are eliminated. Figure 2 shows the output buffer circuit.

With 5 pF of typical input capacitance on any signal input and no pull-up resistors required to achieve a reliable high-level input voltage, any simple TTL logic can be used to drive arrays of the 2602 memory devices. With no high voltage, high current, or low level interface signals, noise and crosstalk problems are practically non-existent.

The net result of all these features is a dramatic decrease in the external support electronics required to implement a memory system. With greatly simplified driving, no clocks, no refreshing, and no sensing, the 2602 has eliminated all the major headaches associated with semiconductor memory system design. The cost of support electronics is also dramatically decreased. The result is that memory system costs per bit relative to dynamic memories are very attractive for 2602 memory systems of small and moderate capacity.

OUTPUT CIRCUITRY

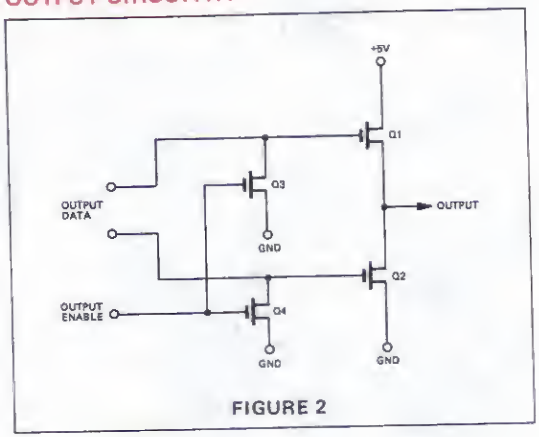


FIGURE 2

POWER

The 2602 contributes in other ways to decreased memory system costs. Only one standard supply voltage, +5V ±5%, is required. Not only are multiple supply costs eliminated, but power distribution and decoupling problems are minimized.

The low average power of less than 200mW typical and the important absence of peak currents both contribute to ease of use and lower costs. The power dissipated by the support circuits in a dynamic memory system — even a small one — can be a large percentage of the system power demands. With the 2602 static memory, the support dissipation is practically eliminated and the memory cell dissipation is very low. Power and cooling costs are, therefore, much less of a factor in the total memory system economics.

CHIP ENABLE

The Chip Enable signal on the 2602 performs three interrelated functions. It controls the status of the three-state output signal, it acts as the decimal address input for memories of more than 1024 words, and it enables and disables the write circuitry.

For a 1K word memory where the outputs share a data bus with other logic subsystems, the $\overline{\text{Chip Enable}}$ signals can be tied together and used simply to connect or disconnect the output data from the data bus. A 2K word version of such a memory (see Figure 3) could then gate the bus connect information with the 11th address bit to form two $\overline{\text{Chip Enable}}$ signals. The output data lines from the first 1K words are wire-ORed with the output data lines from the second 1K words. The two $\overline{\text{Chip Enable}}$ signals will then connect the first 1K or connect the second 1K or disconnect both from the output data bus. Notice that the Read/$\overline{\text{Write}}$ lines need not be gated with the 11th address bit since an unselected chip automatically has the write circuit disabled.

The Read Cycle for the 2602 is very easy to execute. See the timing diagram in Figure 4. With the chip enabled and in the read state, simply input an address. The data will be valid at the output after the access time has elapsed. Because there are no clocks to define the Read Cycle, it is measured as the time addresses are required to be stable. This interval is from the latest arriving address to the earliest departing address. For the same reason the access time should be measured from the latest address input.

Care should be taken to make sure that the Read/$\overline{\text{Write}}$ line is fully in the Read state before any cycle starts. Notice that one of the memory cells is being addressed at all times;

CHIP SELECT GATING

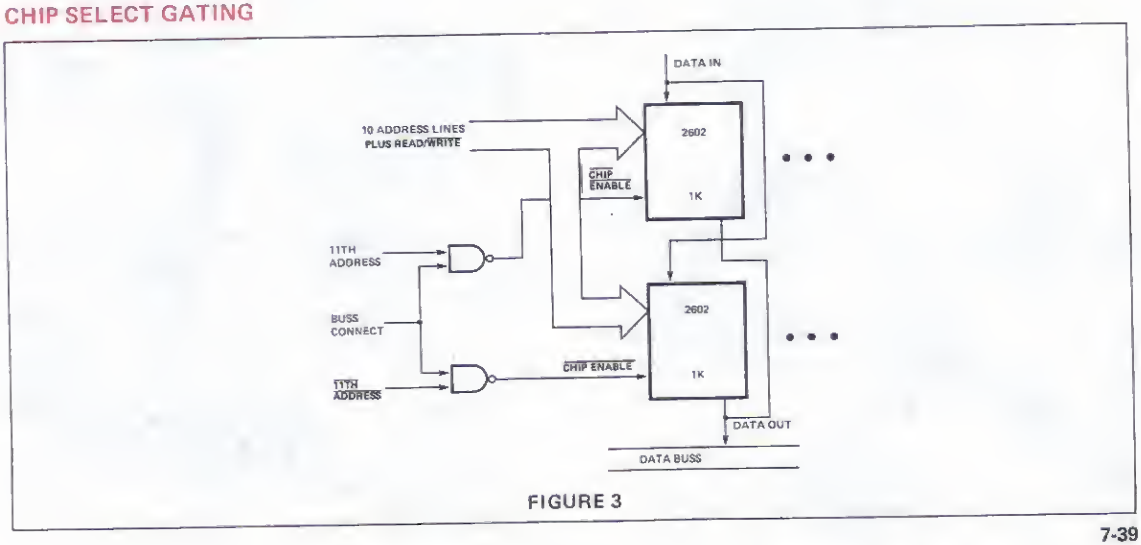


FIGURE 3

TIMING DIAGRAM

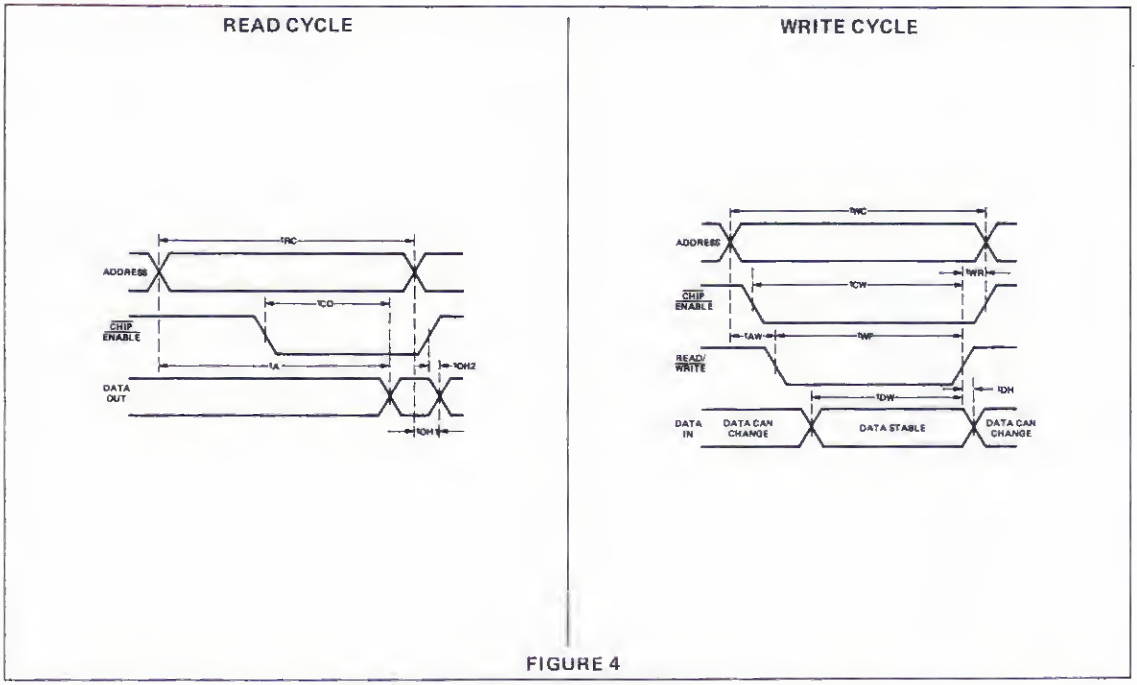


FIGURE 4

there is no quiescent state for the memory array. Thus, any time the Chip Enable and Read/Write lines are both low, something will be written somewhere. The Read/Write line should be considered normally high with a negative-going write pulse allowed only under strict conditions.

The Chip Enable signal may arrive sometime after the start of a cycle without impacting the access time. This will often come in handy when there are extra levels of address gating involved with generating the Chip Enable signal.

WRITE OPERATIONS

The write cycle is also measured by the required stable address time. Since the Chip Enable signal gates the write circuitry, it must arrive earlier than in a read cycle so that the write pulse can propagate properly into the cell array. Notice that the stable addresses must overlap both the start and finish of the write pulse. It is important that the desired cell, and only the desired cell, be fully selected before the write pulse arrives and that the write pulse is fully gone before the addresses begin to change at the cell. The propagation path for the write pulse into the cell is shorter than the address path through the decoders.

For a minimum write cycle the timing of the write pulse is important. Notice in the timing diagram that t_{AW} plus t_{WP} plus t_{WR} adds up to a full 1000ns. A longer write cycle would allow more flexibility in the write pulse timing, and would allow the write pulse window to be adjusted within the cycle.

WAVEFORMS

The waveform picture in Figure 5 shows the 2602 in action. The test pattern being run is a simple one designed to check the general operation of every cell. The memory had previously had zeroes stored in all 1024 cells. Then a pattern of Read-Write-Read is executed at every cell location. The first Read at each cell is used to check for the previously written zero. The Write cycle then writes a one in the addressed cell and the second Read confirms that a one was in fact stored. The address then changes and the three operations are repeated on the next sequential cell.

Notice that in situations like the one pictured in Figure 5 where multiple cycles are executed at one address, there is no obvious, well-defined start of each cycle. Simple external time delays (not shown in the picture) serve to mark the transitions from cycle to cycle. The first change in the Data Out signal following the A_0 address change reflects the zero being read at the newly addressed location. During the succeeding Write cycle, the Data Out line indicates the polarity of the data being written in the cell. At the end of the Write cycle, the same cell is read again and the Data Out signal shows that a one was successfully stored. When the addresses change again, this sequence is repeated.

WAVEFORM

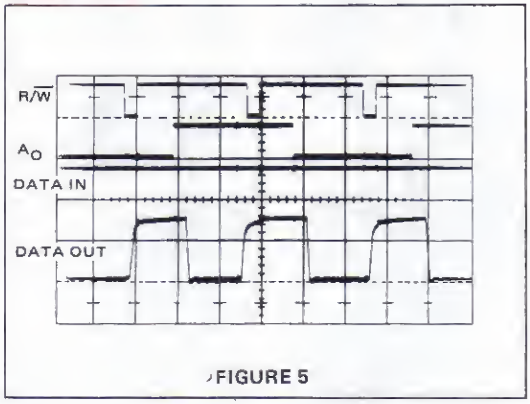


FIGURE 5

MEMORY CELL

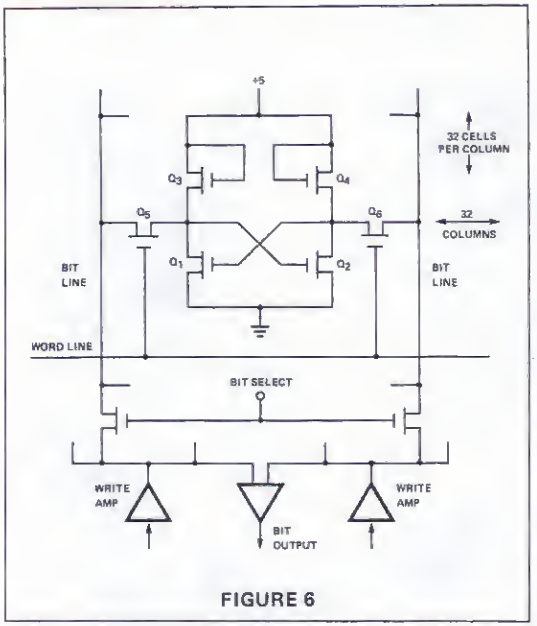


FIGURE 6

STORAGE CELL

Figure 6 is a schematic of the memory bit cell in the 2602. It is a standard six device cell configuration, using two cross-coupled devices (Q1, Q2) with active pull-ups (Q3, Q4). Q5 and Q6 are used to connect the cell to the bit lines.

The cells are arranged in a two-dimensional array of 32 by 32 for a total of 1024 cells. Address lines 0 through 4 are decoded to select 1-of-32 word lines. Each word line drives 32 cells, connecting them to 32 pairs of bit lines. Addresses 5 through 9 are decoded to select 1-of-32 bit line pairs. Thus, the 10 address lines select one cell out of 1024 for reading or writing. The bit lines are ORed together and the selected pair drive the output data amplifier. When writing, the bit lines are driven by the write amplifiers to force the selected cell in one direction or the other.

MEMORY SYSTEMS

For those designers who have worked with dynamic memory systems, the dominant theme with the 2602 is the things that do not have to be done. With no clocks, no refreshing and no sensing, the designer can center his work on optimizing the TTL/MOS interfaces and the system packaging. Because of the lack of support circuitry around the 2602, the propagation paths to and from the memory chip are much shorter than is the case with dynamic memories. This fact will help to compensate for the somewhat longer access times of the 2602, although there are large numbers of applications where the 2602 offers more than sufficient speed. The lack of support circuits makes it easy to gain performance from the static memory by interleaving. The expensive dynamic support circuitry does not have to be duplicated for a two-way interleave.

The lack of power surge currents, high voltage transitions, low level sense currents, and multiple power supplies simplifies memory system designs in several ways. One significant result is that many systems will work very well on two-sided printed circuit boards, with consequent savings in design and production costs. With less board area devoted to supporting the memory chips, the board bit density can be increased.

Applications

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digital
linear
mos

signetics

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